To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Date: May.13.2008

RENESAS TECHNICAL UPDATE

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Renesas Technology Corp.

Product Category	MPU&MCU		Document No.	TN-SH7-A656A/E	Rev.	1.00
Title	Notice about DMA cycle steal mode		Information Category	Technical Notification		
Applicable Product	R5S72650P200BG R5S72651P200BG R5S72652P200BG R5S72653P200BG R5S72050W200BG	Lot No. ALL	Reference Document	・ SH7265 Group Hardware Manual Rev.1.00 (REJ09B0351-0100) ・ SH7205 Group Hardware Manual Rev.1.00 (REJ09B0372-0100)		

We would like to inform you of the notice about DMA cycle steal mode.

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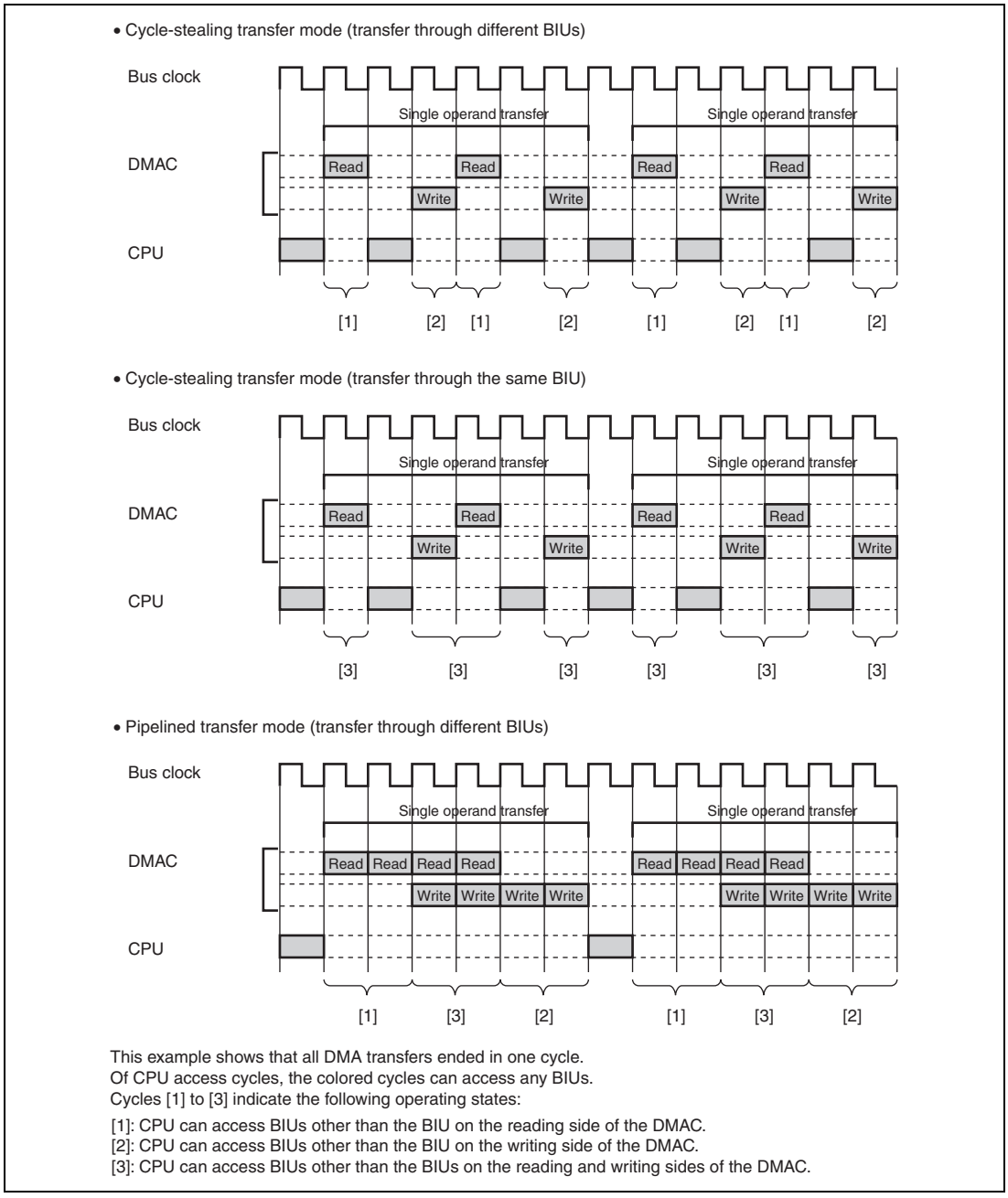
Before amendment



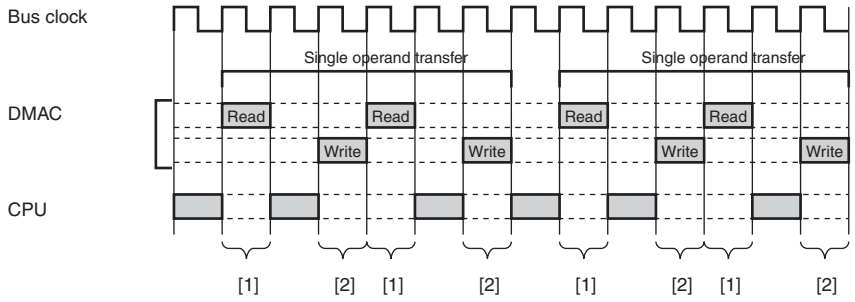
This example shows that all DMA transfers ended in one cycle.
Of CPU access cycles, the colored cycles can access any BIUs.
Cycles [1] to [3] indicate the following operating states:

[1]: CPU can access BIUs other than the BIU on the reading side of the DMAC.
[2]: CPU can access BIUs other than the BIU on the writing side of the DMAC.
[3]: CPU can access BIUs other than the BIUs on the reading and writing sides of the DMAC.

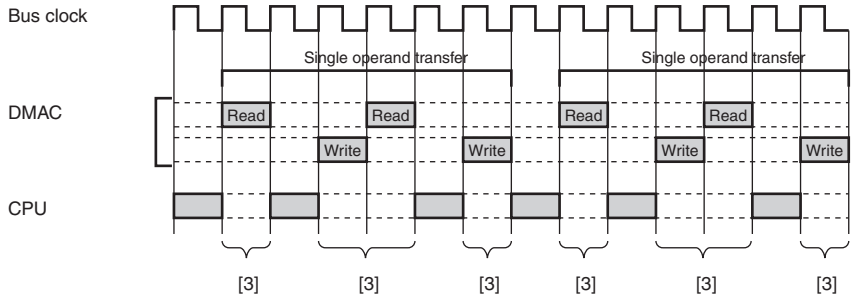
Figure 11.3 Example of Bus Mastership Alternation between DMAC and CPU in Various DMA Transfer Modes

After amendment

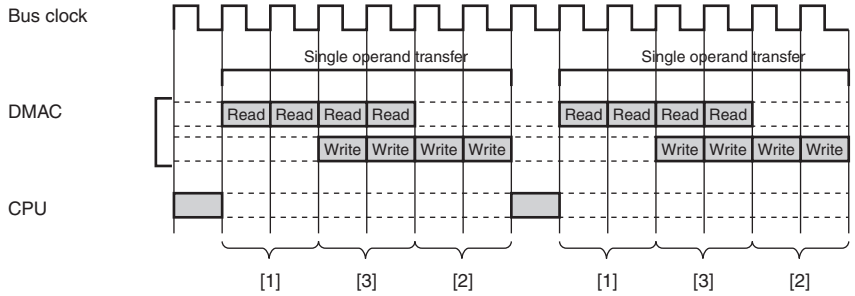
• Cycle-stealing transfer mode (transfer through different BIUs)



• Cycle-stealing transfer mode (transfer through the same BIU)



• Pipelined transfer mode (transfer through different BIUs)



This example shows that all DMA transfers ended in one cycle.
Of CPU access cycles, the colored cycles can access any BIUs.
Cycles [1] to [3] indicate the following operating states:

[1]: CPU can access BIUs other than the BIU on the reading side of the DMAC.
[2]: CPU can access BIUs other than the BIU on the writing side of the DMAC.
[3]: CPU can access BIUs other than the BIUs on the reading and writing sides of the DMAC.

However, when a DMA access to external address space followed by CPU access to external space is occurred, CPU access next to DMA cycle may not be occurred.

Figure 11.3 Example of Bus Mastership Alternation between DMAC and CPU in Various DMA Transfer Modes