HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	December 15, 1999	No.	TN-SH7 -201 A/E
THEME	Notes for using DMAC in clock mode 3 or 4		
CLASSIFICATION	☐ Spec. change ☐ Supplement of Documents	■ Limitation on Use	
PRODUCT NAME	HD6417709A, HD6417729		
REFERENCE DOCUMENTS	SH7709A (HD6417709A) Hardware manual SH7729 (HD6417729) Hardware manual	Effective Date Eternity From	

The following is the modification of Hitachi Semiconductor Technical Update TN-SH7-192A/E. The pin number in 2.1 is modified to "27-29" from "27-39" shown below with underlined.

SH7709A and SH7729 have followed usage notice.

1. Usage notice:
In the case of using DMAC in clock mode 3 or 4, illegal bus cycle may be caused by the jitter of internal PLLs because of the noise on Vcc/Vss line.

2. Work around:
Please perform the following method.

2.1 The case of using DMAC in clock mode 3 or 4
To reduce the influence of the noise, for example, by mounting decoupling capacitors for each Vcc/Vss pairs.
Vcc/Vss pairs:
19-21, <u>27-29</u>, 33-35, 45-47, 57-59, 69-71, 79-81, 83-85, 95-97, 109-111,
132-134, 153-154, 161-163, 173-175, 181-183, 205-208
3-6, 145-147, 148-150
Please refer to the following chapter of the hardware manual.
a) SH7709A hardware manual : 9.11 Notes on Board Design
b) SH7729 hardware manual : 10.11 Notes on Board Design

2.2 The case of that method 2.1 is insufficient
To use the clock mode 0,1,2,7 when using DMAC