## **RENESAS TECHNICAL UPDATE**

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Product Category	MPU/MCU	Document No.	TN-MC*-A025A/E	Rev.	1.00	
Title	Notes about the TEND bit in the status regist of Serial Peripheral Interface	Information Category	Technical Notification			
Applicable Product	See below	Lot No.				
		ALL	Reference Document	See below		

We would like to inform you of the following notice about the TEND bit in the status register (SPSR) of Serial Peripheral Interface.

[Description of the TEND bit]

This bit is set to 1 when transmission is completed.

And this is 0 when transmission is not completed.

[Clearing condition]

• When transmit data are moved from the transmit register to the shift register.

[Setting condition]

• When the number of data units in the transmit buffer (SPTX) is zero when a serial transfer is completed.

Note: This bit is valid only in SPI master mode.

Applicable Products and Reference Documents

Applicable Products			Devi	Description	
Series	Group	Reference Document Title	Rev.	Document No.	
	SH7262, SH7264	SH7262 Group, SH7264 Group User's Manual: Hardware	Rev.3.00	R01UH0134EJ0300	
SH7260 Series	SH7266, SH7267	SH7266 Group, SH7267 Group User's Manual: Hardware	Rev.2.00	R01UH0412EJ0200	
SH7200 Selles	SH7268, SH7269	SH7268 Group, SH7269 Group User's Manual: Hardware	Rev.2.00	R01UH0048EJ0200	
	SH726A, SH726B	SH726A Group, SH726B Group User's Manual: Hardware	Rev.1.00	R01UH0202EJ0100	
RZ/A Series	RZ/A1L	RZ/A1L Group User's Manual: Hardware	Rev.1.00	R01UH0437EJ0100	

