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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX-A015A/E	Rev.	1.00
Title	Note on Using Main Clock in RX210 Group		Information Category	Technical Notification		
Applicable Product	RX210 Group	Lot No. All	Reference Document	RX210 Group User's Manual: Hardware Rev.1.10 (R01UH0037EJ0110)		

1. Note

When selecting the main clock as the clock source in RX210 Group, the MCU may not operate properly due to a problem with the internal circuit.

2. Solution

Do not use the main clock as the system clock source, the reference clock for the clock frequency accuracy measurement circuit (CAC), and the clock to be measured by the CAC. Specifically, comply with the following instructions:

(1) Do not set the clock source select bits in the system clock control register 3 (SCKCR3.CKSEL[2:0]) to 010b (main clock oscillator).

(2) Do not set the frequency measurement clock select bits in the CAC control register 1 (CACR1.FMCS[2:0]) to 000b (output clock of main clock oscillator).

(3) Do not set the reference signal generation clock select bits in the CAC control register 2 (CACR2.RSCS[2:0]) to 000b (output clock of main clock oscillator).

(4) Do not set the sleep mode return clock source select bits in the sleep mode return clock source switching register (RSTCKCR.RSTCKSEL[2:0]) to 010b (main clock oscillator is selected).

The following pages contain the relevant descriptions in the user's manual.

■ The following descriptions are contained in pages 181, 207, 208, and 230 of RX210 Group User's Manual: Hardware.

9.2.2 System Clock Control Register 3 (SCKCR3)

Address(es): 0008 0026h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CKSEL[2:0]			—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10 to b8	CKSEL[2:0]	Clock Source Select	b10 b8 0 0 0: LOCO 0 0 1: HOCO 0 1 0: ~~Main clock oscillator~~ → Do not set 0 1 1: Sub-clock oscillator 1 0 0: PLL circuit Settings other than above are prohibited.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

10.2.2 CAC Control Register 1 (CACR1)

Address: 0008 B001h

	b7	b6	b5	b4	b3	b2	b1	b0
	EDGES[1:0]		TCSS[1:0]		FMCS[2:0]			CACREFE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CACREFE	CACREF Pin Input Enable	0: CACREF pin input is disabled. 1: CACREF pin input is enabled.	R/W
b3 to b1	FMCS[2:0]	Frequency Measurement Clock Select	b3 b1 0 0 0: ~~Output clock of main clock oscillator~~ → Do not set 0 0 1: Output clock of sub-clock oscillator 0 1 0: Output clock of high-speed on-chip oscillator 0 1 1: Output clock of low-speed on-chip oscillator 1 0 0: Output clock of IWDT-dedicated on-chip oscillator 1 0 1: Setting prohibited 1 1 0: Setting prohibited 1 1 1: Setting prohibited	R/W
b5, b4	TCSS[1:0]	Timer Count Clock Source Select	b5 b4 0 0: No division 0 1: × 1/4 clock 1 0: × 1/8 clock 1 1: × 1/32 clock	R/W
b7, b6	EDGES[1:0]	Valid Edge Select	b7 b6 0 0: Rising edge 0 1: Falling edge 1 0: Both rising and falling edges 1 1: Setting prohibited	R/W

10.2.3 CAC Control Register 2 (CACR2)

Address: 0008 B002h

	b7	b6	b5	b4	b3	b2	b1	b0
	DFS[1:0]		RCDS [1:0]		RSCS[2:0]			RPS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	RPS	Reference Signal Select	0: CACREF pin input 1: Internally generated signal	R/W
b3 to b1	RSCS[2:0]	Reference Signal Generation Clock Select	b3 b1 0 0 0: ~~Output clock of main clock oscillator~~ → Do not set 0 0 1: Output clock of sub-clock oscillator 0 1 0: Output clock of high-speed on-chip oscillator 0 1 1: Output clock of low-speed on-chip oscillator 1 0 0: Output clock of IWDT-dedicated on-chip oscillator 1 0 1: Setting prohibited 1 1 0: Setting prohibited 1 1 1: Setting prohibited	R/W
b5, b4	RCDS [1:0]	Reference Signal Generation Clock Frequency Division Ratio Select	b5 b4 0 0: × 1/32 clock 0 1: × 1/128 clock 1 0: × 1/1024 clock 1 1: × 1/8192 clock	R/W
b7, b6	DFS[1:0]	Digital Filter Selection	b7 b6 0 0: Digital filtering is disabled. 0 1: The sampling clock for the digital filter is the frequency measuring clock. 1 0: The sampling clock for the digital filter is the frequency measuring clock divided by 4. 1 1: The sampling clock for the digital filter is the frequency measuring clock divided by 16.	R/W

11.2.6 Sleep Mode Return Clock Source Switching Register (RSTCKCR)

Address(es): 0008 00A1h

	b7	b6	b5	b4	b3	b2	b1	b0
	RSTCKEN	—	—	—	—	RSTCKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	RSTCKSEL [2:0]	Sleep Mode Return Clock Source Select	b2 b0 0 0 1: HOCO is selected 0 1 0: ~~Main clock oscillator is selected~~ → Do not set Settings other than above are prohibited while the RSTCKEN bit is 1.	R/W
b6 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	RSTCKEN	Sleep Mode Return Clock Source Switching Enable	0: Clock source switching at sleep mode cancellation is disabled 1: Clock source switching at sleep mode cancellation is enabled	R/W

3. Changes to Electrical Characteristics

Along with the above, the current drawn of low-speed operating mode 1 was changed as follows:

Table 41.7 DC Characteristics (6)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Unit	Test Conditions
Current drawn*1	Medium-speed operating modes A and B	Normal operating mode	No peripheral operating	ICLK = 32 MHz	I_{CC}	7.0	mA	Ta = 25°C
				ICLK = 20 MHz		6.0		
			All peripherals operating	ICLK = 32 MHz		22.5		
				ICLK = 20 MHz		16.5		
		Sleep mode		ICLK = 32 MHz		5.0		
				ICLK = 20 MHz		4.6		
		All-module clock stop mode		ICLK = 32 MHz		4.5		
				ICLK = 20 MHz		4.3		
		Increase during BGO*2	Medium-speed operating mode A			25		
			Medium-speed operating mode B			20		
	Low-speed operating mode 1	Normal operating mode	No peripheral operating	ICLK = 1 MHz		~~0.68~~ → 1.43		
			All peripherals operating	ICLK = 1 MHz		~~2.4~~ → 3.15		
		Sleep mode		ICLK = 1 MHz		~~0.6~~ → 1.35		
		All-module clock stop mode				~~0.58~~ → 1.33		
	Low-speed operating mode 2	Normal operating mode	No peripheral operating	ICLK = 32 kHz		0.024		
			All peripherals operating	ICLK = 32 kHz		0.05		
		Sleep mode		ICLK = 32 kHz		0.02		
		All-module clock stop mode				0.018		