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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A846A/E	Rev.	1.00
Title	Note on Use of SH7786 Cache		Information Category	Technical Notification		
Applicable Product	SH7786 Group	Lot No. All lots	Reference Document	SH7786 Group User's Manual: Hardware Rev.1.00 Nov 30, 2010 (REJ09B0501-0100)		

There is a note on use of the SH7786 operand cache (OC) access.

[Note on use]

When a write access is executed to the memory-mapped OC address array with all of the following condition 1 to 3, the CPU may hang up.

- Condition

1) Both CPU core 0 and core 1 are operating (multi-processor operation, C0STBCR.MSTP0=0, C1STBCR.MSTP1=0).

2) The OC is used (CCR.OCE=1).

3) Cache coherency control is enable (CCR.CCD=0).

- Workaround

When above condition 1 to 3 are all satisfied, do not write to the OC address arrays by a memory-mapped write operation, use the cache operation instruction such as the OCBI, OCBP or OCBWB instruction.

Note that, the OCBI, OCBP or OCBWB instruction is executed correctly even if that effective address Rn[31:24] is H'F4 (OC address arrays area).

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