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RENESAS TECHNICAL UPDATE

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Title	Note on Use of SH7780 MMU LDTLB Instruction		Information Category	Technical Notification		
Applicable Product	SH7780 Group	Lot No. All lots	Reference Document	SH7780 Hardware Manual Rev.1.00 Dec.13.2005 (REJ09B0158-0100)		

There is a usage note for the LDTLB instruction of the SH7780 MMU (Memory Management Unit).

[Note on Using LDTLB Instruction]

When using an LDTLB instruction instead of software to a value to the MMUCR. URC, execute 1 or 2 below.

1. In 29-bit address mode, follow A. and B. below. In 32-bit address mode, follow A. through D. below.

A. Place the TLB miss exception handling routine*1 only in the P1, P2 area ,or the on-chip memory so that all the instruction accesses*3 in the TLB miss exception handling routine should occur solely in the P1, P2 area, or the on-chip memory. Clear the RP bit in the RAMCR register to 0 (initial value), when the TLB miss exception handling routine is placed in the on-chip memory. In the SH7780 hardware manual, it describes that the exception handling vector address and the LDTLB instruction should be located in the P1 or P2 area, and not the on-chip memory area. However, when RAMCR.RP=0, the on-chip memory area is not the target of the MMU related exception. Thus, when there is no change from RAMCR.RP=0, it is possible to use the on-chip memory area for the exception handling routine.

B. Use only one page of the PMB for instruction accesses*3 in the TLB miss exception handling routine*1. In 32-bit address mode, do not place them in the last 64 bytes of a page of the PMB.

C. In 32-bit address mode, obey 1 and 2 below when recording information in the UTLB in the MMU-related exception*2 handling routine.

a. When the TLB miss exception occurs, and recording the information of a page with the access right in the UTLB, do not record the page, in which the exception has occurred, in the UTLB using the following two operations.

- Specifies the protection key data that causes a protection violation exception upon re-execution of the instruction that has caused the TLB miss exception and records the page, in which the TLB miss exception has occurred, in the UTLB.
- Specifies the protection key data that does not cause a protection violation exception in the protection violation exception handling routine to record the page in the UTLB and re-executes the instruction that has caused the protection violation exception.

b. When an initial page write exception occurs and the TLB entry in the UTLB of which the dirty bit is 1 is replaced, before the write instruction for the page corresponding to this replaced TLB entry is completed, register the TLB entry of which the dirty bit is 1.

D. Do not make an attempt to execute the FDIV or FSQRT instruction in the TLB miss exception handling routine.

2. If a TLB miss exception occurs, add 1 to MMUCR.URC before executing an LDTLB instruction.

Notes: 1. An exception handling routine is an entire set of instructions that are executed from the address (VBR + offset) upon occurrence of an exception to the RTE for returning to the original program or to the RTE delay slot. However, when an interrupt is acknowledged with the exception handling routine, includes until the executed instruction when the interrupt is acknowledged, and not include the instructions from the address VBR+H'0600 which is the branch due to the interrupt and the instructions after this.

2. MMU-related exceptions are: instruction TLB miss exception, instruction TLB miss protection violation exception, data TLB miss exception, data TLB protection violation exception, and initial page write exception.

3. Instruction accesses include the entire TLB miss exception handling routine, which is from the beginning till the end and the PREFI and ICBI instructions.

[Note]

For details of the LDTLB instruction and other instruction, refer to section 10 Instruction Description of the SH-4A Software Manual.

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