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GRADE A

MSC TECHNICAL NEWS

No.M16C-10-9707

Note on accessing addresses 3E0$_{16}$ to 3FF$_{16}$ of the M16C/60 and M16C/61 group MCU

1. Related devices

M16C/60 group, M16C/61 group

2. Symptoms

When using a M16C/6X emulator device, under certain conditions there is a possibility that port and direction register values are falsely written to. This problem only occurs with an emulator device (mask ROM, EPROM, one time PROM versions are not affected).

3. Conditions causing a false write

A false write to port and direction registers can occur under the following conditions:

- External oscillation frequency is greater than 8MHz. The exact frequency at which the false write occurs varies per emulation pod.

- The main clock is not divided (bits 6 and 7 of System Clock Control Register 1 are 00$_2$).

- No wait states are inserted (bit 7 of Processor Mode Register 1 is 0$_2$).

- Immediately after accessing addresses 3E0$_{16}$ to 3FF$_{16}$ (port data and direction registers), a write is executed to a memory address with a value greater than 400$_{16}$, and the lower 5 bits of the address are in the range 01100$_2$-11111$_2$.

- An emulator device is being used (not mask ROM, EPROM, or one time PROM version).

4. Tentative solutions

- Change oscillation frequency to be less than 8MHz.

- Insert a wait state during memory access.

- When executing a data transfer from address range $3E0_{16}$-$3FF_{16}$ to memory (a memory-to-memory transfer), transfer the data through a register.

Insert a dummy read cycle between the memory-to-register and register-to-memory transfer instructions.

```
Example:    (bad)     mov.b   3F4h,7F0h

            (good)    mov.b   3F4h,R0L
                      mov.b   400h,400h     ;dummy read cycle
                      mov.b   R0L,7F0h
```

- When executing a data transfer from a register to memory immediately after writing to an address in the range $3E0_{16}$-$3FF_{16}$

Insert a dummy read cycle between the register-to-memory instruction and the memory access.

```
Example:    (bad)     and.b   700h,3F4h
                      mov.b   R0L,7F0h

            (good)    and.b   700h,3F4h
                      mov.b   400h,400h     ;dummy read cycle
                      mov.b   R0L,7F0h
```

5. Permanent solution

Exchange an old emulator chip with a new emulator chip in the existing pod (upon availability). As soon as a new emulator chip has been developed, all customers, as well as third party tools vendors, will be informed.

6. Cause

In the emulator device, an internal port pre-decode signal is delayed and remains active for a short time after an access to address range $3E0_{16}$ to $3FF_{16}$ is completed. This delayed signal overlaps with the write signal used for the next memory access.
Data is written incorrectly to the corresponding SFR whose address is internally decoded by the pre-decode signal and the lower 5 address bits of the memory access.
Table 1 shows the correspondence between the affected SFR and the lower 5 address bits (in the range 01100_2-11111_2).

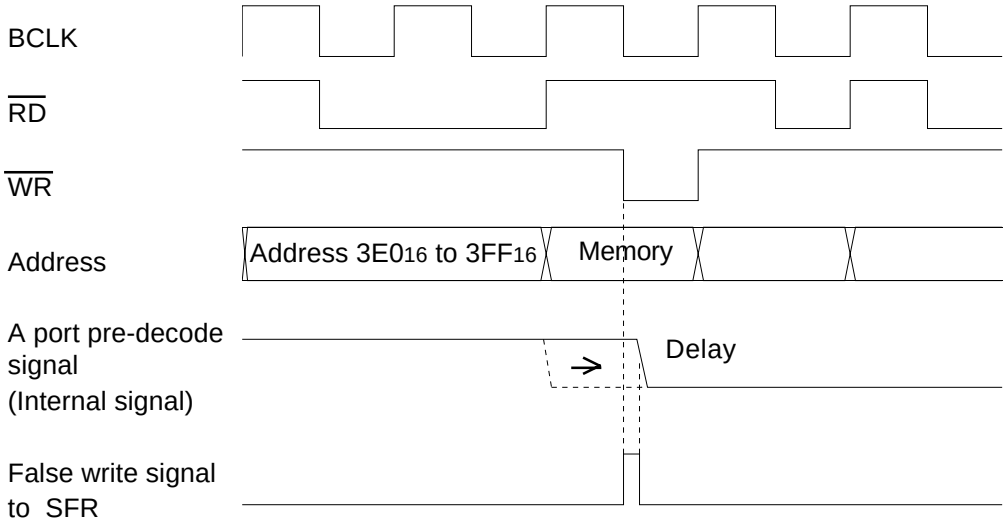

Table 1. Related lower 5 bits of memory and SFR that a false write is done

Lower 5 bits	Corresponding SFR	Lower 5 bits	Correspondence SFR
01100_2	Port P6 (P6)	10110_2	Port P10 direction register (PD10)
01101_2	Port P7 (P7)	10111_2	-
01110_2	Port P6 direction register (PD6)	11000_2	-
01111_2	Port P7 direction register (PD7)	11001_2	-
10000_2	Port P8 (P8)	11010_2	-
10001_2	Port P9 (P9)	11011_2	-
10010_2	Port P8 direction register (PD8)	11100_2	Pull up control register 0 (PUR0)
10011_2	Port P9 direction register (PD9)	11101_2	Pull up control register 1 (PUR1)
10100_2	Port P10 (P10)	11110_2	Pull up control register 2 (PUR2)
10101_2	-	11111_2	-

- not a problem since SFR isn't assigned

7. Memory access methods which could result in a false write

(1) During a DMA transfer from address range $3E0_{16}$-$3FF_{16}$ to a memory address with a value greater than 400_{16}, and the lower 5 bits of the address are as shown in Table 1

(2) During a DMA transfer from memory to address range $3E0_{16}$-$3FF_{16}$

(3) During a transfer instruction under the conditions shown in Table 2

```
Example:    mov.b   3F4h,7F0h    ;Address 3F4(16) = Port P10, address 7F0(16) = RAM
                                 ;The value of port P8 may be altered because
                                 ;lower 5 bits of transfer address are 10000(2) (see Table 1)
```

Table 2. Transfer instructions and addressing modes

Instruction	Addressing mode		Condition
MOV	src	[An], dsp:8[An], dsp:8[SB], dsp:8[FB] dsp:16[An], dsp:16[SB], abs16 dsp:8[SP]	When the src address is in the range $3E0_{16}$-$3FF_{16}$ and the dest address is greater than 400_{16}, and the lower 5 bits of the dest address are as shown in Table 1.
	dest		
LDE	src	abs20, dsp:20[A0], [A1A0]	
	dest	[An], dsp:8[An], dsp:8[SB], dsp:8[FB] dsp:16[An], dsp:16[SB], abs16	
PUSH	src		When the src address is in the range $3E0_{16}$-$3FF_{16}$ and the saved address is greater than 400_{16}, and the lower 5 bits of the dest address are as shown in Table 1.

(4) During a transfer instruction under the conditions shown in Table 4, immediately after a write to address range $3E0_{16}$-$3FF_{16}$ under the conditions shown in Table 3

```
Example:    add.b   700h,3F4h    ;address 3F4(16)=Port P10
                                 ;address 700(16)=RAM
            mov.b   R0L,7F0h     ;address 7F0(16)=RAM
```

Table 3. Instructions that write to address range 3E0$_{16}$-3FF$_{16}$ and addressing modes

Instruction	Addressing mode		Conditions
MOV	src	All addressing modes	When the dest address is in the range 3E0$_{16}$-3FF$_{16}$
	dest	[An], dsp:8[An], dsp:8[SB], dsp:8[FB] dsp:16[An], dsp:16[SB], abs16 dsp:8[SP]	
MOVDir	src	R0L	
	dest	[An], dsp:8[An], dsp:8[SB], dsp:8[FB] dsp:16[An], dsp:16[SB], abs16	
POP ROLC RORC ABS ADCF EXTS NEG NOT	dest		
LDE ROT SHA SHL ADC ADD MUL MULU SBB SUB AND OR XOR STC	src	All addressing mode	
	dest	[An], dsp:8[An], dsp:8[SB], dsp:8[FB] dsp:16[An], dsp:16[SB], abs16	
STE	src	All addressing mode	
	dest	dsp:20[A0], abs20, [A1A0]	
STNZ STZ STZX	src	#IMM8	
	dest	dsp:8[SB], dsp:8[FB], abs16	
BCLR BNOT BSET	dest	[An], base:8[An], bit,base:8[SB] bit,base:8[FB], base:16[An] bit,base:16[SB], bit,base:16 bit,base:11[SB]	
BMCnd	dest	[An], base:8[An], bit, base:8[SB] bit,base:8[FB], base:16[An] bit,base:16[SB], bit,base:16	
DEC INC	dest	dsp:8[SB], dsp:8[FB], abs16	

Table 4. Transmission instructions and addressing modes

Instruction	Addressing mode		Conditions
MOV	src	Rn, An	When the src address is a register and the dest address is greater than 400$_{16}$, and the lower 5 bits of the dest address areas shown in Table 1
	dest	[An], dsp:8[An], dsp:8[SB], dsp:8[FB] dsp:16[An], dsp:16[SB], abs16 dsp:8[SP]	
STC	src	All addressing mode	
	dest	[An], dsp:8[An], dsp:8[SB], dsp:8[FB]	