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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-V85-A025A/E	Rev.	1.00
Title	Note about the RY output delay time of the clock synchronous serial interface (CSIG)		Information Category	Technical Notification		
Applicable Product	V850E2/Dx4 series V850E2/Dx4-H series	Lot No. All lots	Reference Document	Data Sheet of each product		

There is modification in an electrical characteristic of clock synchronous serial interface (CSIG) CSIG0RY output delay time.

This RENESAS Technical update will mention the change contents and the manual correction contents.

1. Modification items

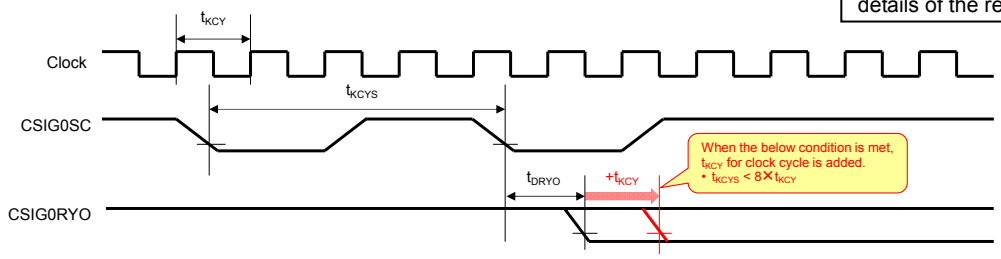
(1) Electrical characteristic change at the CSIG slave mode (CSIG0RY output delay time).

When CSIGnSC cycle time (tKCYS) is smaller than 8 times of the Module clock cycle time (tKCY) as following figure 1, 1 cycle tKCY is added to the CSIG0RY output delay time (tDRYO).

There is no spec change when CSIGnSC cycle time (tKCYS) is more than 8 times of the Module clock cycle time.

Note:
Refer to User Manual of each product for details of the register and its setting.

■ CSIG (CSIG0CFG0.CSIG0CKP / CSIGnCTL1.CSIGnCKR = 0/0 or 1/1)



■ CSIG (CSIG0CFG0.CSIG0CKP / CSIGnCTL1.CSIGnCKR = 0/1 or 1/0)

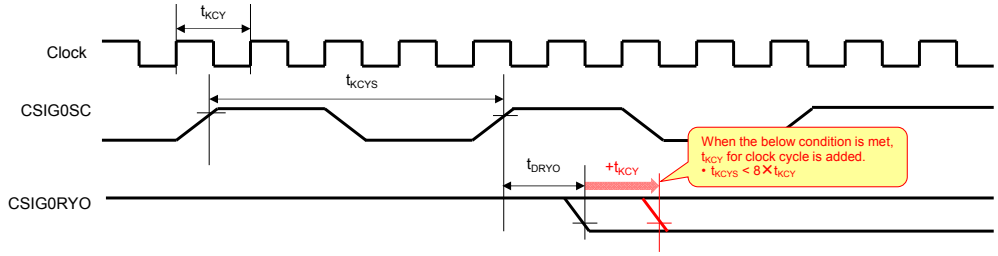


Figure 1. CSIG0SC and CSIG0RY timing chart

2. Manual modification

(1) CSIG Electrical characteristic modification points

The CSIG0RY output delay time (tDRYO) is changed as below.

Parameter	CT	Symbol	Condition		Ratings			Unit
					MIN.	TYP.	MAX.	
Ready / Busy output signal (CSIG0RY) output delay time (vs. CSIG0SC input)[d]	DS	tDRYO	filtered (DNF) [a]	tKCYS ≧ 8×tKCY			30 + tdDNFSCI(max)	ns
				tKCYS < 8×tKCY			30 + tdDNFSCI(max) + tKCY	ns
			filter-bypassed [c]	tKCYS ≧ 8×tKCY			30	ns
				tKCYS < 8×tKCY			30+tKCY	ns