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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0123A/E	Rev.	1.00
Title	The method of updating AFL entry of CANFD during communication		Information Category	Technical Notification		
Applicable Product	RA6M5 Group	Lot No. All	Reference Document	Renesas RA6M5 Group User's Manual: Hardware Rev.1.20		

The method of updating AFL entry of CANFD during communication and the incorrect description are updated as follows.

1) The following register descriptions are added between 32.2.83 and 32.2.84

32.2.x CFDGAFLIGNENT : Global AFL Ignore Entry Register

Base address: CANFD = 0x400B_0000
Offset address: 0x1324

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ICN
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	IRN[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	IRN[7:0]	Define rule number which ignores an AFL entry	R/W
15:8	-	These bits are read as 0. The write value should be 0.	R/W
16	ICN	Define channel number which ignores an AFL entry	R/W
31:17	-	These bits are read as 0. The write value should be 0.	R/W

IRN[7:0] bits (Ignore Rule Number)
These bits define the rule number which updates an AFL entry.
Users should enter, only the values between 0 and 127 inclusive.
only write to these bits when CFDGAFLIGNCTR.IREN bit is 0b.
Users cannot write to these bits when the CAN-FD module is in GL_SLEEP mode.

ICN bit (Ignore Channel Number)
This bit defines the channel number which updates an AFL entry.
Users should enter, only the values between 0 and 1 inclusive.
Users should only write to this bit when CFDGAFLIGNCTR.IREN bit is 0b.
Users cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

32.2.y CFDGAFLIGNCTR : Global AFL Ignore Control Register

Base address: CANFD = 0x400B_0000
Offset address: 0x1328

Bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								-	-	-	-	-	-	-	IREN
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IREN	0: AFL entry number does not ignore 1: AFL entry number ignores	R/W
7:1	-	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	These bits control the right or wrong of rewriting of a IREN bit.	W
31:16	-	These bits are read as 0. The write value should be 0.	R/W

IREN bit (Ignore entry Enable)
When this bit is set, the entry number (selected by CFDGAFLIGNENT register) is ignored.
This bit is cleared automatically when CAN-FD module enters GL_RESET mode.

KEY[7:0] (Key code)
When 0xC4 is written in these bits, the write of a IREN bit becomes available.
Read value from these bits is always 0x00.
Users should write IREN bit and KEY bits simultaneously.

2) The following descriptions are updated in 32.2.19

32.2.19 CFDGAFLCFG0 : Global Acceptance Filter List Configuration Register 0

(omission)

The Global Acceptance Filter List Configuration Register 0 is used to define the number of rules for entries in the Acceptance Filter List, applicable for channels 0 to 1.
The total number of available entries in the Acceptance Filter List is 64 × (n + 1), 128 for 2 CAN channels. However, the filters can be allocated flexibly to the different channels depending on requirements as long as both of the following conditions are satisfied:

- The maximum number of acceptance filter per channel is **128**
- The total number of rules defined for all channels is not exceeding the number of available entries in the Acceptance Filter List.

3) The following descriptions are added after 32.5.6 .

32.5.7 Updating AFL entry during communication

User can update the AFL entry without disabling all CAN communications.
User chooses the entry number which is due to be updated.
Set AFL entry number/**CFDGAFLIGNENT.IRN** and channel number/**CFDGAFLIGNENT.ICN**.
Then set ignore enable bit/**CFDGAFLIGNCTR.IREN**, and .KEY/ **CFDGAFLIGNCTR.KEY**
This entry number is ignored from AFL matching while user update the entry.
Figure 32.28 shows the AFL entry update flow.

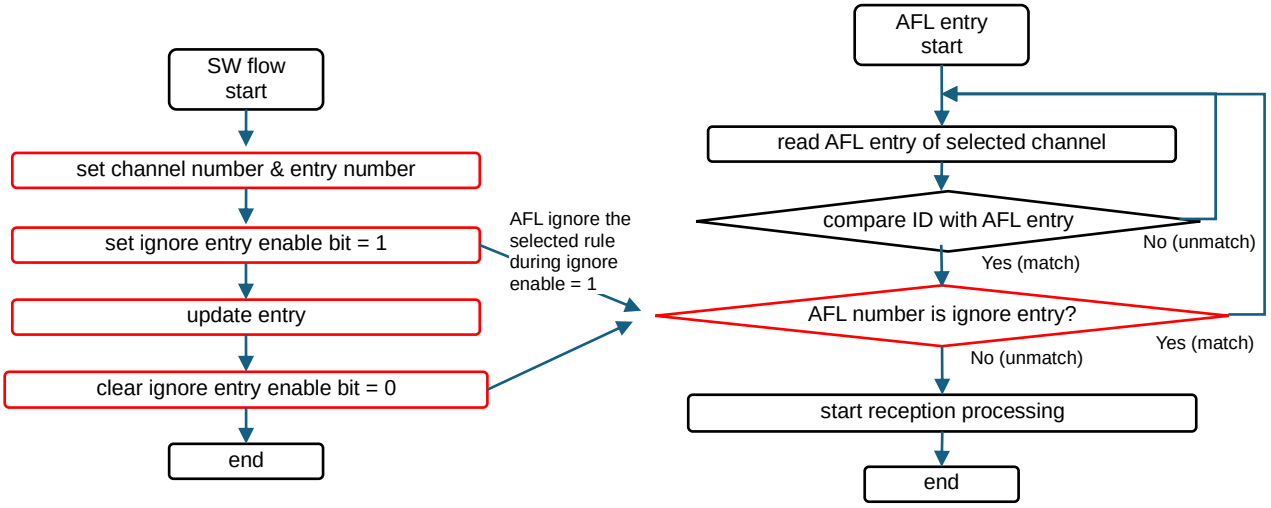

Figure 32.28 AFL entry update flow

The method of update of an AFL entry is shown below.
(1) Set entry number and a channel number to **CFDGAFLIGNENT** register
(2) Set the value 0xC401 (key code & set ignore entry enable bit) to **CFDGAFLIGNCTR** register.
(3) Set entry page to **CFDGAFLECTR** register. This page includes the selected entry.
CFDGAFLECTR.AFLDAE is set to 1b.
(4) Set the new rule to **CFDGAFLIDn, CFDGAFLMn, CFDGAFLP0n, CFDGAFLP1n** registers.
(5) **CFDGAFLECTR.AFLDAE** is cleared to 0b.
(6) Set the value 0xC400 (key code & clear ignore entry enable bit) to **CFDGAFLIGNCTR** register.

(*) This updating entry number becomes ignoring for RXSCAN during the periods from (2) to (6).

For example: case1
When total entry is 6 per channel, delete one of the entries.
Current entry is follows. Delete the entry3 of channel 1.

		entry number of page0	
for channel 0	entry0	0	ID=0x050
(total entry=6)	entry1	1	ID=0x051
	entry2	2	ID=0x052
	entry3	3	ID=0x053
	entry4	4	ID=0x054
	entry5	5	ID=0x055
for channel 1	entry0	6	ID=0x150
(total entry=6)	entry1	7	ID=0x151
	entry2	8	ID=0x152
	entry3	9	ID=0x153 ←delete rule
	entry4	10	ID=0x154
	entry5	11	ID=0x155
for channel 2	entry0	12	ID=0x250
(total entry=4)	entry1	13	ID=0x251
	entry2	14	ID=0x252
	entry3	15	ID=0x253

How to delete the entry
(1) Set 32'h0001_0003 to **CFDGAFLIGNENT** register.
(2) Set 32'h0000_c401 to **CFDGAFLIGNCTR** register
(3) Set 32'h0000_0100 to **CFDGAFLECTR** register
(4) Set same rule as previous rule by accessing to **CFDGAFLIDn**, **CFDGAFLMn**, **CFDGAFLP0n**, **CFDGAFLP1n** (n=9, this is entry3 of channel 1)
(5) Set 32'h0000_0000 to **CFDGAFLECTR** register
(6) Set 32'h0000_c400 to **CFDGAFLIGNCTR** register
Finish to delete the entry3 of channel 1. Current entry is follows

		entry number of page0	
for channel 0	entry0	0	ID=0x050
(total entry=6)	entry1	1	ID=0x051
	entry2	2	ID=0x052
	entry3	3	ID=0x053
	entry4	4	ID=0x054
	entry5	5	ID=0x055
for channel 1	entry0	6	ID=0x150
(total entry=5)	entry1	7	ID=0x151
	entry2	8	ID=0x152
	entry3	9	ID=0x152 ←set rule same as previous rule
	entry4	10	ID=0x154
	entry5	11	ID=0x155
for channel 2	entry0	12	ID=0x250
(total entry=4)	entry1	13	ID=0x251
	entry2	14	ID=0x252
	entry3	15	ID=0x253

For example: case2

When total entry is 6 per channel, add one of the entries.
Current entry is follows. New entry is added to entry3 of the channel 1.

		entry number of page0		
for channel 0	entry0	0	ID=0x050	
(total entry=6)	entry1	1	ID=0x051	
	entry2	2	ID=0x052	
	entry3	3	ID=0x053	
	entry4	4	ID=0x054	
	entry5	5	ID=0x055	
for channel 1	entry0	6	ID=0x150	
(total entry=5)	entry1	7	ID=0x151	
entry2=entry3	entry2	8	ID=0x152	
	entry3	9	ID=0x152	←add new rule in this position
	entry4	10	ID=0x154	
	entry5	11	ID=0x155	
for channel 2	entry0	12	ID=0x250	
(total entry=4)	entry1	13	ID=0x251	
	entry2	14	ID=0x252	
	entry3	15	ID=0x253	

How to add entry
(1) Set 32'h0001_0003 to **CFDGAFLIGNENT** register.
(2) Set 32'h0000_c401 to **CFDGAFLIGNCTR** register
(3) Set 32'h0000_0100 to **CFDGAFLECTR** register
(4) Set new rule by accessing to **CFDGAFLIDn**, **CFDGAFLMn**, **CFDGAFLP0n**, **CFDGAFLP1n**
(**n**=9, this is entry3 of channel 1)
(5) Set 32'h0000_0000 to **CFDGAFLECTR** register
(6) Set 32'h0000_c400 to **CFDGAFLIGNCTR** register
Finish to add entry. Current entry is follows

		entry number of page0		
for channel 0	entry0	0	ID=0x050	
(total entry=6)	entry1	1	ID=0x051	
	entry2	2	ID=0x052	
	entry3	3	ID=0x053	
	entry4	4	ID=0x054	
	entry5	5	ID=0x055	
for channel 1	entry0	6	ID=0x150	
(total entry=6)	entry1	7	ID=0x151	
	entry2	8	ID=0x152	
	entry3	9	ID=0x156	←add new rule
	entry4	10	ID=0x154	
	entry5	11	ID=0x155	
for channel 2	entry0	12	ID=0x250	
(total entry=4)	entry1	13	ID=0x251	
	entry2	14	ID=0x252	
	entry3	15	ID=0x253	

AFL entry can be used to the range set **CFDGAFLCFG0**. An addition and deletion of an entry are possible in it. Therefore, it is necessary to set the maximum number to be used to **CFDGAFLCFG0**.