To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A571A/E	Rev.	1.00
Title	Manual correction about synchronous DRAM Interface when using 64-bit bus width (SH7750R only)		Information Category	Technical Notification		
Applicable Product	SH7750R (HD6417750R)	Lot No. All lots	Reference Document	SH7750 Series Hardware Manual (ADE-602-124E Rev.6.0)		

The description of the bus state controller (BSC) of the SH7750 series hardware manual is corrected in the following section.

13.3.5 Synchronous DRAM Interface last clause

Connecting a 128-Mbit/256-Mbit Synchronous DRAM with 64-bit Bus Width (SH7750ROnly):

"Notes on Usage" fourth bullet item

This description is applied to the example of using the CS3# (#: low active) pin and connecting the SDRAMs to areas 2 and 3 showing in figure 13.45 in the manual. Please refer to the following for the details.

Red part with underline is corrected or added.

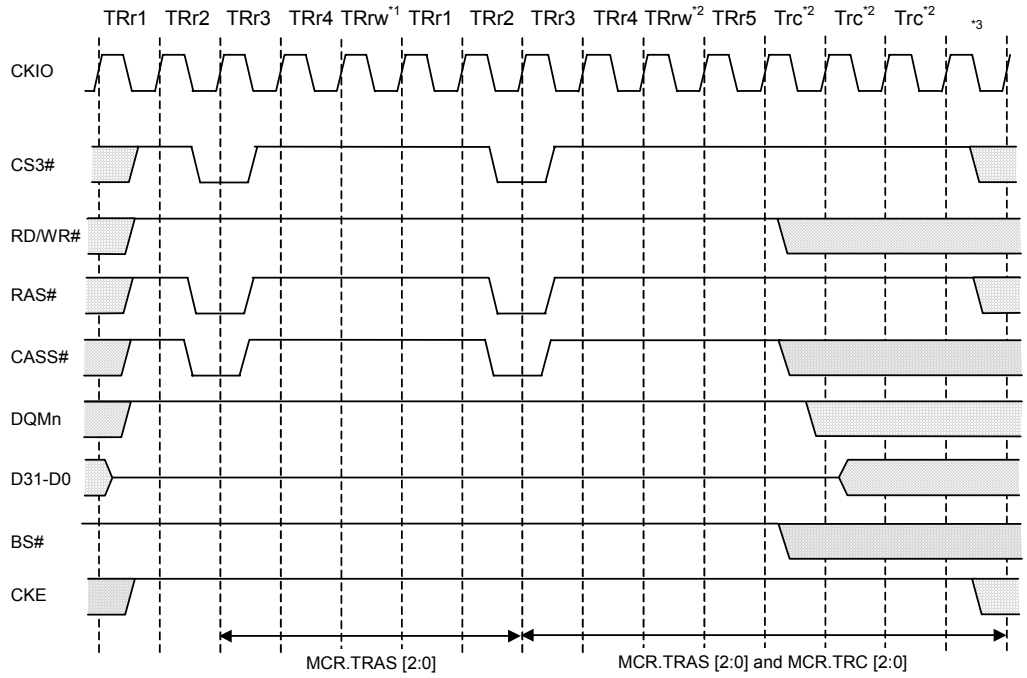
[After correction]

13.3.5 Synchronous DRAM Interface

Connecting a 128-Mbit/256-Mbit Synchronous DRAM with 64-bit Bus Width (SH7750R Only):

Notes on Usage

- BCR1.DRAMTP2-DRAMTP0 = 011: Sets areas 2 and 3 as synchronous-DRAM-interface spaces.
- MCR.SZ = 00: Sets the bus width of the synchronous DRAM to 64 bits.
- MCR.AMX = 6: Selects the 128-Mbit or 256-Mbit address-multiplex setting for the synchronous DRAM.
- In the auto-refresh operation, the REF command is issued **twice continuously** in response to a single refresh request. **The interval cycle number between the first and second REF commands issuance is specified by the setting of the TRAS2-TRAS0 bits in MCR, which is 4 to 11 CKIO cycles. The interval cycle number between the second REF command and the next ACTV command issuance is specified by the settings of both the TRAS2-TRAS0 bits and the TRC2-TRC0 bits in MCR in the sum total, which is 4 to 32 CKIO cycles.** Set RTCOR, bits CKS2–CKS0, **and MCR** so as to satisfy the refresh-interval rating of the synchronous DRAM which you are using. **The synchronous DRAM auto-refresh timing with 64-bit bus width is shown below figure.**
- When setting the mode register of the synchronous DRAM, set the address for area 2 first.
- Control signals required in this connection are RAS#, CASS#, RD/WR#, CS3#, DQM0-DQM7, and CKE. CS2# is not used.
- Do not use partial-sharing mode. If you use this, correct operation is not guaranteed.



Notes: *1 The interval cycle number between the first and second REF commands is 4 + TRrw x m (m=0 to 7) CKIO cycles by the setting of the TRAS[2:0] bits.

*2 The interval cycle number between the second REF command and the ACTV command after the refresh operation is 4 + TRrw x m (m=0 to 7) + 3Trc x n (n=0 to 7) CKIO cycles by the setting of the TRAS[2:0] bits and the TRC[2:0] bits.

*3 The next ACTV command is issued at TRr3 to TRr5 (including TRrw x m) + 3Trc x n (n=0 to 7) + 1 CKIO cycles after second REF command in this refresh operation. This 1 CKIO cycle is included in the setting of the TRAS[2:0] bits. Set MCR.TRAS[2:0], MCR.TRC[2:0], RTCOR and RTCSR.CKS[2:0] so as to satisfy the specification of the synchronous DRAM.

Figure Synchronous DRAM Auto-Refresh Timing with 64-Bit Bus Width (TRAS[2:0]=001,TRC[2:0]=001)