To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	Application specific IC		Document No.	TN-ASP-022A/E	Rev.	1.00
Title	M66291 Usage Precautions of the Buffer memory initialization by the Control Read Buffer		Information Category	Technical Notification		
Applicable Product	USB ASSP M66291	Lot No.	Reference Document	M66291 Data Sheet (REJ03F0125)		

1. Phenomenon

When sending/receiving packets other than EP0 (EP1, EP2, etc.), the buffer clear process (see Note 1) is disabled when executed in the Control Read Buffer (the buffer used for control read transfers).

2. Occurrence Conditions

This phenomenon occurs when the buffer clear process (see Note 1) is executed in the Control Read Buffer during any of the following three packet transfers (during the periods described).

* This phenomenon does not affect systems in which the control read transfer process does not occur after configuration.

(1) Bulk/Interrupt OUT transfer (ACK response):

phenomenon will occur between DATA packet receive start and ACK response completion

(2) Bulk/Interrupt IN transfer (ACK response):

phenomenon will occur between DATA packet send start and ACK receive completion

(3) Isochronous OUT/IN transfer (normal send/receive):

phenomenon will occur between DATA packet send/receive start and completion.

3. Countermeasures

Repeat the Control Read Buffer buffer clear process until normal completion.

Specifically, use the clear process as described below (also see Fig. 1).

1. Execute Control Read Buffer buffer clear process (see Note 1).
2. Wait 105ns or more after Step 1.
3. Confirm E0req. Repeat Steps 1 and 2 until E0req is “0” (normal completion)

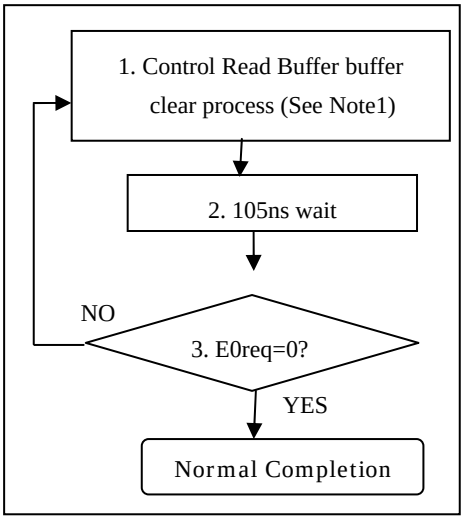

Figure 1. Buffer clear for Control Read Buffer

Note 1: When ISEL = 1, set EP0_BCLR = 1.

Related Terms:

ISEL: Buffer select (EP0_FIFO select register bit 0)

EP0_BCLR: Buffer clear (EP0_FIFO control register bit 12)

E0req: EP0_FIFO ready (EP0_FIFO control register bit 11)