To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-16C-A163A/E	Rev.	1.00
Title	M32C/87 Group Document Revision for UART5 and UART6 in Serial interfaces (Serial I/O)		Information Category	Technical Notification		
Applicable Product	M32C/87 Group	Lot No.	Reference Document			

The description of the UiC0 register (UARTi Transmit/Receive Control Register 0) (i = 0 to 6) has been revised.

When using the subject documents, please pay attention to the changes.

1. Subject Documents

M32C/87 Group Hardware Manual Rev.0.20
M32C/87 Group (M32C/87, M32C/87A, M32C/87B) Hardware Manual Rev.1.00

2. Corrections

Refer to the following page in the subject documents.

M32C/87 Group Hardware Manual Rev.0.20
Page 196 (Figure 16.7) U0C0 to U6C0 registers

M32C/87 Group (M32C/87, M32C/87A, M32C/87B) Hardware Manual Rev.1.00
Page 200 (Figure 17.7) U0C0 to U6C0 registers

Rev.1.00 is used as an example for corrections shown in the following pages.

M32C/87 Group (M32C/87, M32C/87A, M32C/87B) Hardware Manual Rev.1.00 Page 200

UiC0 register (UARTi Transmit/Receive Control Register 0) (i = 0 to 6) (Before)

UARTi Transmit/Receive Control Register 0 (i = 0 to 6)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
U0C0 to U4C0	$036C_{16}$, $02EC_{16}$, $033C_{16}$, $032C_{16}$, $02FC_{16}$	$0000\ 1000_2$
U5C0, U6C0	$01C4_{16}$, $01CC_{16}$	$0000\ 1000_2$

Bit Symbol	Bit Name	Function	RW
CLK0	UiBRG Count Source Select Bits	b1 b0 0 0: Selectes f_1 0 1: Selectes f_8 1 0: Selectes f_{2n}(2) 1 1: Do not set to this value	RW
CLK1			RW
CRS	$\overline{CST}/\overline{RTS}$ Function Select Bit	Enabled when CRD=0 0: Selects $\overline{CTS}$ function 1: Selects $\overline{RTS}$ function	RW
TXEPT	Transmit Register Empty Flag	0: Data in the transmit register (during transmission) 1: No data in the transmit register (transmission is completed)	RO
CRD	$\overline{CTS}/\overline{RTS}$ Disable Bit	0: Enables $\overline{CTS}/\overline{RTS}$ function 1: Enables $\overline{CTS}/\overline{RTS}$ function	RW
NCH	Data Output Select Bit(1)	0: TXDi/SDAi and SCLi are ports for the CMOS output 1: TXDi/SDAi and SCLi are ports for the N-channel open drain output	RW
CKPOL	CLK Polarity Select Bit	0: Data is transmitted on the falling edge of the transfer clock and data is received on the rising edge 1: Data is transmitted on the rising edge of the transfer clock and data is received on the falling edge	RW
UFORM	Transfer Format Select Bit(3)	0 : LSB first 1 : MSB first	RW

NOTES:

Deleted

1. $P7_0$/TXD2 and $P7_1$/SCL2 are ports for the N-channel open drain output, but not for the CMOS output. This is used as the TXDi port only in UART5 and UART6.
2. The CNT3 to CNT0 bits in the TCSPR register select no division (n = 0) or divide-by-2n (n = 1 to 15).
3. The UFORM bit setting is enabled when the SMD2 to SMD0 bits in the UiMR register are set to "001_2" (clock synchronous serial I/O mode) or "101_2" (UART mode, 8-bit transfer data). Set the UFORM bit to "1" when setting the SMD2 to SMD0 bits to "010_2" (I^2C mode), or to "0" when setting them to "100_2" (UART mode, 7-bit transfer data) or "110_2" (UART mode, 9-bit transfer data).

Figure 17.7 U0C0 to U6C0 Registers

UiC0 register (UARTi Transmit/Receive Control Register 0) (i = 0 to 6) (After)

UARTi Transmit/Receive Control Register 0 (i = 0 to 6)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
U0C0 to U4C0	036C16, 02EC16, 033C16, 032C16, 02FC16	0000 10002
U5C0, U6C0	01C416, 01CC16	0000 10002

Bit Symbol	Bit Name	Function	RW
CLK0	UiBRG Count Source Select Bit	b1 b0 0 0: Selectes f1 0 1: Selectes f8 1 0: Selectes f2n(2) 1 1: Do not set to this value	RW
CLK1			RW
CRS	$\overline{CST}$/$\overline{RTS}$ Function Select Bit	Enabled when CRD=0 0: Selects $\overline{CTS}$ function 1: Selects $\overline{RTS}$ function	RW
TXEPT	Transmit Register Empty Flag	0: Data in the transmit register (during transmission) 1: No data in the transmit register (transmission is completed)	RO
CRD	$\overline{CTS}$/$\overline{RTS}$ Disable Bit	0: Enables $\overline{CTS}$/$\overline{RTS}$ function 1: Enables $\overline{CTS}$/$\overline{RTS}$ function	RW
NCH	Data Output Select Bit(1)(4)	0: TXDi/SDAi and SCLi are ports for the CMOS output 1: TXDi/SDAi and SCLi are ports for the N-channel open drain output	RW
CKPOL	CLK Polarity Select Bit	0: Data is transmitted on the falling edge of the transfer clock and data is received on the rising edge 1: Data is transmitted on the rising edge of the transfer clock and data is received on the falling edge	RW
UFORM	Transfer Format Select Bit(3)	0 : LSB first 1 : MSB first	RW

NOTES:
1. P70/TXD2 and P71/SCL2 are ports for the N-channel open drain output, but not for the CMOS output.
2. The CNT3 to CNT0 bits in the TCSPR register select no division (n = 0) or divide-by-2n (n = 1 to 15).
3. The UFORM bit setting is enabled when the SMD2 to SMD0 bits in the UiMR register are set to "0012" (clock synchronous serial I/O mode) or "1012" (UART mode, 8-bit transfer data).
   Set the UFORM bit to "1" when setting the SMD2 to SMD0 bits to "0102" (I^2C mode), or to "0" when setting them to "1002" (UART mode, 7-bit transfer data) or "1102" (UART mode, 9-bit transfer data).
4. This bit is reserved in UART5 and UART6. Set to "0".

Figure 17.7 U0C0 to U6C0 Registers