To our customers,

Old Company Name in Catalogs and Other Documents

    On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU			Document No.	TN-SH7-A542A/E	Rev.	1.0
Title	Limitation for use of SH7615/SH7616 internal Serial Communication Interface with FIFO.			Information Category	Technical Notification		
Applicable Product	HD6417615 HD6417616	Lot No.		Reference Document	SH7615 Hardware manual ADE-602-198 Rev.1.0 SH7616 Hardware manual ADE-602-243 Rev.1.0		
		ALL					

The SH7615/SH7616 has the following usage notice.

There is a limitation for use of Serial Communication Interface with FIFO (SCIF) in SH7615/SH7616, and their countermeasures are shown below.

<Phenomenon>

When SCIF initialization of SH7615 and SH7616 is executed more than twice, RXI request may be set despite the fact that there is no receipt of data.

<Condition>

Figure 1. shows an example of SCIF initialization flowchart with 2nd initialization.

RXI request may be set at the trigger(RTRG1-0) setting 2) of 2nd initialization when you try to reset the value of the Receive FIFO Data Number Trigger(RTRG1-0) setting 1) of 1st initialization.

<Countermeasures>

Please apply any of the following countermeasures, if the write-access occurs at the Receive FIFO Data Number Trigger setting 2) of 2nd initialization.

(1)   Read out SCFCR and write the same value with the Receive FIFO Data Number Trigger(RTRG1-0).

(2)   Set Receive Interrupt Enable (RIE) bit to "0" in SCSCR before changing the value of the Receive FIFO Data Number Trigger(RTRG1-0). Mask the RXI request. After writing the SCFCR, clear the interrupt request to Receive Data Register Full (RDF). Set Receive Interrupt Enable (RIE) bit to "1" in SCSCR to terminate the mask-setting.

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| Initialization |
| Clear TE and RE bits to 0 in SCSCR |
| Set TFRST and RFRST bits to 1 in SCFCR | → Reset the transmit/receive data resister
| Set CKE1 and CKE0 bits in SCSCR (leaving TE and RE bits cleared to 0) |
| Set tramsmit/receive format in SCSMR |
| Set value in SCBRR |

Wait

1-bit interval elapsed?   No

Yes

| Set RTRG1-0 and TTRG1-0 bits in SCFCR, and clear TFRST and RFRST bits to 0 | → 1) Trigger setting / Set the transmit/receive FIFO data count

| Set TE or RE bit to 1 in SCSCR, and set RIE,TIE and MPIE bits |

1st initialization

| Clear TE and RE bits to 0 in SCSCR |
| Set TFRST and RFRST bits to 1 in SCFCR | → 2) Trigger setting / RXI request may be set when the value of the receive FIFO data count has been changed from 1st initialization.
| Set CKE1 and CKE0 bits in SCSCR (leaving TE and RE bits cleared to 0) |
| Set tramsmit/receive format in SCSMR |
| Set value in SCBRR |

Wait

1-bit interval elapsed?   No

Yes

| Set RTRG1-0 and TTRG1-0 bits in SCFCR, and clear TFRST and RFRST bits to 0 |

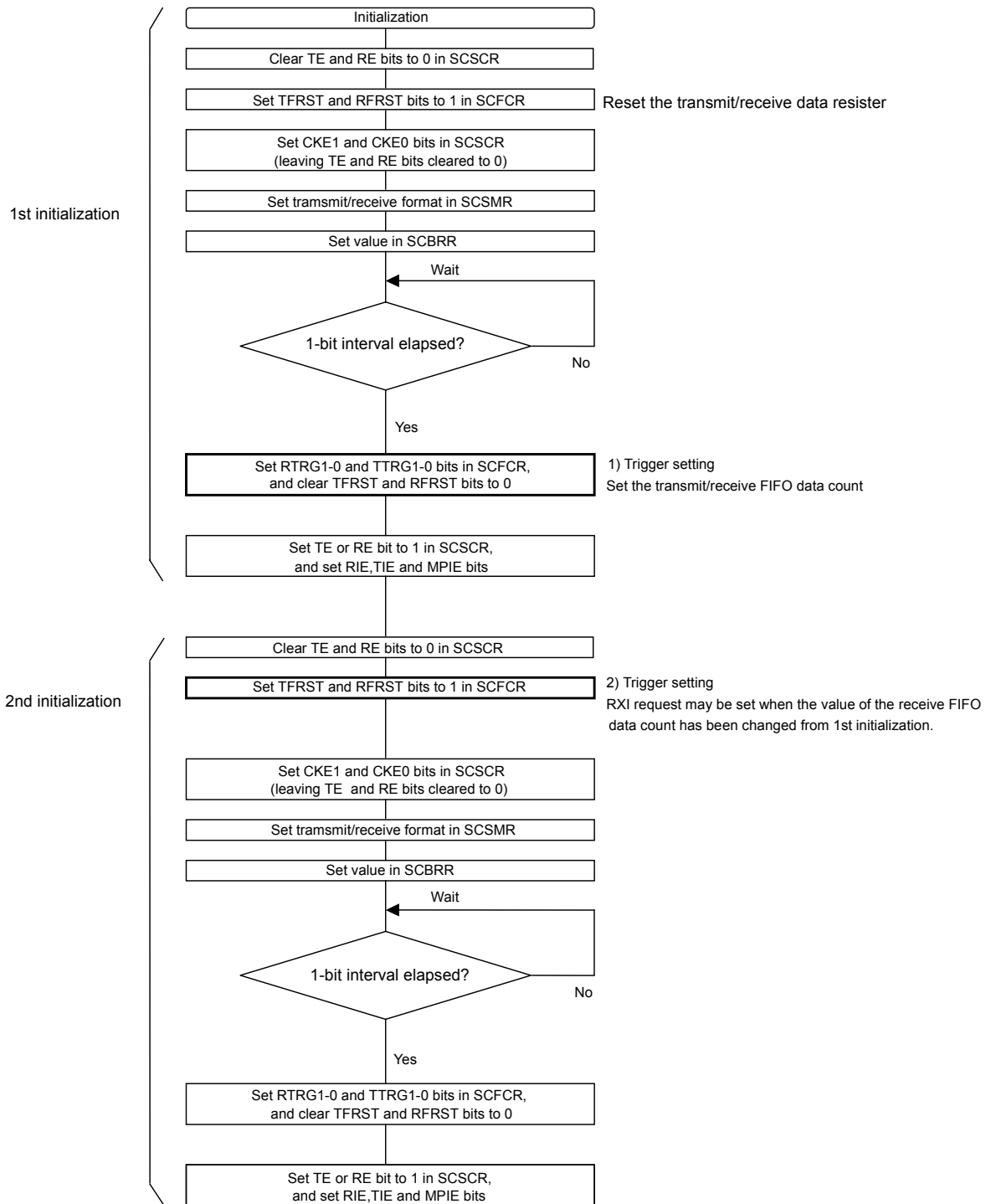| Set TE or RE bit to 1 in SCSCR, and set RIE,TIE and MPIE bits |

2nd initialization

Figure 1.   Example of SCIF initialization flowchart

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