To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A753A/E	Rev.	1.00
Title	The limitation of the output clock frequency for the PLL circuit		Information Category	Technical Notification		
Applicable Product	SH7730 group	Lot No. All	Reference Document	SH7730 Group Hardware Manual (REJ09B0359)		

About the output clock frequency of the PLL circuit(*) described in the SH7730 Group Hardware Manual (Figure 13.1 Block Diagram of CPG), we would like to inform you of the notification below.

[Limitation]

The range of the output clock frequency for the PLL circuit is as follows.

Please use the STC[4:0] bit in Frequency Control Register (FRQCR.STC) to become it within the following ranges.

266 MHz version: 75 MHz to 266.67 MHz

200 MHz version: 75 MHz to 200 MHz

(*)

As described In Figure 13.1 Block Diagram of CPG, the input clock from the EXTAL pin or

the output clock from Crystal oscillation circuit is the input clock of PLL circuit.

The PLL circuit multiplies the input clock frequency by the ratio of ×2 to ×16 and outputs the multiplied clock frequency.

The output clock frequency of the PLL circuit means the multiplied clock frequency.