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Old Company Name in Catalogs and Other Documents

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HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	4th January, 1999	No.	TN-SH7-117 A /E

THEME	The limitation of exception handling routine description

CLASSIFICATION	☐ Spec. change ■ Limitation on Use ☐ Supplement of Documents

PRODUCT NAME	HD6417091BP200, HD6417091RBP200, HD6417750BP200, HD6417750F167, HD6417750VF128

REFERENCE DOCUMENTS	SH7750 Hardware manual	Effective Date eternity
		From

1. Abstract

First instruction at the entry of exception handling routine may have mulfunction.
The conditions are following.
(1) PC-relative branch instruction located at the address of VBR+H'100,
    VBR+H'400 and VBR+H'600.
(2) PC-relative branch instruction located at the address indicated by DBR.

Above (1) or (2) cases, location such a PC-relative branch instruction may have
mulfunction.

Example of limitation

(*1)BSR,BT,BF,BT/S and BF/S are applied, too.

2. Limitation

- Do not use BRA,BSR,BT,BF,BT/S or BF/S instruction as the exception handling routine at the address
  VBR+H'100, VBR+H'400, VBR+H'600.
- Additionally, when utilizing the user debug support function(*1) setting the UBDE bit of the BRCR register to 1, do not put BRA,BSR,BT,BF,BT/S or BF/S instruction to the address indicated by DBR.
  (*1) Please refer to Section 20.4 in SH-4 Hardware manual.

3. Phenomenon

When exception/interrupt occurs, and branch to the exception handling routine indicated by VBR+offset or DBR is made with,
(a) the instruction at the entry of the handler hitting the instruction-cache, and,
(b) the above (a) instruction being BRA,BSR,BT,BF,BT/S or BF/S,
the branch target address of (1b) instruction is incorrect.

Incorrect branch address is depend on a instruction code next to the entry of exception handling routine, and it can calculate following expression.

```
OP:    Instruction code next to entry of exception handling routine.
IADR: Entry address of exception handling routine.
BA:    Incorrect branch address.

unsigned int low,mid,high,OP,IADR,BA;
low = OP & 0x000000FF;
mid = (OP & 0x00002000) ? (OP & 0x00000F00) :
         ((OP & 0x00000080) ? 0x00000F00 : 0x00000000);
high =(mid & 0x00000800) ? 0xFFFFF000 : 0x00000000;
BA = IADR + 6+ ((high | mid | low) <<1);
```