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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0109A/E	Rev.	1.00
Title	Limitation of D-Cache enablement		Information Category	Technical Notification		
Applicable Product	RA8M1 Group, RA8D1 Group, RA8T1 Group	Lot No. All	Reference Document	Renesas RA8M1 Group User's Manual: Hardware Rev.1.10 Renesas RA8D1 Group User's Manual: Hardware Rev.1.10 Renesas RA8T1 Group User's Manual: Hardware Rev.1.10		

Arm Limited has notified Errata ID3175626 and ID3190818 in Cortex-M85 AT640 and Cortex-M85 with FPU AT641 Software Developer Errata Notice.

The required countermeasure is described below.

- Procedure1 is required if enabling D-Cache. This is a countermeasure for ID3190818.
- Procedure2 is required if enabling D-Cache but【Writeback setting acceptable condition】is not satisfied. This is a countermeasure for ID3175626.

Refer ARM Limited references for the actual register setting method.

【Procedure1】

1) Set ACTLR [16] to 1.(*1)
2) Set Configuration and Control Register to enable D-Cache.

【Procedure2】

1) Set MSCR.FORCEWT=1.
2) Set Configuration and Control Register to enable D-Cache.
   In this case, all cacheable memory becomes Write-Through attribute.

Note1: Secure access is required to set ACTLR [16].

【Write-Back setting acceptable condition】

If the below conditions (a, b and c) are all met, setting Write-Back attribute is acceptable. No need to set MSCR.FORCEWT=1, as mentioned above in Procedure2.

a. CPU does not **write** any data to either Standby SRAM, CSC/SDRAM or OSPI.
b. During setting Write-Back attribution If CPU **access** to SRAM0, either "DMAC/DTC"," EDMAC", "GLCDC", "DRW" or "MIPI" does not **read** any data from SRAM0.
c. During setting Write-Back attribution If CPU **access** to SRAM1, either "DMAC/DTC"," EDMAC", "GLCDC", "DRW" or "MIPI" does not **read** any data from SRAM1.

Note: "GLCDC", "DRW" and "MIPI" exist in RA8D1 Group only.

References

Arm® v8-M Architecture Reference Manual

ARM Limited, Document type: Architecture Document

D1.2.9 CCR, Configuration and Control Register

D1.2.164 MAIR_ATTR, Memory Attribute Indirection Register Attributes

D1.2.165 MMFAR, MemManage Fault Address Register

D1.2.166 MMFSR, MemManage Fault Status Register

D1.2.167 MPU_CTRL, MPU Control Register

D1.2.168 MPU_MAIR0, MPU Memory Attribute Indirection Register 0

D1.2.169 MPU_MAIR1, MPU Memory Attribute Indirection Register 1

D1.2.170 MPU_RBAR, MPU Region Base Address Register

D1.2.171 MPU_RBAR_An, MPU Region Base Address Register Alias, n = 1 – 3

D1.2.172 MPU_RLAR, MPU Region Limit Address Register

D1.2.173 MPU_RLAR_An, MPU Region Limit Address Register Alias, n = 1 – 3

D1.2.174 MPU_RNR, MPU Region Number Register

D1.2.175 MPU_TYPE, MPU Type Register

D1.2.1 ACTLR, Auxiliary Control Register

Arm® Cortex®-M85 Processor

ARM limited, Document type: Technical Reference Manual

5.9 ACTLR, Auxiliary Control Register

5.14 MSCR, Memory System Control Register

Cortex-M85 AT640 and Cortex-M85 with FPU AT641

ARM Limited, Document type: Software Developer Errata Notice

ID: 3175626

ID: 3190818