Date: Dec. 14, 2016

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A016A/E	Rev.	1.00
Title	Limitation of changing PLL0 multiplication ratio for CPG of RZ/G Series		Information Category	Technical Notification		
Applicable Product	RZ/G Series, RZ/G1H	Lot No. All lots	Reference Document	RZ/G Series User's Manual: Hardware Rev.1.00		

This technical update describes the limitation of the RZ/G1H.

[Summary]

Please follow the procedure defined in this document when changing PLL0 multiplication ratio.

[Products]

RZ/G1H

[Note]

This is a limitation for the RZ/G1H.

[Limitation]

When changing PLL0 multiplication ratio, please follow the procedure defined in the [Description].

[Description]

1. Set ZFC[4:0] (bit 12-8) and bit 4-0 (Reserved bits) in FRQCRC to B'1 1111 respectively.
   Don't change the other bits (Read-modify-write).
2. Set KICK (bit 31) in FRQCRB to 1.
   Don't change the other bits (Read-modify-write).
3. Read KICK in FRQCRB and confirm that the bit is cleared to 0.
   Read FRQCRB repeatedly until 0 can be read from KICK in FRQCRB.
4. Set STC[6:0] (bit 30-24) in PLL0CR to the desired value.
   Don't change the other bits (Read-modify-write).
5. Read and confirm that PLL0ST (bit 8) in PLLECR is equal to 1.
   Count the number that 1 can be read from the bit.
   When the number reaches to ten, this operation for waiting can be finished. Go to the next step.
6. Set ZFC[4:0] (bit 12-8) in FRQCRC to the desired value (for example, B'0 0000 for x 32/32) and set bit 4-0 in FRQCRC to B'0 0000.
   Don't change the other bits (Read-modify-write).
7. Set KICK (bit 31) in FRQCRB to 1.
   Don't change the other bits (Read-modify-write).

Note: The frequency of not only Zϕ but also Z2ϕ is decreased during this procedure.

Finally, the description above should be added as new section, 7.8 Usage Notes in “7.CPG” of RZ/G Series User's Manual.

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