Microcomputer Technical Information

CP(K), O

IE-V850E-MC-A In-Circuit Emulator for V850E/MA1, V850E/MA2, Nx85E Cores Upgrade		Document No.	SBG-DT-03-0019-E		1/1
		Date issued	January 29, 2003		
		Issued by	Microcomputer Group 2nd Solutions Division Solutions Operations Unit NEC Electronics Corporation		
Related documents	IE-V850E-MC, IE-V850E-MC-A User's manual: U14487EJ1V0UM00	Document classification		Usage restriction	
			√	Upgrade	
				Document modification	
				Other notification	

1. Affected product

Product	Outline	Control code[Note]
IE-V850E-MC-A	In-circuit emulator for V850E/MA1, V850E/MA2, Nx85E cores	B, C, D, E, F

It is not necessary to upgrade a control code G product.

2. Details of upgrade

The bug described on the following page will be corrected (addition of specifications). After upgrading, the control code will be G.

See the document "IE-V850E-MC, IE-V850E-MC-A In-Circuit Emulators for V850E/MA1, V850E/MA2, V850E/IA1, V850E/IA2 Cores Usage Restrictions" (SBG-DT-03-0018-E) for details of restrictions.

3. Upgrade petition period

From February 3, 2003.

The upgrade described herein will be provided for free for a period of one year from the above date. After the free upgrade period expires, upgrade will be available for a fee. We therefore recommend that you take advantage of the free upgrade offer during the free upgrade period.

Note The "control code" is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.

List of Restrictions Modified in This Version (1/2)

No.		Restrictions	Control Code					
			B	C	D	E	F	G
Restrictions dependent on CPU functions	a-1	Interrupt aborts LD instruction immediately before JMP	×	×	√	√	√	√
	a-2	Restrictions on IRAM read access after start of interrupt servicing	×	×	√	√	√	√
	a-3	Fetching is abnormal immediately after writing to SCRn register	×	×	√	√	√	√
	a-4	Single, line, or single-step transfer of 2-cycle DMA	×	×	√	√	√	√
	a-5	Port C is not set in control mode immediately after starting in ROMless mode.	×	×	√	√	√	√
	a-6	Restrictions on ports DH and DL	×	×	√	√	√	√
	a-7	HLDAK output illegal due to conflict of self-refresh cycle and HOLDRQ in STOP mode	×	×	√	√	√	√
	a-8	Fetch/data access fails if hardware STOP is executed after CBR refresh of DRAM/SDRAM	×	×	√	√	√	√
	a-10	PFCCM register cannot be read.	×	×	√	√	√	√
	a-12	Restrictions on VSB bus signal	×	×	√	√	√	√
	a-14	Restrictions on memory controller (NB85E500) signal	×	×	√	√	√	√
	a-15	Restrictions on instruction cache	×	×	√	√	√	√
	a-16	Restriction on SDRAM access during bus hold	×	×	√	√	√	√
	a-17	Restriction on self-refresh cycle by SELFREF pin	×	×	√	√	√	√
	a-18	Restriction on flyby DMA transfer to EDO DRAM	×	×	√	√	√	√
	a-19	Restriction on EDO DRAM with idle state inserted	×	×	√	√	√	√
	a-20	Restriction on flyby DMA transfer	×	×	√	√	√	√
	a-21	Restriction on pin status in single-step mode 1 and ROMless modes 0 and 1	×	×	√	√	√	√
	a-22	When executing a CALLT/SWITCH instruction, LD/SLD instruction writeback is incorrect.	×	×	×	√	√	√
	a-24	Restriction on output of the _DMAAK signal	×	×	×	√	√	√
	a-25	Restriction on starting DMA by built-in peripheral I/O interrupt	×	×	×	√	√	√
	a-26	Restriction on EDO DRAM bus collision	×	×	×	√	√	√
	a-27	Restriction on the 2-way associative function of the instruction cache	×	×	×	√	√	√
	a-29	Restriction on reading the DCHC register when DMA 2-cycle transfer is complete	×	×	×	√	√	√
	a-30	Restriction on conflict between SDRAM initialization and SELFREF input	×	×	×	√	√	√
	a-31	Restriction on halfword writing to BSC, BCC, DWC0, and DWC1 registers	×	×	×	√	√	√
	a-32	Restriction on SDRAM write operation	×	×	×	√	√	√
	a-33	Restriction on DRAM fetch immediately after block DMA transfer from DRAM to internal RAM	×	×	√	√	√	√

×: Restriction is applicable √: Restriction has been corrected

List of Restrictions Modified in This Version (2/2)

No.		Restrictions	Control Code					
			B	C	D	E	F	G
Restrictions dependent on CPU functions	a-35	Restriction on SLD instruction	×	×	×	×	√	√
	a-36	I/O that cannot be used when using a VSB bus	×	×	×	×	√	√
	a-37	Restriction on instruction cache (3)	×	×	×	×	√	√
	a-39	Restriction caused by interrupt input during execution of bit manipulation instruction	×	×	×	×	√	√
	a-40	Restriction on hardware stop during bit manipulation instruction execution	×	×	×	×	√	√
	a-41	Restriction related to interruption of DMA transfer by external cause	×	×	×	×	√	√
	a-42	Restriction on SDCKE signal during bus hold	×	×	×	×	×	√
Restrictions on debug functions	b-1	Restriction on operating frequency	×	×	×	√	√	√
	b-3	Restriction on trace in case of mis-alignment (during read access only)	×	×	√	√	√	√
	b-4	Restrictions on trace data on execution of HALT or STOP instruction	×	×	√	√	√	√
	b-5	Bit manipulation instruction (set1, clr1, not1, tst1) access data is illegally traced by tracer.	×	×	√	√	√	√
	b-6	Events including data conditions by access of bit manipulation instruction cannot be detected.	×	×	√	√	√	√
	b-7	Restriction on HOLD status	×	×	√	√	√	√
	b-10	Restrictions on programmable I/O space	×	×	×	×	√	√
	b-15	Restriction on illegal guard break when IRAM size is 28KB	×	×	×	×	√	√
	b-16	Restriction on illegal trace when big endian is used	×	×	×	×	√	√
Other	c-1	Modification through quality improvement	None	Provided				

×: Restriction is applicable √: Restriction has been corrected