

CUSTOMER NOTIFICATION

SUD-DT-04-0094 (1/11)
March 5, 2004
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**IE-78K0K1-ET**  
**(Control Code: A, B, C)**

**Operating Precautions**

**Be sure to read this document before using the product.**

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## Notes on Using IE-78K0K1-ET

### 1. Product History

No.	Bugs and Changes/Additions to Specifications	Control Code <sup>Note</sup>		
		A	B	C
1	SFRs may not be able to be accessed when operating at a frequency of over 5 MHz and at 3.3 to 4.0 V	×	√	√
2	Transmit data cannot be written to the buffer RAM using the 3-wire serial interface with automatic transfer function (CSIA0) of the target device 78K0/KF1	×	√	√
3	The long-type emulation probe 80-pin package (NP-H80GC-TQ and NP-H80GK-TQ) cannot be used	×	√	√
4	An internal reset may not be generated by the watchdog timer	×	√	√
5	The integrated debugger may not start when it is restarted	×	×	√
6	78K0/Kx1+ has been added to supported devices [Addition of specification]	–	–	√
7	Some restrictions apply if Break (peripheral functions stopped) is specified as Peripheral Break in the Configuration dialog box of the integrated debugger ID78K0-NS	×	×	×

×: Restriction applies

√: Restriction does not apply or already corrected

–: Specification not supported

**Note** The “control code” is the second digit from the left in the 10-digit serial number in the warranty supplied with the in product you purchased (if it has not been upgraded). If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.

### 3. Details of Bugs and Additions to Specifications

No.1 SFRs may not be able to be accessed when operating at a frequency of over 5 MHz and at 3.3 to 4.0 V

[Description]

SFRs may not be able to be accessed when operating at the following frequency and voltage.

Voltage	Frequency
3.3 to 4.0 V	Over 5 MHz

[Workaround]

There is no workaround.

This restriction has been corrected in control code B.

No.2 Transmit data cannot be written to the buffer RAM using the 3-wire serial interface with automatic transfer function (CSIA0) of the target device 78K0/KF1

[Description]

When writing transmit data to the buffer RAM using the 3-wire serial interface with automatic transfer function (CSIA0) of the target device 78K0/KF1, data may not be written correctly depending on the instruction executed after the write instruction (see SBG-DT-0128-E for details).

[Workaround]

See [Workaround] (3) in SBG-DT-0128-E.

This restriction has been corrected in control code B.

No.3 The long-type emulation probe 80-pin package (NP-H80GC-TQ and NP-H80GK-TQ) cannot be used

[Description]

The long-type emulation probe 80-pin package (NP-H80GC-TQ and NP-H80GK-TQ) cannot be used.

[Workaround]

There is no workaround. This restriction has been corrected in control code B.

No.4 An internal reset may not be generated by the watchdog timer

[Description]

An internal reset may not be generated by the watchdog timer.

[Workaround]

There is no workaround. This restriction has been corrected in control code B.

No.5 The integrated debugger may not start when it is restarted

[Description]

The integrated debugger may not start after it is shut down and restarted.

[Workaround]

Be sure to disconnect the power supply to the IE-78K0K1-ET after the integrated debugger is shut down. This restriction has been corrected in control code C.

No.6 78K0/Kx1+ has been added to supported devices. [Addition of specification]

[Description]

The 78K0/Kx1+ are now supported in control code C, but restrictions apply.

See No.7 in **3. Restrictions** for details.

No.7 The watchdog timer operation may not stop and a reset signal may be generated when NONMSK is set for the mask option RINGMSK

[Description]

The watchdog timer operation does not stop even if NONMSK (Ring-OSC can be stopped by software) is set for the mask option RINGMSK and the HALT instruction is executed, as long as the operation clock to the watchdog timer does not stop. As a result, a reset signal is generated.

[Workaround]

There is no workaround. This restriction will be corrected in control code D or later.

### 3. Restrictions

No.1 The initial value of the SFR PCC differs between the target device and IE system.

[Description]

The initial value of the SFR PCC differs between the target device and IE system.

Target device: 00H IE system: 04H

[Workaround]

Set the initial value when the target device is started or reset.

No.2 The processing of the  $\overline{\text{RESET}}$  pin differs from that in the target device.

[Description]

The processing of the  $\overline{\text{RESET}}$  pin differs from that in the target device.

Target device: Without pull-up IE system: 4.7 k $\Omega$  pull-up in the IE system

[Workaround]

There is no workaround.

No.3 Do not use an accessing method that generates a wait request for the WDTM, ASIS0, ASIS6, ADM, ADS, PFM, PFT, and ADCR registers when operating with the subsystem clock and with the input clock stopped

[Description]

Do not use an accessing method that generates a wait request for the WDTM, ASIS0, ASIS6, ADM, ADS, PFM, PFT, and ADCR registers when operating with the subsystem clock and with the input clock stopped.

[Workaround]

LED2 (RETRY) that indicates the wait (retry) status stays lit in the IE system, the integrated debugger ID78K0-NS hangs up. Apply a reset by using either of the following methods to restore from the hang-up status.

- Reset applied from a circuit on the target device
- Internal reset by comparing the power supply voltage of the POC circuit and detection voltage
- Internal reset by comparing the power supply voltage of the low-voltage detector (LVI) and detection voltage
- Clock monitor reset by pressing emulation switch SW2 on the clock monitor

No.4 The values of the RESF, LVIM, and LVIS registers are initialized by applying a reset from the target system even if RESET is masked

[Description]

The values of the RESF, LVIM, and LVIS registers are initialized by applying a reset from the target system to the IE system even if RESET is masked in the Configuration dialog box of the integrated debugger ID78K0-NS. (The values of other registers are not initialized.)

[Workaround]

There is no workaround.

No.5 The values of the RESF, LVIM, and LVIS registers are not initialized by the CPU reset button of the integrated debugger ID78K0-NS.

[Description]

The values of the RESF, LVIM, and LVIS registers are not initialized by the CPU reset button of the integrated debugger ID78K0-NS.

[Workaround]

Initialization can be implemented using the following resets.

<RESF register>

- Reset applied from a circuit on the target device
- Internal reset by comparing the power supply voltage of the POC circuit and detection voltage

<LVIM and LVIS registers>

- Reset applied from a circuit on the target device
- Internal reset by comparing the power supply voltage of the POC circuit and detection voltage
- Clock monitor reset by pressing emulation switch SW2 on the clock monitor
- Reset applied from the watchdog timer

No.6 Some restrictions apply if Break (peripheral functions stopped) is specified as Peripheral Break in the Configuration dialog box of the integrated debugger ID78K0-NS

[Description]

(1) Prohibition of write

Do not write data to the TMC00, TMC01, WDTM, ADM, ADS, PFM, and PFT registers in the SFR window and Watch window and the buffer RAM area in the Memory window (there is no problem if data is written by the program.).

(2) Restriction on display

The value of the ADCR register in the SFR window and Watch window is illegal (there is no problem when Non Break is specified. In addition, there is no problem with the read value in the program.)

(3) Restriction on non-real-time execution

Writing to the TMC00, TMC01, WDTM, ADM, ADS, PFM, and PFT registers and the buffer RAM area may not be performed when a non-real-time execution (step-in, next over, or slow motion) is performed.

(4) Restriction on break immediately before/after write operation to I/O register that generates a wait

Writing to the TMC00, TMC01, WDTM, ADM, ADS, PFM, and PFT registers and the buffer RAM area may not be performed normally when a break is set immediately before/after the write operation.

[Workaround]

There is no workaround.

## No.7 Restrictions on using 78K0/Kx1+

## [Description]

- (1) Accessing the system control register (VSWC) is not possible. VSWC operates with the initial value 0H.
- (2) An operating voltage lower than 2.5 V is not supported.
  - The POC function of the device generates a POC reset when the voltage becomes  $2.1 \pm 0.1$  V, but the target voltage cannot be set to lower than 2.5 V in the IE-78K0K1-ET. Therefore, the POC reset cannot be emulated in the IE-78K0K1-ET.
  - A detection voltage (VLVI) of  $2.35 \pm 0.1$  V cannot be used for the LVI function. Use a detection voltage of  $2.6 \pm 0.1$  V or higher.
- (3) The self-programming function is not supported.
- (4) The boot swap function is not supported.
- (5) The maximum operating frequency of the device is 16 MHz, but the IE-78K0K1-ET does not support operation at a frequency higher than 12 MHz. Therefore, use the IE-78K0K1-ET with an operating frequency of 12 MHz or lower.
- (6) The option byte function is not supported. Set RINGOSC using the mask option of the debugger.

## [Workaround]

There is no workaround.

## 4. Cautions

### No.1 LED3 (POC RESET)

#### [Description]

LED3 (POC RESET) is lit during the reset shown below. Do not perform a break when LED3 is lit; otherwise the integrated debugger ID78K0-NS will hang up.

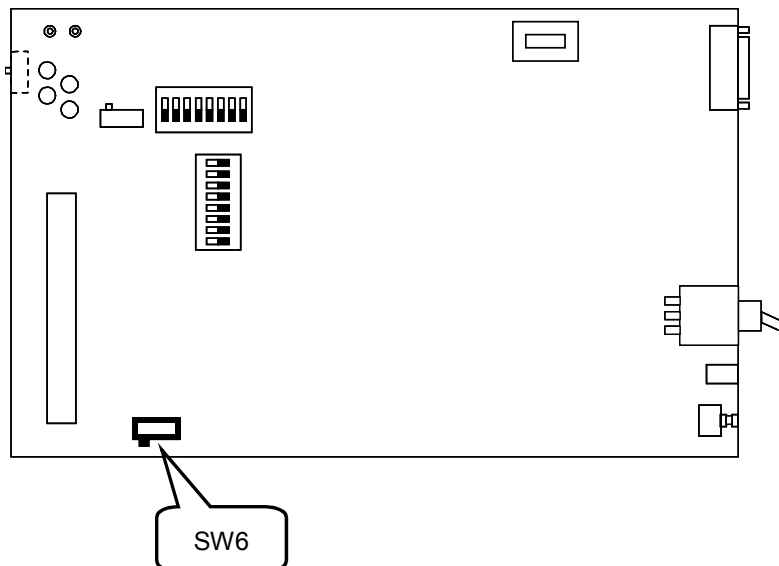
- Internal reset by comparing the power supply voltage and detection voltage of the POC circuit

### No.2 SW6

#### [Description]

Use SW6 in the default setting (3-side). (SW6 is a switch used for maintenance.)

### Package Drawing of Emulation board (S-780148 Board)



### No.3 Product information

#### [Description]

NEC Electronics' Microcomputer website ([http://www.necel.com/micro/index\\_e.html](http://www.necel.com/micro/index_e.html)) provides product information, FAQs on development tools, the latest development tools, user's manuals, and a device file download service, etc.



## 5. Difference Manual

This section explains changes from control code C and differences from the user's manual.

Target manual: IE-78K0K1-ET In-Circuit Emulator Preliminary User's Manual (document number: U16604E)

(1) Addition of 78K0/KB1+, 78K0/KC1+, 78K0/KD1+, 78K0/KE1+, 78K0/KF1+ to target devices

[Location] Cover, pages 3, 6, 8, 10, and 17

(2) Change of supported low-voltage range from "2.7 V to 5.5 V" to "2.5 V to 5.5 V"

[Location] Page 10

(3) Deletion of SW8

[Location] Pages 13, 14, and 31

(4) Change of description of PD78F0148 to PD78F0148H in figures

[Location] Pages 23 and 29

(5) Change of description "2.0 MHz to 10.0 MHz" to "2.0 MHz to 12.0 MHz"

[Location] Page 24

(6) Addition of multiplication circuit setting

[Location] Page 32

Main System Clock Frequency	SW2	SW3
10 MHz to 12 MHz	1, 6 ON (Other: OFF)	4, 6 ON (Other: OFF)

(7) Deletion of **3.10**

[Location] Page 33

(8) Addition of 78K0/KB1+ to target devices

[Location] Page 35

(9) Addition of 78K0/KC1+ to target devices

[Location] Page 39

(10) Addition of 78K0/KD1+ to target devices

[Location] Page 43

(11) Addition of 78K0/KE1+ to target devices

[Location] Page 47

(12) Addition of 78K0/KF1+ to target devices

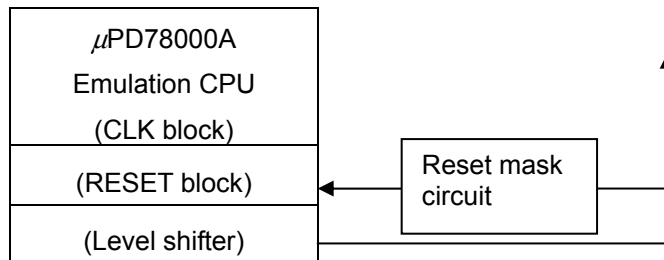
[Location] Page 51

(13) Change of emulation CPU from  $\mu$ PD78F0148 to  $\mu$ PD78F0148H

[Location] Pages 35 to 37, 39 to 41, 43 to 45, 47 to 49, and 51 to 53

(14) Addition of reset mask circuit

[Location] Pages 37, 41, 45, 49, and 53



(15) Addition of case for 78K0/Kx1+ to mask option settings

[Location] Page 33

(a) When target device is 78K0/Kx1

- Ring-OSC
- POC ON/OFF and detection voltage 2.85 V, 3.5 V
- P60 to P63 (these ports are not provided in the  $\mu$ PD780101, 780102, 780103, and 78F0103)

Set the mask options in the integrated debugger.

Open the mask option window from [Option] → [Mask Option] and set the mask options.

Refer to the ID78K0-NS Ver.2.52 Integrated Debugger Operation (U16488E) for details.

• RINGMSK	NONMSK	Ring-OSC stop by software enabled Watchdog timer stop enabled
	MSK	Ring-OSC stop by software disabled Watchdog timer stop disabled
• POC	ON	POC function ON
	OFF	POC function OFF
• POCV	2.85 V	POC detection voltage 2.85 V
	3.5 V	POC detection voltage 3.5 V
• P60 to P63	ON	Pulled up by the mask option resistor
	OFF	No mask option resistor

(b) When target device is 78K0/Kx1+

- Ring-OSC

Set the mask options in the integrated debugger.

Open the mask option window from [Option] → [Mask Option] and set the mask options.

Refer to the ID78K0-NS Ver.2.52 Integrated Debugger Operation (U16488E) for details.

- |           |        |  |
|-----------|--------|--|
| • RINGMSK | NONMSK | Ring-OSC stop by software enabled<br>Watchdog timer stop enabled   |
|           | MSK    | Ring-OSC stop by software disabled<br>Watchdog timer stop disabled |

**Caution** When emulating the 78K0/Kx1+, “78K0Kx1plus” is displayed in the mask option window, but this does not need to be set.