CUSTOMER NOTIFICATION

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IE-78K0-NS
(Control Code: N)
Operating Precautions

Be sure to read this document before using the product.

Notes on Using IE-78K0-NS and IE-78K0-NS-A

1. Bug Description

No.	Bugs and Changes/Additions to Specifications
1	External memory mapping bug
2	Cannot emulate flash memory self-write when using 780988.
3	FIP pin mask option function (VLOAD, VSS0 pull down) cannot be set correctly mask option bug when using D780232.
4	Debugger does not start up correctly with devices using IE-78K0-NS-P04 (D780818/0828).
5	If a reset command occurs immediately after single step execution, the value of the PC is incorrect.
6	Not compatible with performance board (IE-78K0-NS-PA)
7	Instruction fetch from external memory is not possible when using external expansion memory emulation with IE-78K0-NS and D7881 mounted on emulation board. (Normal memory access works fine.) Target devices and combinations affected are as follows. • IE-78K0-NS-P01 + IE-780988-NS-EM4: D78098x • IE-78K0-NS-P01 + IE-780066-NS-EM4: D78006x
8	Count value of execution time counter becomes incorrect if an overflow occurs when connected to the IE-78K0-NS-PA.
9	An SFR illegal break occurs if an attempt to rewrite the IXS register is made in a program.
10	Flash self-write cannot be emulated when using the ID78K0-NS V1.xx (16-bit ID)
11	Fan not mounted. When mounting the IE-78K0-NS-PA + IE-78K0-NS-P04, a fan is required for cooling.
12	When executing "Go-Non Break", the interval timer in the timer window cannot be stopped when the tracer is stopped.
13	The debugger will not start when connected to the IE-780835-NS-EM4.
14	If a break occurs when a time out is detected in the timer window or an external sense event, the wrong break name is displayed.
15	If the memory contents are changed during a break when the real-time RAM monitor is specified for the internal high-speed RAM space, when execution continues, the memory data displayed may be undefined. (If a data write is performed in the program, this will be executed correctly.)
16	If a time out is detected in the timer window when executing "Go-Non Break" when connected to the IE-78K0-NS-PA, neither a break nor external sense event is issued.
17	If any section event-related setting is changed while executing "Go-Non Break" when connected to the IE-78K0-NS-PA, trace start and end may not work correctly. (Change the settings after issuing a break)
18	The external memory expansion mode cannot be used when connected to the IE-780988-NS-EM4. (The pin remains a port.)
19	If data in a space for which real-time RAM monitoring is specified is being displayed in the memory window or variable window, the data displayed in the memory window or variable window is not updated after a break. * Reload the window (close the window, then open it again.)

No.	Bugs and Changes/Additions to Specifications
20	If a forced break occurs during step execution (Step, Next, Slowmotion), the debugger hangs up.
21	If execution is interrupted by STOP (forced break) immediately after executing "Go-Non Break" with the snap shot setting when connected to the IE-78K0-NS-PA, the snap data is not displayed in subsequent trace data. Remedy: When using snap shot execute “Go-break”.
22	The snap data in the trace data is displayed in the wrong order if a 16-bit pair register is specified in the snap shot specification when connected to the IE-78K0-NS-PA. (The lower 8 bits are shown in place of the higher 8 bits and vice versa.) Example: If AX is specified, the values of the A and X registers are reversed in the trace data. Remedy: Specify as 8-bit registers.
23	Step execution can result in "Send time out" or "Receive time out." • If data in a space for which real-time RAM monitoring is specified is being displayed in the memory window or variable window, and step execution is used after a break, this may result in "Send time out" or "Receive time out."
24	If many debugger windows are open the speed of step execution, etc., will become slower.
25	One extra snap trace frame may appear.
26	Incorrect data may be written when the RAM sampler is executed.
27	If step execution is used, followed by a trace clear, and then step execution is resumed, the trace data becomes incorrect.
28	If a forced break is applied during RUN, the debugger may hang up.
29	If more than one software break point is specified, then RUN is executed, and then more software break points are specified, only the last break point specified is valid.
30	The break operation does not work correctly in the flash self-programming mode.
31	If "External clock" is selected in the configuration window of the debugger, and the OK button is pressed when no target is connected (no external clock is being input), the debugger hangs up. Workaround: Select "Internal clock" when no target is connected.
32	A break factor will become an event break after step is executed if an event break is set for an inactive address.
33	Hang up may occur if a break is applied while the user program is executing.
34	When connected to the IE-78K0-NS-P04, it may not be possible to perform read/write to the CAN RAM area correctly.
35	When connected to the IE-780988-NS-EM4, output by the pins TO70 to TO75 does not stop even if watchdog timer mode 1 is set (WDTM3 = 0, WDTM4 = 1) and a watchdog timer interrupt (INTWDT) is generated. To avoid this bug, it is necessary to upgrade DF780988 to V1.02 or later.
36	If PM4 = 0h is not set when connected to an emulation board with the external expansion memory (IE-780034-NS-EM1 or IE-780078-NS-EM1), read and write operations to the external expansion memory area xx24h may not be performed correctly.

No.	Bugs and Changes/Additions to Specifications
37	The debugger hangs up if an attempt is made to perform any of the following operations with the subsystem clock when connected to the IE-780958-NS-EM4. To avoid this bug, it is necessary to upgrade DF780958. Consult NEC for details of the corrected version. (1) Generate an event break after executing PCC = 10H in user program. (2) Generate a forced break after executing PCC = 10H in user program. (3) Execute RUN after setting PCC = 10H on SFR window.
38	A high-level signal is output from ports 50 to 52 while the power of the emulator is on and the debugger has not been started.
39	The characteristics of the operation clock used in the in-circuit emulator have been improved (addition of specification).
40	A specification change in the following devices (high-speed specification: 12 MHz operation) has been supported. (Addition of specification) Target devices: μPD780024A, 780024AY, 780034A, 780034AY Subseries μPD780078, 780078Y Subseries μPD780988 Subseries Target emulation board: IE-780034-NS-EM1 (control code J or later) IE-780078-NS-EM1 (control code D or later) IE-780988-NS-EM4 (control code B or later) + IE-78K0-NS-P01 (control code D or later)

2. Restrictions

No.	Description	IE-78K0-NS	IE-78K0-NS-A
1	If a setting which causes DMM or snap shot to occur is made during execution time measurement with a zone specified, the measured execution time is greater than the actual value. Workaround: Do not specify DMM or snap shot during execution time measurement.	√	√
2	If a DMM or snap shot event is specified with section trace specified, the trace data may not be correctly displayed. Workaround: When executing section trace, do not specify DMM or a snap shot event. When specifying DMM or a snap shot event, do not specify section trace.	√	√
3	If 00 is written by the program or by DMM at an address where a software break has been set, the data when the break occurs returns to the value before the program was executed. Workaround: Do not set a software break at a memory address that is written to during program execution.	√	√
4	If “Break” is selected for the peripheral break of the debugger and the sub-clock is used as the main-clock, the operation of the peripheral emulation chip will not stop, even if a break is applied.	√	√
5	Flash self-mode related restrictions (1) Of the four access events in flash self-mode, only one may be consumed. Consequently, users should release the above events on the debugger side and then set a maximum of three events each when switching to flash self-mode. (2) The system may enter restart processing once a break occurs in flash self-mode that is not the result of break settings. This will cause some of the time measurement results and some trace data and path count to become invalid.	√	√
6	During subclock operation, if the main clock is stopped as is shown in the following program and the clock is switched from the subclock to the main clock, which is monitored after switching is complete, the clock is switched normally in the IE system, but a program loop occurs in the target device (equipped with a subclock). XXX: SET1 PCC.7H CLR1 PCC.4H BT PCC.5H,$XXX	√	√

√: Applicable, –: Not applicable (except for control code A to C)

No.	Description	IE-78K0-NS	IE-78K0-NS-A
7	According to specification change in the following devices (high-speed specification: 12 MHz operation), the trace function used at a frequency of 10 MHz or higher may not operate correctly. (Other emulation functions are not affected.) Target devices: μPD780024A, 780024AY, 780034A, 780034AY Subseries μPD780078, 780078Y Subseries μPD780988 Subseries Target emulation boards: IE-780034-NS-EM1 IE-780078-NS-EM1 IE-780988-NS-EM4 + IE-78K0-NS-P01	–	√

√: Applicable, –: Not applicable (except for control code A to C)

3. Product History

No.	Control Code [Note]																		
	IE-78K0-NS													IE-78K0-NS-A					
	A	B	C	D	E	F	G	H	J	K	L	M	N	A	B	C	D	E	F
1	√	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
2	√	√	–	–	–	√	–	–	–	–	–	–	–	–	–	–	–	–	–
3	√	√	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
4	√	√	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
5	√	√	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
6	√	√	√	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
7	√	√	√	√	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
8	√	√	√	√	√	–	–	–	–	–	–	–	–	–	–	–	–	–	–
9	–	–	–	–	√	–	–	–	–	–	–	–	–	–	–	–	–	–	–
10	–	–	–	–	√	√	–	–	–	–	–	–	–	–	–	–	–	–	–
11	√	√	√	√	√	√	–	–	–	–	–	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–	–	–	–	–	–	√	–	–	–	–	–
13	–	–	–	–	–	–	–	–	–	–	–	–	–	√	–	–	–	–	–
14	–	–	–	–	–	–	–	–	–	–	–	–	–	√	–	–	–	–	–
15	–	–	–	√	√	√	√	–	–	–	–	–	–	√	–	–	–	–	–
16	–	–	–	√	√	√	√	–	–	–	–	–	–	√	–	–	–	–	–
17	–	–	–	√	√	√	√	–	–	–	–	–	–	√	–	–	–	–	–
18	–	–	–	√	√	√	√	–	–	–	–	–	–	√	–	–	–	–	–
19	–	–	–	√	√	√	√	–	–	–	–	–	–	√	–	–	–	–	–
20	–	–	–	√	√	√	√	–	–	–	–	–	–	√	–	–	–	–	–
21	–	–	–	√	√	√	√	–	–	–	–	–	–	√	–	–	–	–	–
22	–	–	–	√	√	√	√	–	–	–	–	–	–	√	–	–	–	–	–
23	–	–	–	√	√	√	√	–	–	–	–	–	–	√	–	–	–	–	–
24	–	–	–	√	√	√	√	–	–	–	–	–	–	√	–	–	–	–	–
25	–	–	–	–	–	–	–	–	–	–	–	–	–	√	–	–	–	–	–
26	√	√	√	√	√	√	√	√	–	–	–	–	–	√	–	–	–	–	–
27	√	√	√	√	√	√	√	√	–	–	–	–	–	√	–	–	–	–	–
28	–	–	–	–	–	–	–	√	–	–	–	–	–	√	–	–	–	–	–
29	–	–	–	√	√	√	√	√	–	–	–	–	–	√	–	–	–	–	–
30	–	–	–	√	√	√	√	√	–	–	–	–	–	√	–	–	–	–	–
31	–	–	–	√	√	√	√	√	√	–	–	–	–	√	√	–	–	–	–
32	–	–	–	√	√	√	√	√	√	–	–	–	–	√	√	–	–	–	–
33	–	–	–	√	√	√	√	√	√	–	–	–	–	√	√	–	–	–	–
34	√	√	√	√	√	√	√	√	√	√	–	–	–	√	√	√	–	–	–
35	√	√	√	√	√	√	√	√	√	√	–	–	–	√	√	√	√	–	–
36	√	√	√	√	√	√	√	√	√	√	–	–	–	√	√	√	√	–	–
37	√	√	√	√	√	√	√	√	√	√	–	–	–	√	√	√	√	–	–
38	√	√	√	√	√	√	√	√	√	√	√	–	–	√	√	√	√	√	–
39	√	√	√	√	√	√	√	√	√	√	√	–	–	√	√	√	√	√	–
40	√	√	√	√	√	√	√	√	√	√	√	√	–	√	√	√	√	√	√

√: Applicable or no additional specification, –: Not applicable or additional specification

Note The “control code” is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.

In addition to control code M, products in which the 78K0 Executer is V2.7 are control code N products. The version of the 78K0 Executer is indicated in the [About…] window on the [Help] menu in the integrated debugger ID78K0-NS. Control code “I” is not available.