CUSTOMER NOTIFICATION

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IE-789882-NS-EM1

Preliminary User's Manual

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INTRODUCTION

Product Overview

The IE-789882-NS-EM1 is designed to be used with the IE-78K0S-NS or IE-78K0S-NS-A to debug the following target devices that belong to the 78K0S Series of 8-bit single-chip microcontrollers.

- μPD789882 Subseries: μPD78F9882, 789882

Target Readers

This manual is intended for engineers who will use the IE-789882-NS-EM1 with the IE-78K0S-NS or IE-78K0S-NS-A to perform system debugging.
Engineers who use this manual are expected to be thoroughly familiar with the target device's functions and use methods and to be knowledgeable about debugging.

Organization

When using the IE-789882-NS-EM1, refer to not only this manual (supplied with the IE-789882-NS-EM1) but also the manual that is supplied with the IE-78K0S-NS or IE-78K0S-NS-A.

IE-78K0S-NS
User's Manual

- Basic specifications
- System configuration
- External interface functions

IE-789882-NS-EM1
User's Manual

- General
- Part names
- Installation
- Differences between target devices and target interface circuits

IE-78K0S-NS-A
User's Manual

- Basic specifications
- System configuration
- External interface functions

Purpose

This manual's purpose is to explain various debugging functions that can be performed when using the IE-789882-NS-EM1.

Terminology The meanings of certain terms used in this manual are listed below.

Term	Meaning
Emulation device	This is a general term that refers to the device in the emulator that is used to emulate the target device. It includes the emulation CPU.
Emulation CPU	This is the CPU block in the emulator that is used to execute user-generated programs.
Target device	This is the device (a real chip) that is the target for emulation.
Target system	This includes the target program and the hardware provided by the user. When defined narrowly, it includes only the hardware.
IE system	This refers to the combination of the IE-78K0S-NS or IE-78K0S-NS-A and the IE-789882-NS-EM1.

Conventions

Data significance: Higher digits on the left and lower digits on the right

Note: Footnote for item marked with **Note** in the text

Caution: Information requiring particular attention

Remark: Supplementary information

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LIST OF TABLES

CHAPTER 1 GENERAL

The IE-789882-NS-EM1 is a development tool for efficient debugging of hardware or software when using one of the following target devices that belong to the 78K0S Series of 8-bit single-chip microcontrollers.

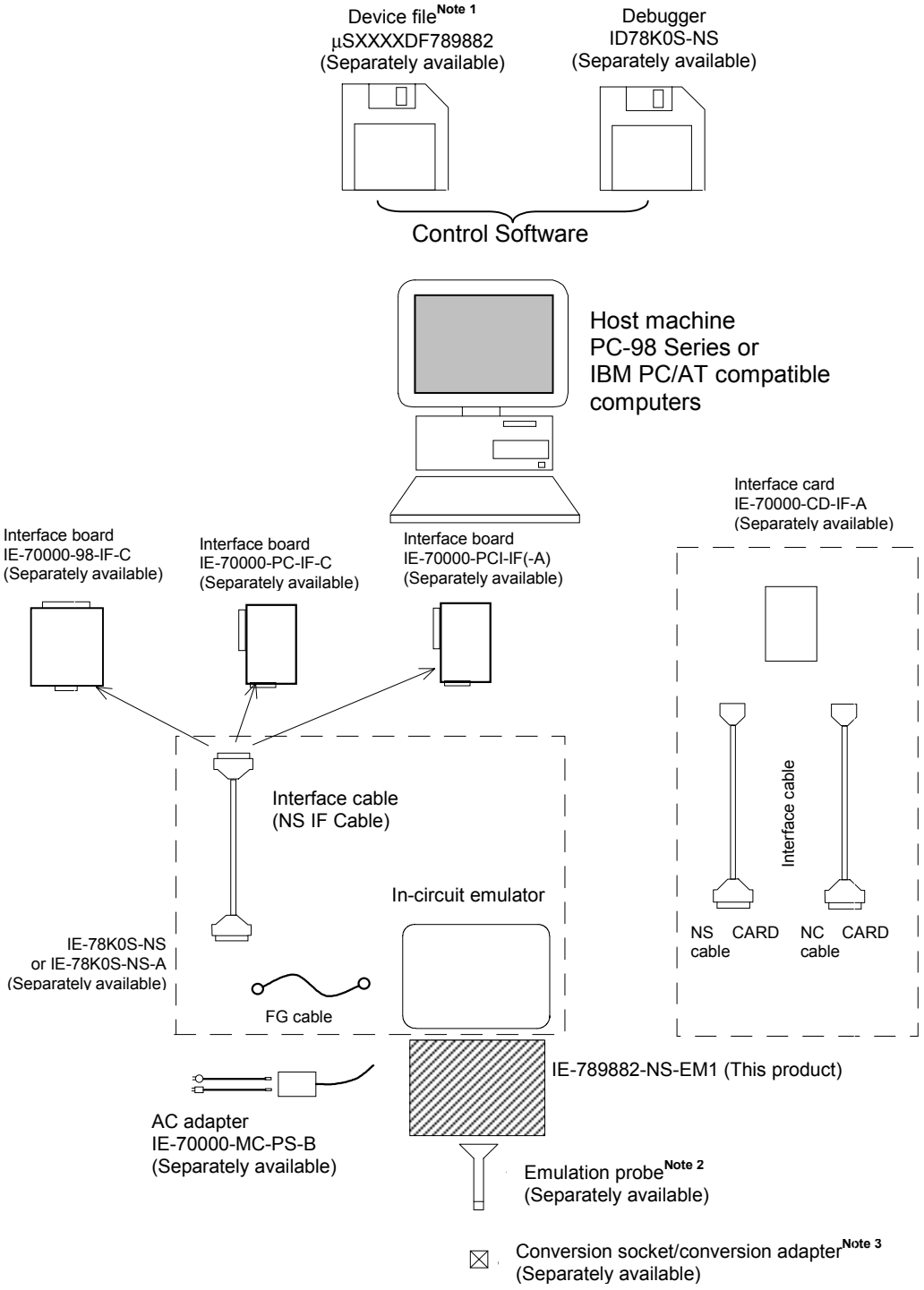
This chapter describes the IE-789882-NS-EM1 system configuration and basic specifications.

- Target device
  - μPD789882 Subseries

1.1 System Configuration

Figure 1-1 illustrates the IE-789882-NS-EM1 system configuration.

Figure 1-1. System Configuration



Notes 1. The device file is as follows.

μSXXXXDF789882: μPD789882 Subseries

2. The emulation probe is as follows.

NP-H64GB-TQ: 64-pin plastic QFP (probe length: 400 mm)

NP-H64GK-TQ: 64-pin plastic QFP (probe length: 400 mm)

NP-64GK: 64-pin plastic QFP (probe length: 200 mm)

NP-H64GB-TQ, NP-H64GK-TQ and NP-64GK are products of Naito Densei Machida Mfg. Co., Ltd.

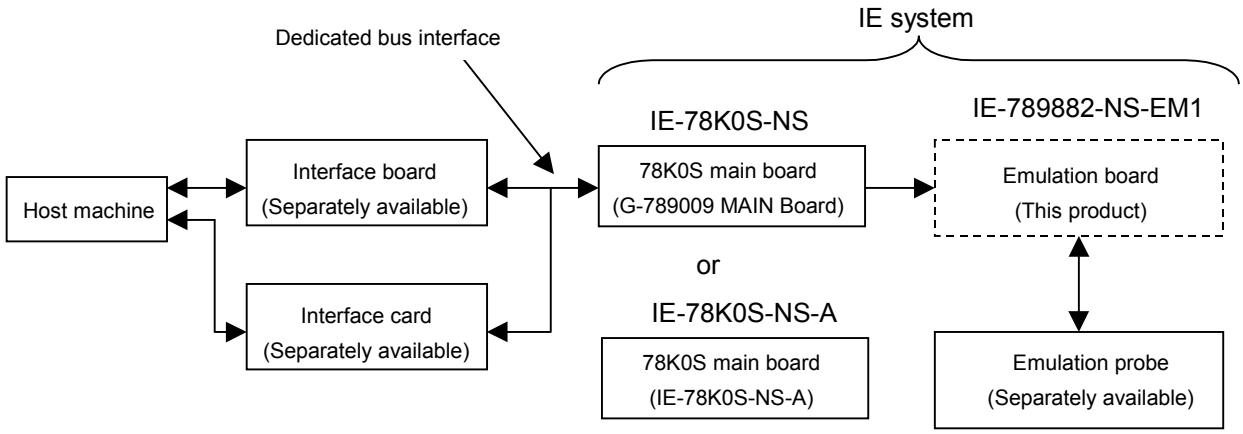
Contact: Naito Densei Machida Mfg. Co., Ltd. (TEL: 044-822-3813)

3. The conversion socket and conversion adapter are products of TOKYO ELETECH CORP.

1.2 Hardware Configuration

Figure 1-2 shows the IE-789882-NS-EM1's position in the basic hardware configuration.

Figure 1-2. Basic Hardware Configuration



1.3 Basic Specifications

The IE-789882-NS-EM1's basic specifications are listed in Table 1-1.

Table 1-1. Basic Specifications

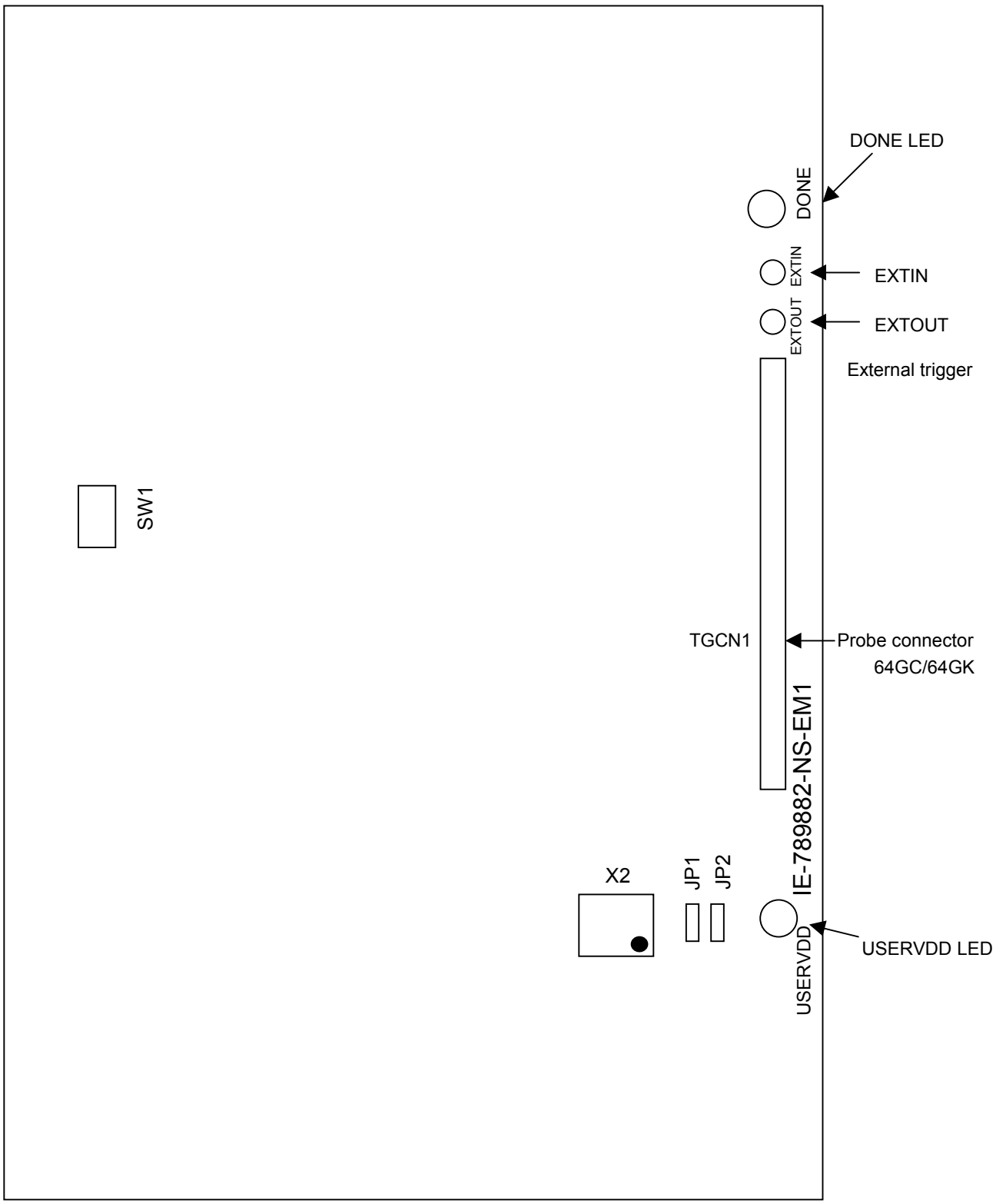
Parameter		Description
Target device		μPD789882 Subseries
System clock		Main system clock: 5.000 MHz Subsystem clock: 32.768 kHz, 38.4 kHz
Clock supply		Internal: Mounted on emulation board
Low-voltage support		2.7 V to 3.6 V: same as the device
Notification function	Target voltage detection LED	Indicates by lighting the LED (USER VDD)
	System configuration completion LED	Indicates by lighting the LED (DONE)

CHAPTER 2 PART NAMES

This chapter introduces the parts of the IE-789882-NS-EM1 main unit.
The packing box contains the emulation board (IE-789882-NS-EM1).
If there are any missing or damaged items, please contact an NEC sales representative.
Fill out and return the guarantee document that comes with the main unit.

2.1 Parts of Board

Figure 2-1. IE-789882-NS-EM1 Part Names



CHAPTER 3 INSTALLATION

This chapter describes methods for connecting the IE-789882-NS-EM1 to the IE-78K0S-NS or IE-78K0S-NS-A and emulation probe. Mode setting methods are also described.

Caution Connecting or removing components to or from the target system, or making switch or other setting changes must be carried out after the power supply to both the IE system and the target system has been switched off.

3.1 Connection

(1) Connection with IE-78K0S-NS or IE-78K0S-NS-A main unit

See the IE-78K0S-NS or IE-78K0S-NS-A User's Manual for a description of how to connect the IE-789882-NS-EM1 to the IE-78K0S-NS or IE-78K0S-NS-A.

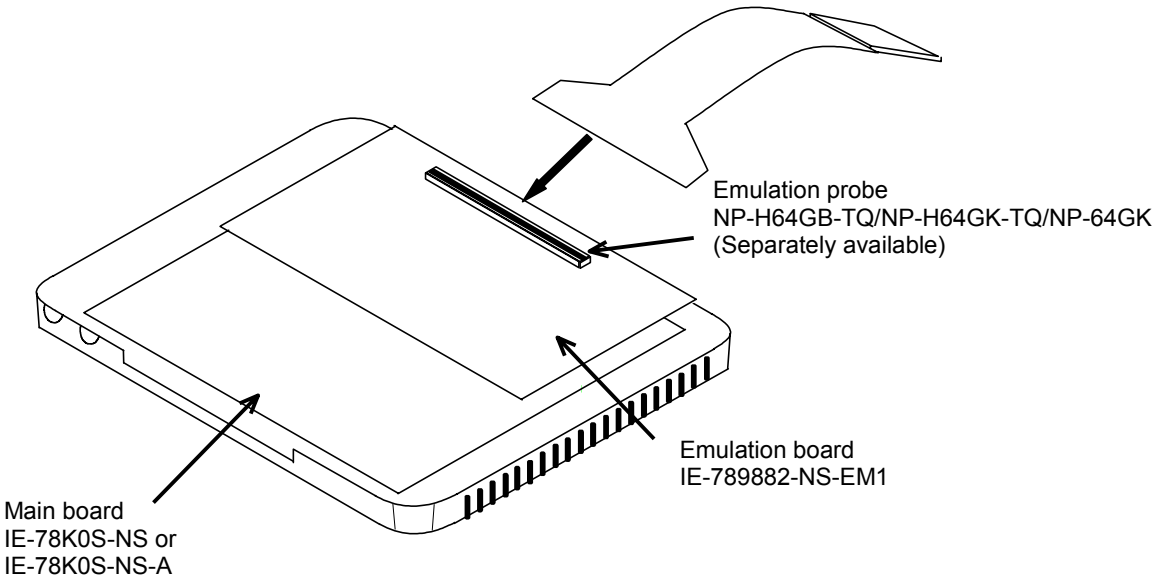
(2) Connection with emulation probe

See the IE-78K0S-NS or IE-78K0S-NS-A User's Manual for a description of how to connect an emulation probe to the IE-789882-NS-EM1.

On this board, connect the emulation probe to TGCN1.

Caution Incorrect connection may damage the IE system. For more details on connection, see the user's manual for each emulation probe.

Figure 3-1. Mounting of Emulation Probe



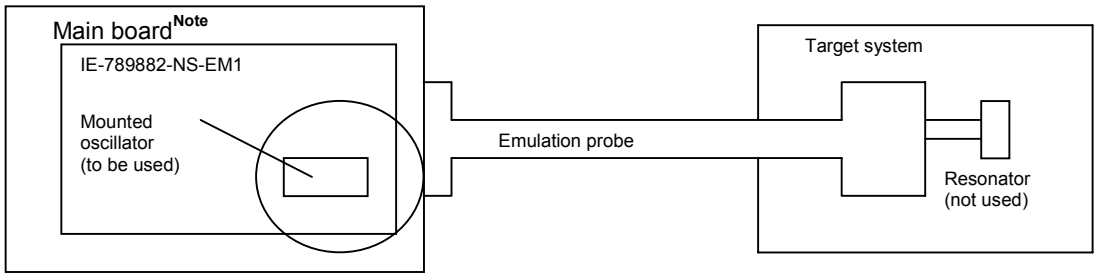
3.2 Clock Settings

3.2.1 Outline of clock settings

The main system clock is fixed to 500 MHz during debugging, the same frequency as that of the internal ring oscillator of the targeted device (the clock frequency cannot be changed).

The oscillator mounted on the target system is not used for the subsystem clock during debugging because the subsystem clock multiplied by four is used for emulation. Instead, the clock mounted on the emulation board is used.

Figure 3-2. Outline of Clock Settings



Only the clock that is supplied from the oscillator on the IE-789882-NS-EM1 (encircled) can be used as the main system clock.

Note Main board: IE-78K0S-NS or IE-78K0S-NS-A

3.2.2 Main system clock settings

When starting the integrated debugger (ID78K0S-NS), open the configuration dialog box and select “Internal” in the area (Clock) for selecting the CPU’s clock source (this selects the emulator’s internal clock).
There is no need to make any other hardware settings.

Caution The program hangs up if an external clock is selected during debugging. When starting the integrated debugger (ID78K0S-NS), open the configuration dialog box and select “Internal” in the area (Clock) for selecting the CPU’s clock source.

3.2.3 Setting of subsystem clock

Table 3-1 shows the setting of the subsystem clock.

Table 3-1. Setting of Subsystem Clock

IE-789882-NS-EM1	Subsystem Clock Frequency Used [Note 1]	
Parts Board (X2)	Subsystem Clock	x4 Subsystem Clock [Note 2]
4.194304 MHz oscillator mounted (as factory-set condition)	32.768 kHz	131.072 kHz
4.1952 MHz oscillator mounted (accessory)	38.4 kHz	153.6 kHz

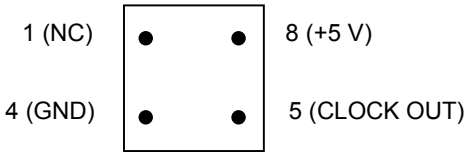
Notes 1. The subsystem clock is generated by dividing the clock of the IE system by 128.

2. The subsystem clock multiplied by four can be set by using a mask option.

Caution Before replacing the oscillator on the board, turn off power to the IE-78K0S-NS or IE-78K0S-NS-A.

- **To replace crystal oscillator**
  - ♦ Necessary items
    - Crystal oscillator (with pin configuration as shown in Figure 3-3)

Figure 3-3. Crystal Oscillator (When Using Subsystem Clock or Clock Mounted by User)

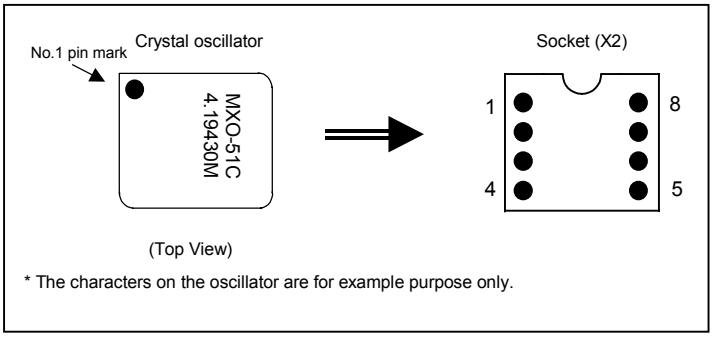


<Procedure>

<1> Prepare the IE-789882-NS-EM1.

<2> Remove the crystal oscillator from the socket (marked X2) on the IE-789882-NS-EM1.

<3> Mount the new crystal oscillator in the socket (X2) from which the oscillator was removed in <2> above. At this time, insert the oscillator into the socket aligning the pins as indicated below.



Crystal Oscillator Pin	Socket Pin No.
NC	1
GND	4
CLOCK OUT	5
+5 V	8

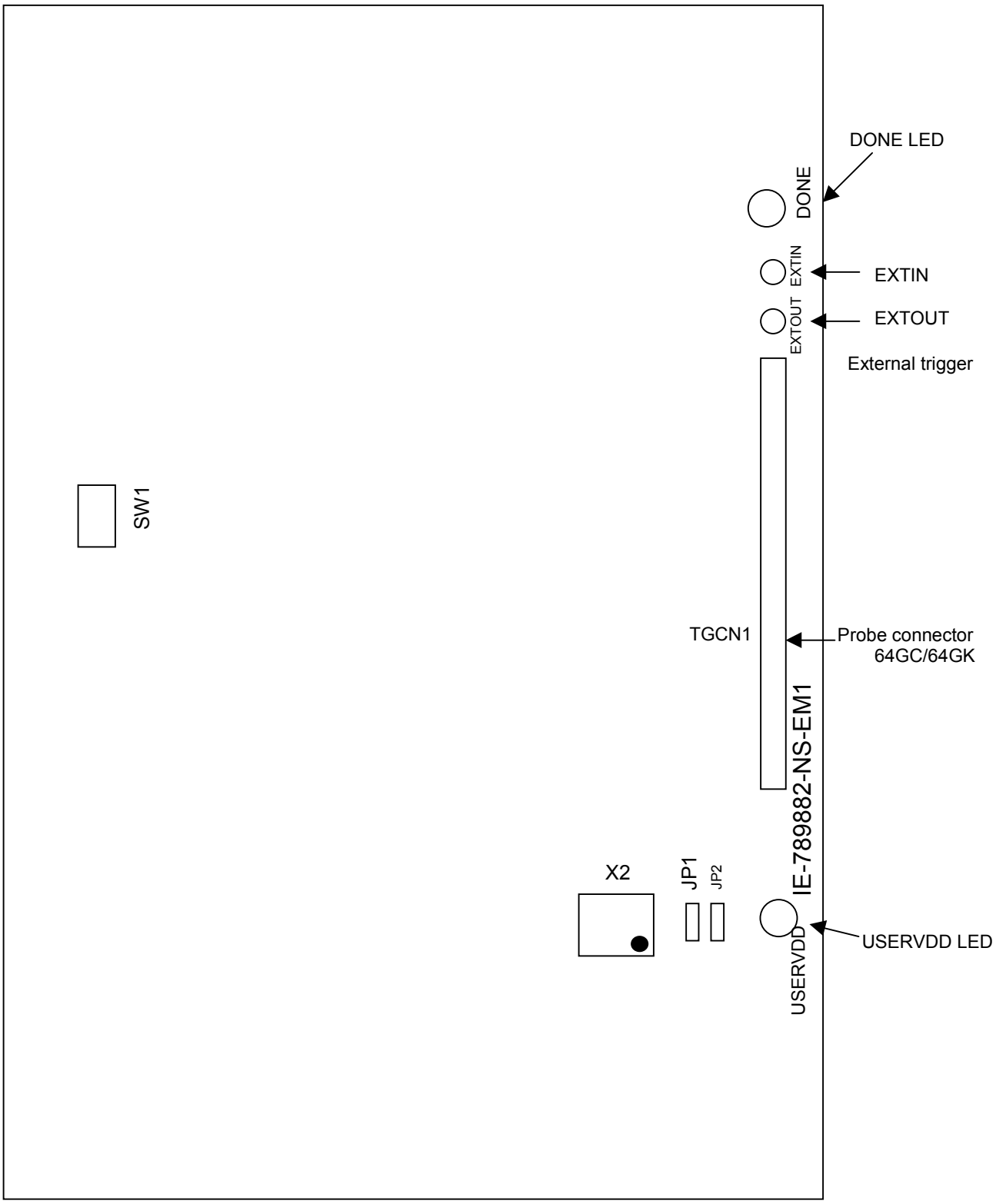
Caution If the crystal oscillator is mounted in the wrong direction, the oscillator may be damaged.

3.3 External Trigger

To set up an external trigger, connect it to the IE-789882-NS-EM1's check pin, EXTIN pin, and EXTOUT pin as shown below.

See the IE-78K0S-NS or IE-78K0S-NS-A User's Manual for descriptions of related use methods and pin characteristics.

Figure 3-4. External Trigger Input Position



3.4 Setting of Main Board

The main board to which the IE-789882-NS-EM1 can be connected is the IE-78K0S-NS or IE-78K0S-NS-A. Set the switches and jumpers on these boards as follows:

(1) Setting of IE-78K0S-NS

Before using the IE-789882-NS-EM1, set each jumper and switch as described below. For the positions of the switches and jumpers, refer to the IE-78K0S-NS User's Manual.

Table 3-4. Setting of Switches and Jumpers on IE-78K0S-NS

	SW1	SW3	SW4	JP1	JP4
Setting	OFF	All "ON"	All "ON"	1-2	2-3

Note Be sure to set the switches and jumpers as described above; otherwise the IE-78K0S-NS may be damaged.

(2) Setting of IE-78K0S-NS-A

Before using the IE-789882-NS-EM1, set each jumper and switch as described below. For the positions of the switches and jumpers, refer to the IE-78K0S-NS-A User's Manual.

Table 3-5. Setting of Switches and Jumpers on IE-78K0S-NS-A

	SW1	JP1	JP3
Setting	OFF	2-3	Shorted (fixed)

Note Be sure to set the switches and jumpers as described above; otherwise the IE-78K0S-NS may be damaged.

3.5 Mask Option Settings

• Mask option of port 5

P50 to 53 of the IE-789882-NS-EM1 can be connected to approx. 33 kΩ pull-up resistor with a dip switch (SW1) of the mask option.

Dip switch settings are as follows:

Table 3-2. SW1 Settings

	SW2			
	1	2	3	4
Connects to	P50	P51	P52	P53

The pin is pulled-up with the target voltage LVCC pin when the dip switch is set on. When the dip switch is set off, the pin is disconnected.

* Default setting (when shipped) SW1: all off

• Subsystem clock 4x mask option

In the IE-789882-NS-EM1, 4x subsystem clock selection mask options can be set.

Table 3-3. JP2 Settings

Location	Setting	Function
JP2	1-2	Original frequency when CPU subsystem clock operates (SSUB = 1)
	2-3 (factory setting)	4x frequency when CPU subsystem clock operates (SSUB = 0)

Remark When debugging a flash model (such as the μPD78F9882), use the JP2 setting of 2-3 shorted (factory-set condition).

The setting when the CPU subsystem clock is used must be changed by using an SFR.

For details, refer to the manual of the device.

3.6 Other Jumper Settings

• JP1: 1-2 short (fixed)

Use other jumper switches in their default settings.

3.7 Setting for Emulating Target Voltage

Because the IE-789882-NS-EM1 internally emulates the voltage (2.7 to 3.6 V: same as the voltage to the device) supplied from the VDD pin of the emulation probe, no special setting is necessary.

If the target board is used, be sure to supply the same voltage as the target system to the VDD pin.

If the target board is not used, the emulator is designed to automatically operate on the internal voltage.

CHAPTER 4 DIFFERENCES BETWEEN TARGET DEVICES AND TARGET INTERFACE CIRCUITS

This chapter describes differences between the target device's signal lines and the signal lines of the IE-789882-NS-EM1's target interface circuit.

Although the target device is a CMOS circuit, the IE-789882-NS-EM1's target interface circuit consists of a pin emulator, TTL, CMOS-IC, and other emulation circuits.

When the IE system is connected with the target system for debugging, the IE system performs emulation so as to operate as the actual target device would operate in the target system.

However, some minor differences exist since the operations are performed via the IE system's emulation.

(1) CPU EVA chip, signals input/output to/from the μPD789009A
(2) Signals input/output to/from the pin emulator and μPD7883
(3) Signals output from the pin emulator and μPD7883
(4) Other signals

The IE system's circuit is used as follows for signals listed in (1) to (3) above.

(1) CPU EVA chip, signals input/output to/from the μPD789009A

- Signals related to port 0
- Signals related to port 1
- RESET

(2) Signals input/output to/from the pin emulator and μPD7883

- Signals related to port 3
- Signals related to port 5

(3) Signals output from the pin emulator and μPD7883

- Signals related to port 2
- Signals related to port 8
- Signals related to port 9
- Signals related to LCD

  COM, S

(4) Other signals

- VDD (target voltage input from the probe)
- VSS

Figure 4-1. Equivalent Circuit of Emulation Circuit (1)

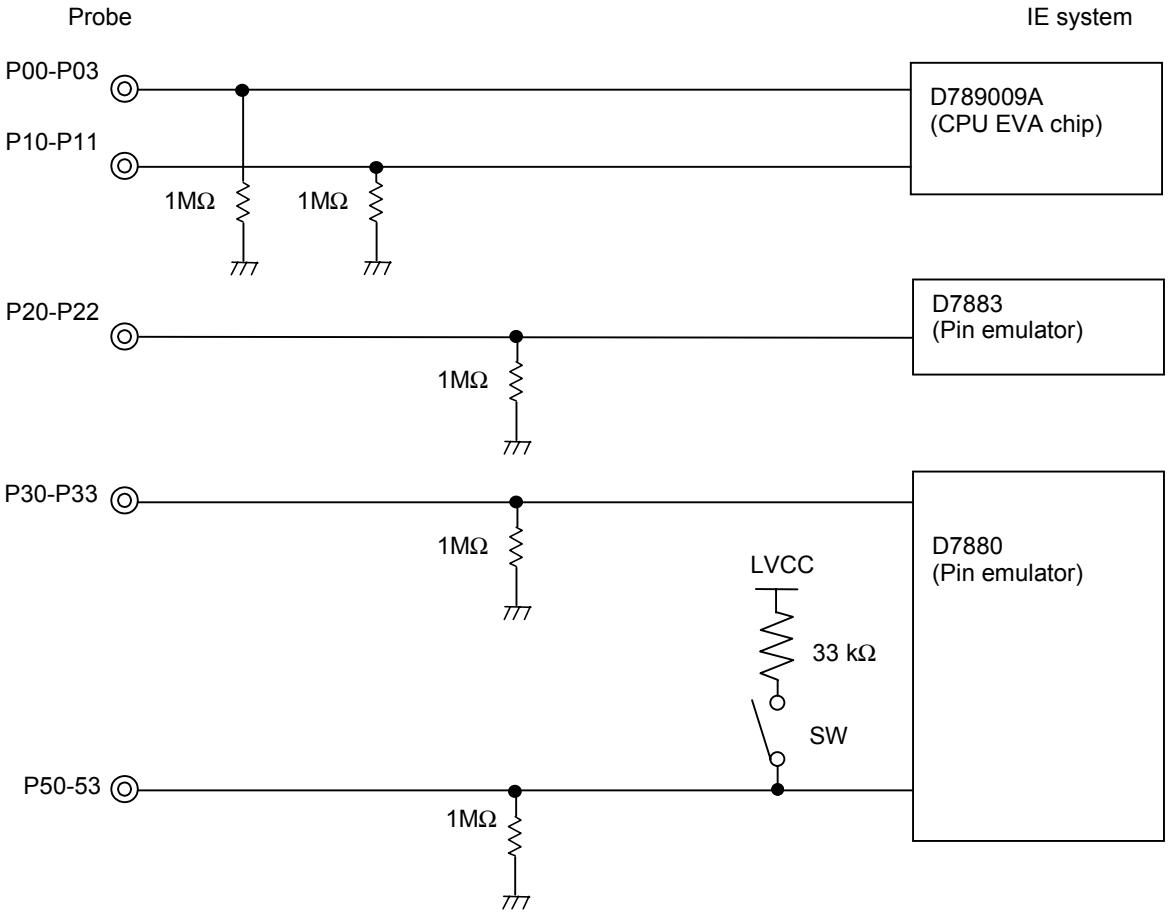
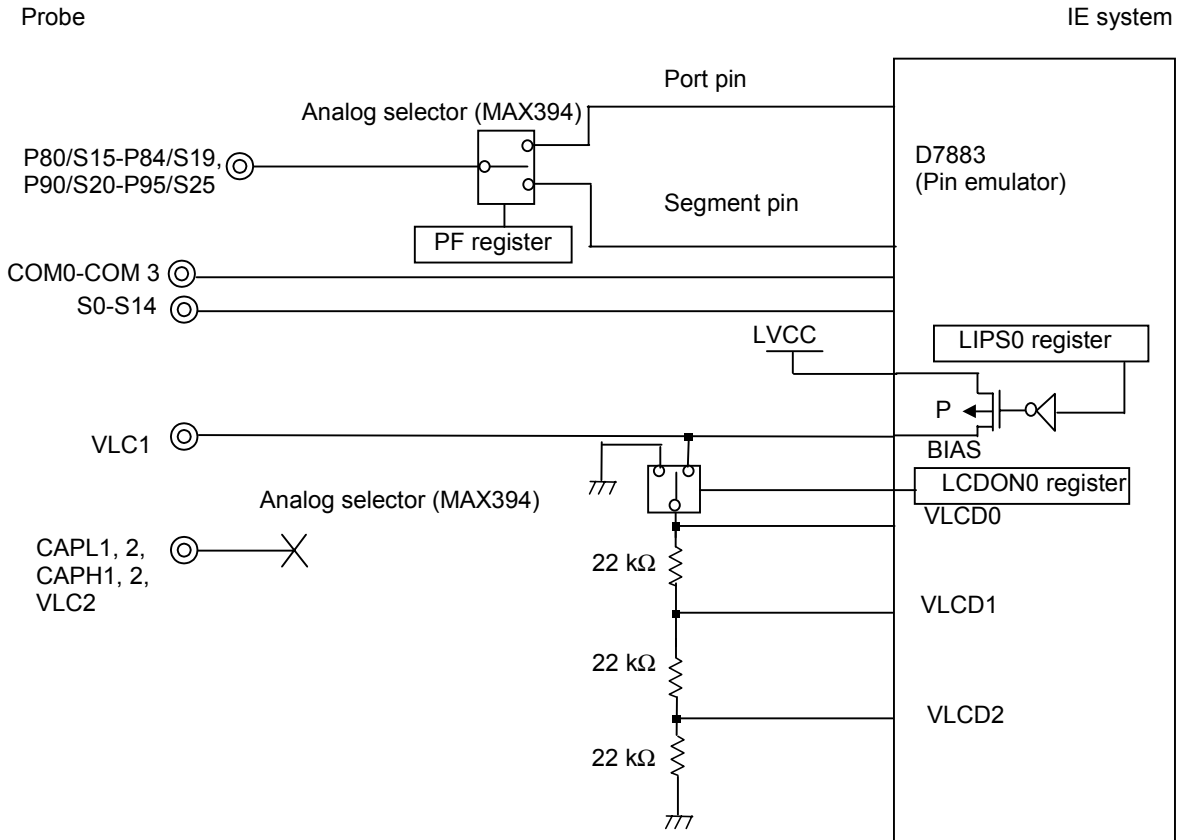


Figure 4-2. Equivalent Circuit of Emulation Circuit (2)

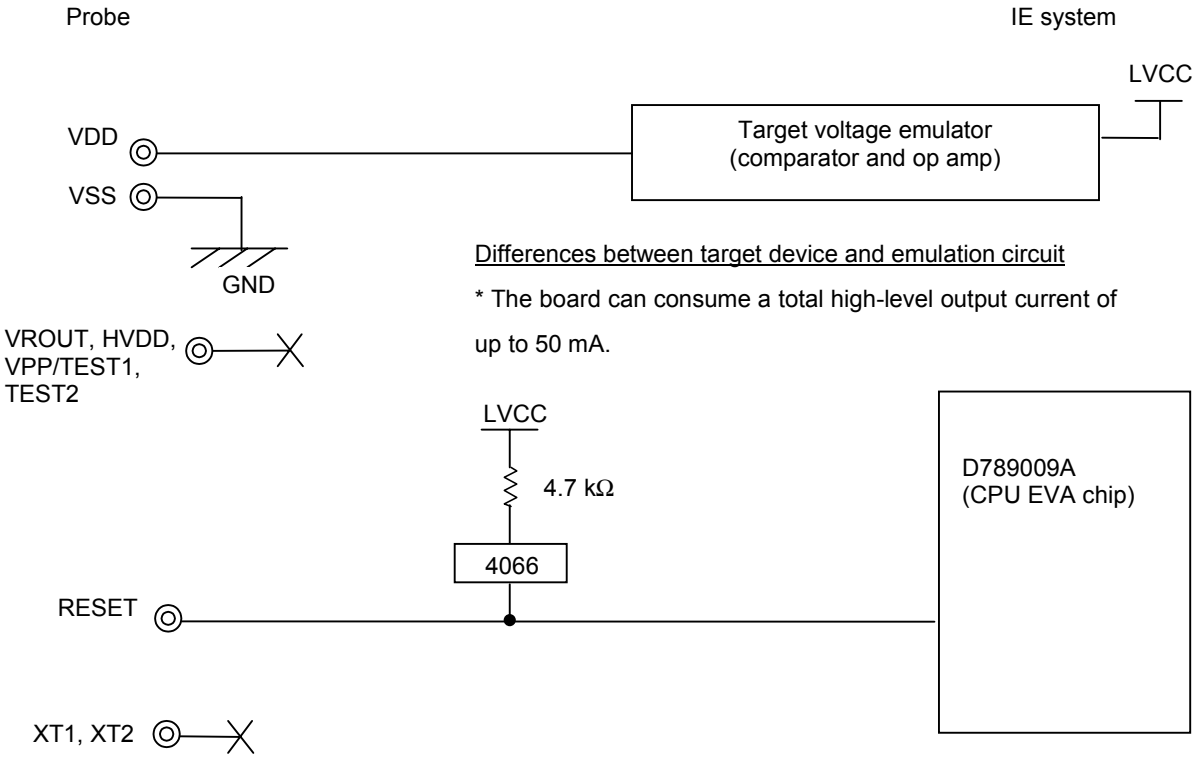


Differences between target device and emulation circuit

*In the dynamic mode, the LVCC voltage is divided to generate the LDC drive voltage by the LIPS register, regardless of the capacitor connector to the VLC1 pin.

In the static mode, the voltage of the VLC1 pin is connected in parallel with the LCD drive pin (VLCD0 of the D7883) to three 22 kΩ resistors (66 kΩ in all).

Figure 4-3. Equivalent Circuit of Emulation Circuit (3)



CHAPTER 5 DIFFERENCES IN OPERATION BETWEEN TARGET DEVICE AND EMULATION BOARD

This chapter explains the operational differences between the target device and IE-789882-NS-EM1.

(1) A wait cycle of one subsystem clock is not inserted when the HALT mode is released.

Because the clock mounted on the IE system is used, the x4 subsystem clock is supplied to the peripheral circuits even in the HALT mode.

Table 5-1. Operation of Subsystem Clock During Break

Peripheral Break Mode	Selection of CPU Operating Subsystem Clock (Setting of SCS Register or Mask Option)	Operation of Subsystem Clock During Break	
		Original Clock (f_{XT}) Divided by two (f_{XT}/2^n)	×4 clock ($4f_{XT}$)
Valid (ON)	×4 subsystem clock	Stopped	Stopped
	Original subsystem clock	Stopped	Stopped
Invalid (OFF)	×4 subsystem clock	Operates	Operates
	Original subsystem clock	Operates	Stopped

(2) No oscillation stabilization time elapses when reset is cleared.

As soon as reset has been cleared, the CPU starts operating.

(3) Concerning subsystem clock during break

The subsystem clock operation stops during a break if the peripheral break mode is off and the x4 clock is used.

(4) The subsystem clock on the target system cannot be emulated.

Use the subsystem clock on the emulation board. Refer to **3.2.3 Setting of Subsystem Clock** for details.

APPENDIX. EMULATION PROBE PIN CORRESPONDENCE TABLE

Table A-1. NP-H64GB-TQ, NP-H64GK-TQ, and NP-64GK Pin Correspondence

Emulation Probe Pin No.	TGCN1 Pin No.	Emulation Probe Pin No.	TGCN1 Pin No.
1	108	41	92
2	107	42	91
3	104	43	98
4	103	44	97
5	100	45	102
6	99	46	101
7	94	47	106
8	93	48	105
9	30	49	77
10	29	50	78
11	24	51	73
12	23	52	74
13	20	53	69
14	19	54	70
15	16	55	63
16	15	56	64
17	43	57	61
18	44	58	62
19	47	59	65
20	48	60	66
21	51	61	71
22	52	62	72
23	57	63	75
24	58	64	76
25	59		
26	60		
27	55		
28	56		
29	49		
30	50		
31	45		
32	46		
33	14		
34	13		
35	18		
36	17		
37	22		
38	21		
39	28		
40	27		

Remark NP-H64GB-TQ, NP-H64GK-TQ, and NP-64GK are products of Naito Densei Machida Mfg. Co., Ltd.