CUSTOMER NOTIFICATION

SUD-TT-0218-1-E

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IE-789488-NS-EM1

Preliminary User's Manual

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REVISION HISTORY

The control code and revision history are shown below.

Control Code [Note]	Document No.	Description
A, B, C	SUD-T-4599-1-E (Apr. 2, 2000)	Newly created.
D	SUD-T-4884-2-E (Jul. 18, 2001)	Addition of description on IE-78K0S-NS-A (main board), addition of APPENDIX B NOTES ON TARGET SYSTEM DESIGN, correction of erroneous description
E	SUD-TT-0218-1-E (This document)	Addition of μPD789479, 78F9479, 789489, 78F9489 as target devices, correction of erroneous description

Note The “control code” is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.

INTRODUCTION

Product Overview

The IE-789488-NS-EM1 is designed to be used with the IE-78K0S-NS or IE-78K0S-NS-A to debug the following target devices that belong to the 78K0S Series of 8-bit single-chip microcontrollers.

- μPD789479 Subseries: μPD789477, 789478, 78F9478, 789479, 78F9479
- μPD789489 Subseries: μPD789488, 78F9488, 789489, 78F9489

Target Readers

This manual is intended for engineers who will use the IE-789488-NS-EM1 with the IE-78K0S-NS or IE-78K0S-NS-A to perform system debugging.
Engineers who use this manual are expected to be thoroughly familiar with the target device's functions and use methods and to be knowledgeable about debugging.

Organization

When using the IE-789488-NS-EM1, refer to not only this manual (supplied with the IE-789488-NS-EM1) but also the manual that is supplied with the IE-78K0S-NS or IE-78K0S-NS-A.

IE-78K0S-NS User's Manual	IE-78K0S-NS-A User's Manual	IE-789488-NS-EM1 User's Manual
• Basic specifications • System configuration • External interface functions	• Basic specifications • System configuration • External interface functions	• General • Part names • Installation • Differences between target devices and target interface circuits

Purpose

This manual's purpose is to explain various debugging functions that can be performed when using the IE-789488-NS-EM1.

Terminology The meanings of certain terms used in this manual are listed below.

Term	Meaning
Emulation device	This is a general term that refers to the device in the emulator that is used to emulate the target device. It includes the emulation CPU.
Emulation CPU	This is the CPU block in the emulator that is used to execute user-generated programs.
Target device	This is the device (a real chip) that is the target for emulation.
Target system	This includes the target program and the hardware provided by the user. When defined narrowly, it includes only the hardware.
IE system	This refers to the combination of the IE-78K0S-NS or IE-78K0S-NS-A and the IE-789488-NS-EM1.

Conventions

Data significance: Higher digits on the left and lower digits on the right

Note: Footnote for item marked with **Note** in the text

Caution: Information requiring particular attention

Remark: Supplementary information

Related Document The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name	Document Number	
	Japanese	English
IE-78K0S-NS	U13549J	U13549E
IE-78K0S-NS-A	U15207J	U15207E
IE-789488-NS-EM1	SUD-TT-0218-1	This manual
ID78K Series Integrated Debugger Ver.2.30 or Later Operation (Windows™ Based)	U15185J	U15185E
μPD789478 Subseries	U15400J	U15400E
μPD789479 Subseries		
μPD789488 Subseries	U15331J	U15331E
μPD789489 Subseries		

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1 GENERAL

The IE-789488-NS-EM1 is a development tool for efficient debugging of hardware or software when using one of the following target devices that belong to the 78K0S Series of 8-bit single-chip microcontrollers.

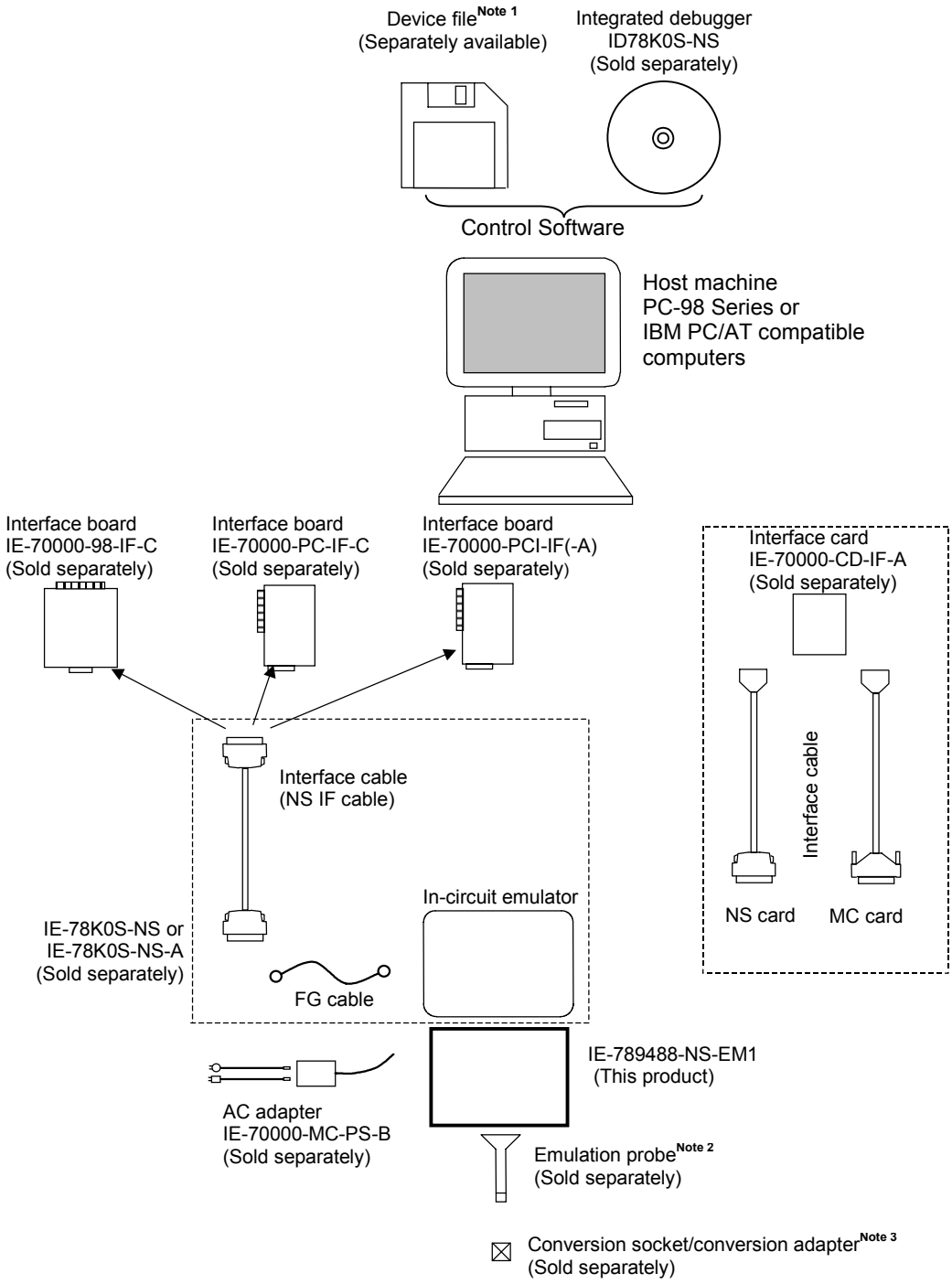
This chapter describes the IE-789488-NS-EM1 system configuration and basic specifications.

- Target device
  - μPD789479 Subseries
  - μPD789489 Subseries

1.1 System Configuration

Figure 1-1 illustrates the IE-789488-NS-EM1 system configuration.

Figure 1-1. System Configuration



Notes 1. The device file is as follows.

μSxxxxDF789488: μPD789479, 789489 Subseries

The device file can be downloaded from the NEC Electron Devices Microprocessor homepage. (URL: http://www.ic.nec.co.jp/micro)

2. The emulation probe is as follows.

NP-H80GK-TQ: 80-pin plastic TQFP (probe length: 400 mm)
NP-80GK: 80-pin plastic TQFP (probe length: 200 mm)
NP-H80GC-TQ: 80-pin plastic QFP (probe length: 400 mm)
NP-80GC-TQ: 80-pin plastic QFP (probe length: 200 mm)
NP-80GC: 80-pin plastic QFP (probe length: 200 mm)

NP-H80GK-TQ, NP-80GK, NP-H80GC-TQ, NP-80GC-TQ, and NP-80GC are products of Naito Densei Machida Mfg. Co., Ltd.

Contact: Naito Densei Machida Mfg. Co., Ltd. (TEL: 045-475-4191)

3. The conversion socket and conversion adapter are as follows.

TGK-080SDP: 80-pin plastic TQFP (GK-9EU)
TGC-080SBP: 80-pin plastic QFP (GC-8BT)
EV-9200GC-80: 80-pin plastic QFP (GC-8BT)

TGK-080SDP, TGC-080SBP, and EV-9200GC-80 are products of Tokyo Eletech Corporation.

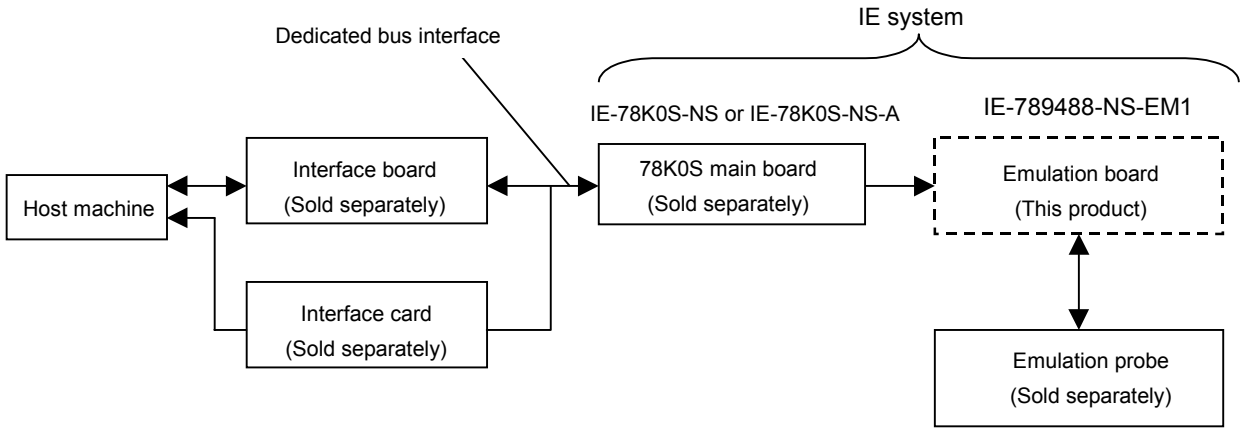
For further information, contact: Daimaru Kogyo, Ltd.

Tokyo Electronics Department (TEL +81-3-3820-7112)
Osaka Electronics Department (TEL +81-6-6244-6672)

1.2 Hardware Configuration

Figure 1-2 shows the IE-789488-NS-EM1's position in the basic hardware configuration.

Figure 1-2. Basic Hardware Configuration



1.3 Basic Specifications

The IE-789488-NS-EM1's basic specifications are listed in Table 1-1.

Table 1-1. Basic Specifications

Parameter	Description
Target devices	μPD789479, 789489 Subseries
System clock	Main system clock: 1.000 to 5.000 MHz Subsystem clock: 32.768 kHz
Main clock supply	Internal: Mounted on the emulation board (5 MHz) or mounted by user on the parts board External: Pulse input from the target system via an emulation probe
Subclock supply	Internal: Mounted on the emulation board (32.768 kHz) or mounted by user on the parts board External: Pulse input from the target system via an emulation probe
Target interface voltage	V_{DD} = 1.8 V to 5.5 V (Same as the target device) When target system not connected: Operates @ 5 V internal voltage

CHAPTER 2 PART NAMES

This chapter introduces the parts of the IE-789488-NS-EM1 main unit.

The packing box contains the emulation board (IE-789488-NS-EM1), package details, user's manual, and guarantee card.

If there are any missing or damaged items, please contact an NEC sales representative.

Fill out and return the guarantee card that comes with the main unit.

2.1 Names of Parts on Board

The IE-789488-NS-EM1 includes the following two boards.

- Probe board (IE-789488-NS-EM1 PROBE Board): 1
- I/O board (IE-789488-NS-EM1 I/O Board): 1

Figure 2-1 shows the names of the parts on the probe board.

Figure 2-1. Names of Parts on Probe Board (IE-789488-NS-EM1 PROBE Board)

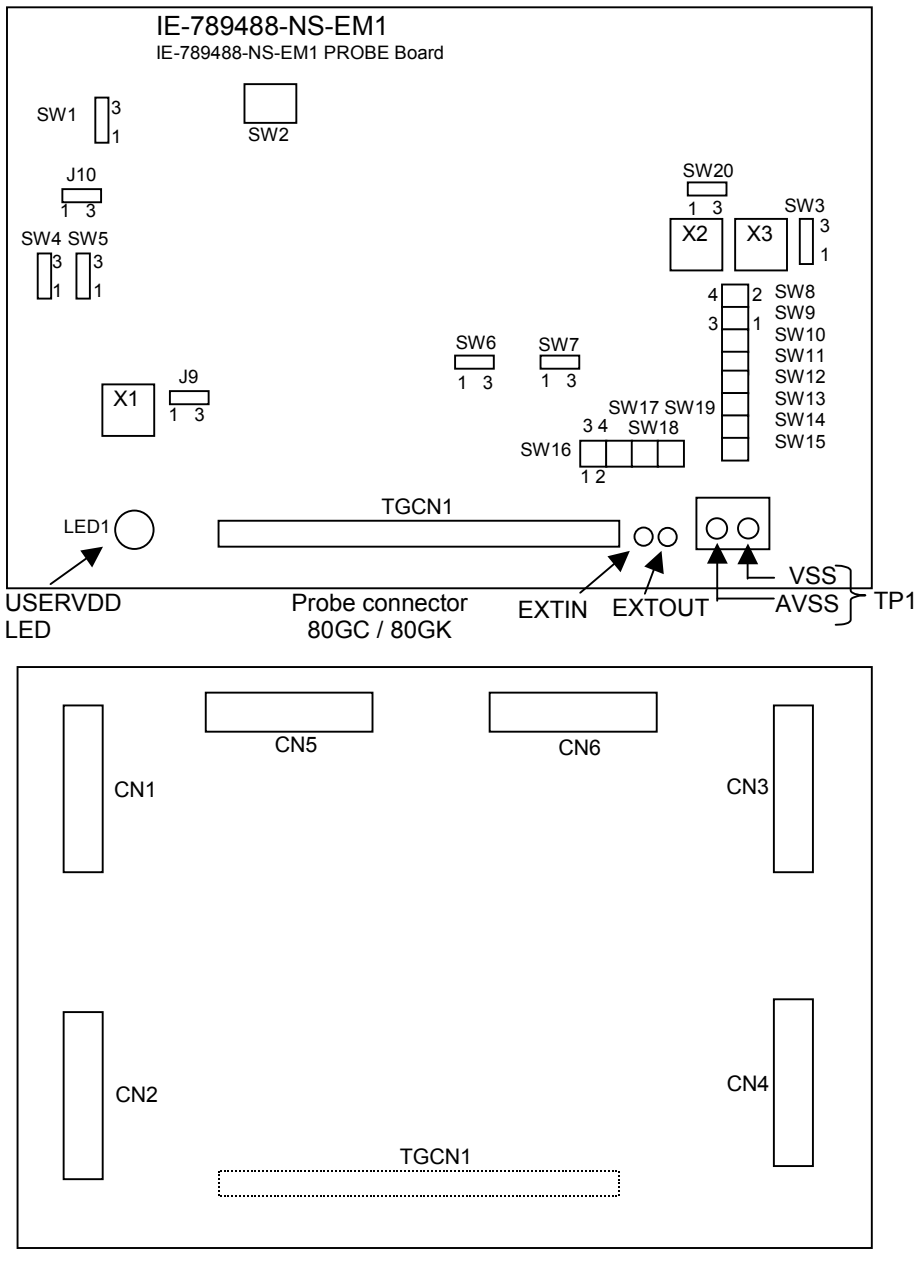
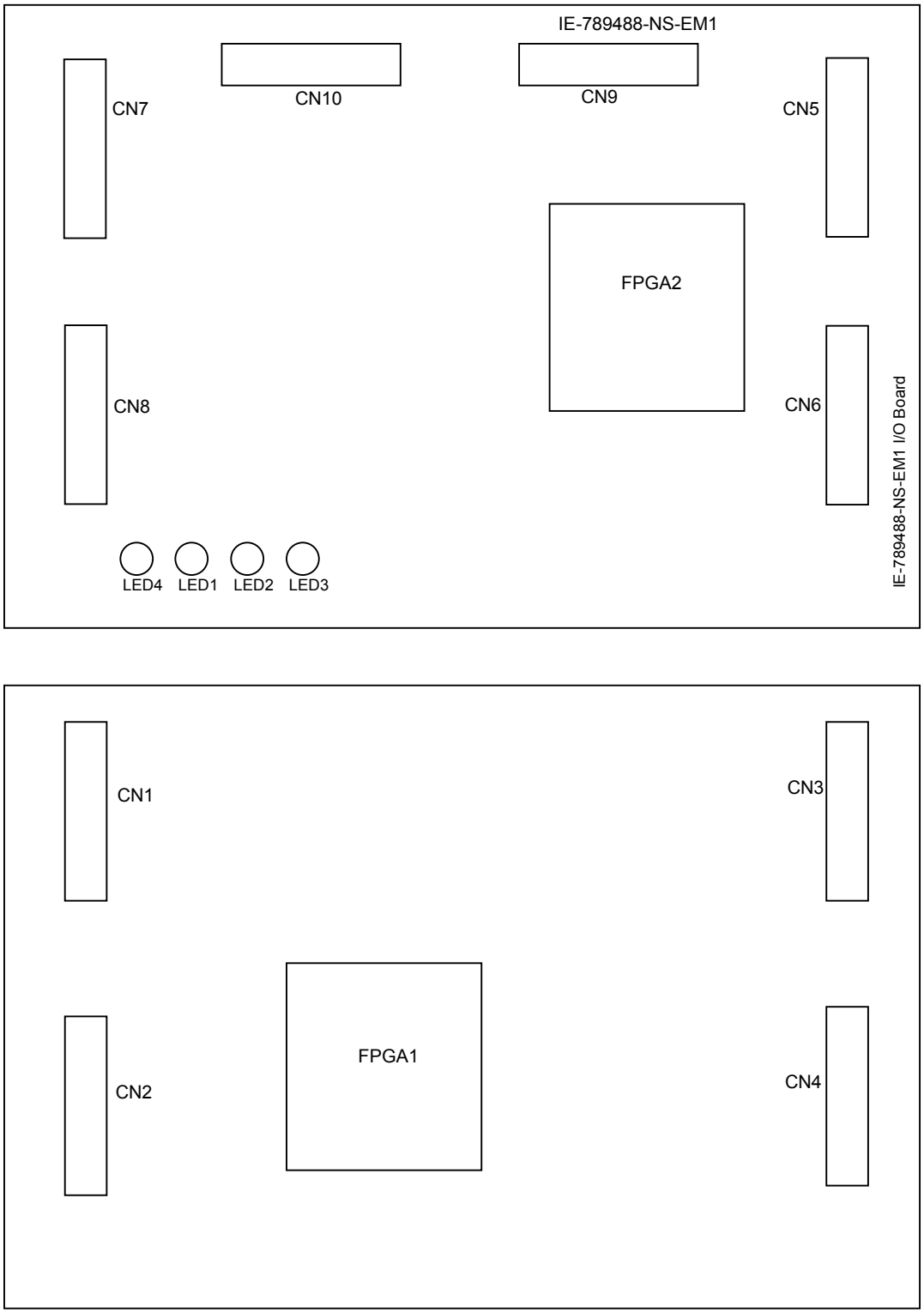


Figure 2-2 shows the names of the parts on the I/O board.

Figure 2-2. Names of Parts on I/O Board (IE-789488-NS-EM1 I/O Board)



2.2 Initial Settings of Switches and Jumpers

Table 2-1 shows the initial settings of switches and jumpers on the IE-789488-NS-EM1 probe board (IE-789488-NS-EM1 PROBE Board).

Refer to **3.3 Switch and Jumper Settings** for the J9, SW4, and SW6 settings.

Refer to **3.5 Clock Settings** for the SW1 setting.

Refer to **3.6 Subsystem Clock x4 Circuit Settings** for the SW3 and SW20 settings.

Refer to **3.7 Mask Option Settings** for the SW2, SW8 to SW19 settings.

Use SW5, SW7, and J10 with the default settings.

Table 2-1. Initial Settings of Switches and Jumpers

	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10
Initial setting	2-3	All OFF	1-2	1-2	1-2 (fixed)	1-2	2-3 (fixed)	1-3 2-4	1-3 2-4	1-3 2-4
	SW11	SW12	SW13	SW14	SW15	SW16	SW17	SW18	SW19	SW20
Initial setting	1-3 2-4	1-3 2-4	1-3 2-4	1-3 2-4	1-3 2-4	1-3 2-4	1-3 2-4	1-3 2-4	1-3 2-4	2-3
	J9	J10								
Initial setting	1-2	1-2 (fixed)								

There are no manual switches and jumpers on the I/O board of the IE-789488-NS-EM1 (IE-789488-NS-EM1 I/O Board).

CHAPTER 3 INSTALLATION

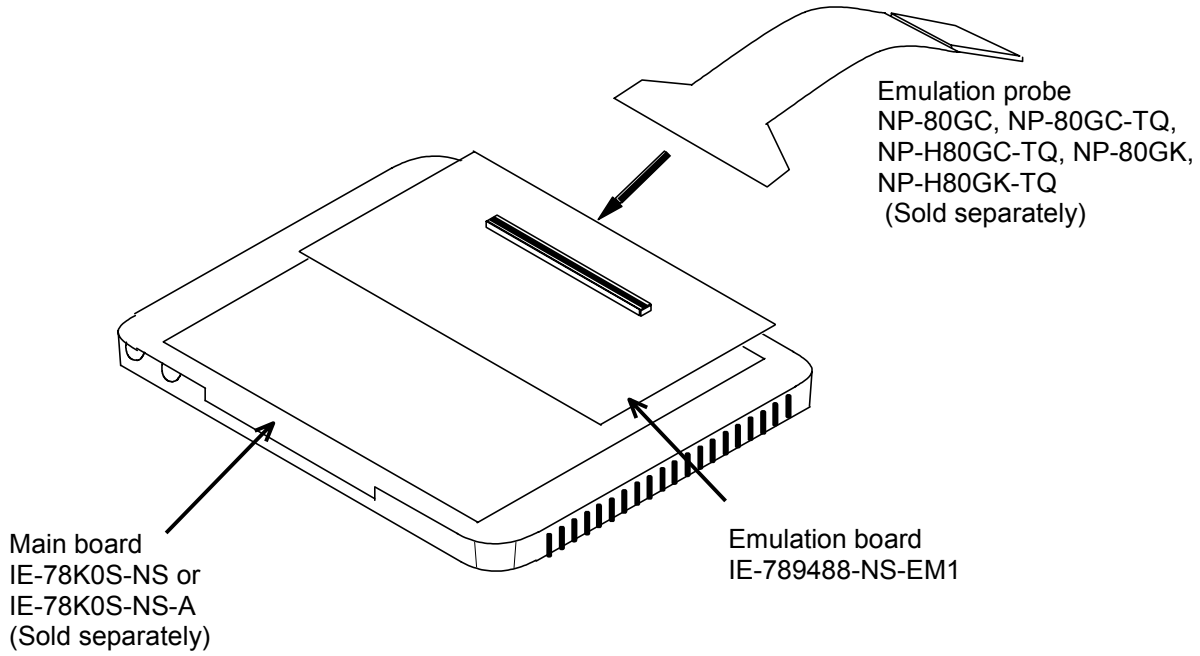
This chapter describes methods for connecting the IE-789488-NS-EM1 to the IE-78K0S-NS or IE-78K0S-NS-A and emulation probe. Mode setting methods are also described.

Caution Connecting or removing parts to or from the target system, or making switch or other setting changes must be carried out after the power supply to both the IE system and the target system has been switched off.

3.1 Connection

A connection diagram of the emulation probe and the main board is shown in Figure 3-1.

Figure 3-1. Mounting of Emulation Probe and Main Board



(1) Connection with IE-78K0S-NS-A or IE-78K0S-NS-A main unit

See the IE-78K0S-NS User's Manual (U13549E) or IE-78K0S-NS-A User's Manual (U15207E) for a description of how to connect the IE-789488-NS-EM1 to the IE-78K0S-NS or IE-78K0S-NS-A.

(2) Connection with emulation probe

See the IE-78K0S-NS-A User's Manual (U15207E) or IE-78K0S-NS-A User's Manual (U15207E) for a description of how to connect an emulation probe to the IE-789488-NS-EM1.

On this board, connect the emulation probe to TGCN1.

Caution Incorrect connection may damage the IE system. For more details on connection, see the user's manual for each emulation probe.

3.2 Settings of Switches and Jumpers on Main Board

(1) Setting of IE-78K0S-NS

Before using the IE-789488-NS-EM1, set each jumper and switch of the IE-78K0S-NS as described below. For the positions of the switches and jumpers, refer to the IE-78K0S-NS User's Manual (U13549E).

Table 3-1. Setting of Switches and Jumpers on IE-78K0S-NS

	SW1	SW3	SW4	JP1	JP4
Setting	OFF	All "ON" (fixed)	All "ON" (fixed)	2-3 shorted	1-2 shorted

(2) Setting of IE-78K0S-NS-A

Before using the IE-789488-NS-EM1, set each jumper and switch of the IE-78K0S-NS-A as described below. For the positions of the switches and jumpers, refer to the IE-78K0S-NS-A User's Manual (U15207E).

Table 3-2. Setting of Switches and Jumpers on IE-78K0S-NS-A

	SW1	JP1	JP3
Setting	OFF	1-2 shorted	Shorted (fixed)

3.3 Settings of Switches and Jumpers

3.3.1 Jumper setting for selecting subseries

With the IE-789488-NS-EM1, a jumper setting can be used to select which subseries, the μPD789479 Subseries or the μPD789489 Subseries, will be debugged. By default, the μPD789479 Subseries is selected.

The connection setting for the jumper is shown in Table 3-3.

Table 3-3. Jumper Setting to Select Subseries

Subseries Selection	J9 Setting
μPD789479 Subseries	1-2 shorted (default)
μPD789489 Subseries	2-3 shorted

Caution Set the jumper when the power of the IE-78K0S-NS or IE-78K0S-NS-A is off.

3.3.2 LCD emulation setting for μPD789489 Subseries

In the IE-789488-NS-EM1, the panel voltage (power supply of the target system) is set by switching the internal power supply between 5 V and 3 V using SW4, not by setting the boost voltage in the LCD display mode register. Refer to **CHAPTER 5 CAUTIONS** for differences between the target device and target interface circuit settings.

The connection settings for 5 V and 3 V are shown in Table 3-4.

Table 3-4. LCD Panel Voltage Setting

Panel Voltage Setting	SW4 Setting
Connected to internal power supply 5 V	1-2 shorted (default)
Connected to internal power supply 3 V	2-3 shorted

Cautions 1. Set SW4 when the power of the IE-78K0S-NS or IE-78K0S-NS-A is off.

2. The voltage set to SW4 is always used as the panel voltage regardless of the setting of bit 0 (GAIN) of LCD boost voltage control register 0 (LCDVA0).

3.3.3 Isolation setting for digital/analog ground

In the IE-789488-NS-EM1, the digital and analog ground can be isolated by a switch.

By default, VSS and AVSS are connected via a filter.

The setting of the switch is shown in Table 3-5.

Table 3-5. Isolation Setting of VSS and AVSS

Status	SW6 Setting
VSS and AVSS are connected via a filter.	1-2 shorted (default)
VSS and AVSS are isolated.	2-3 shorted

Cautions 1. Set SW6 when the power of the IE-78K0S-NS or IE-78K0S-NS-A is off.

2. Be sure to use the 1-2 shorted setting when the target system is not connected.

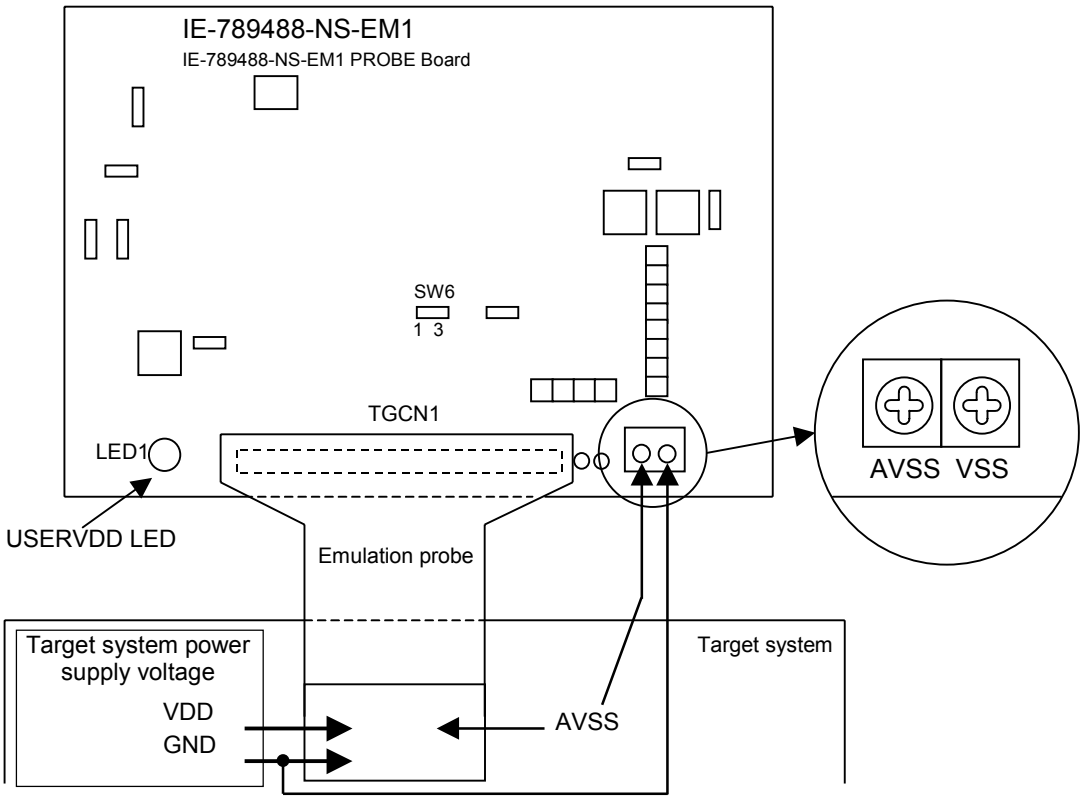
3.4 Settings of Target Interface Voltage

Because the IE-789488-NS-EM1 internally generates the voltage for the target interface (1.8 to 5.5 V; the same as the voltage to the device) supplied from the VDD pin of the emulation probe, no special setting is necessary.
There is no need to make any hardware settings. When the target system is not used (VDD = 0 V), the emulator is designed to automatically operate on the internal voltage (5 V).
The settings for the target interface voltage are shown in Table 3-6.

Table 3-6. Target Interface Voltage Settings

Target Interface Voltage		Integrated Debugger (ID78K0S-NS) Operation Voltage Selection
When the target system is used	1.8 to 5.5 V	Target
When the target system is not used	5 V	Internal

Figure 3-2. Connection of Target System Voltage



Cautions 1. When using the target system, open the configuration dialog box when starting the integrated debugger and select "Target" in the operation voltage selection area (Voltage).

2. The maximum current that can be consumed when operating on VDD current of the target is 1.8 to 5.5 V: approx.100 mA.

3. The TP1 GND pin can be connected to VSS and AVSS on the pin board to reinforce GND. VSS and AVSS of the target system can be independently supplied to the in-circuit emulator.

3.5 Clock Settings

3.5.1 Outline of clock settings

The main system clock and subsystem clock to be used during debugging can be selected from (1) to (3) below.

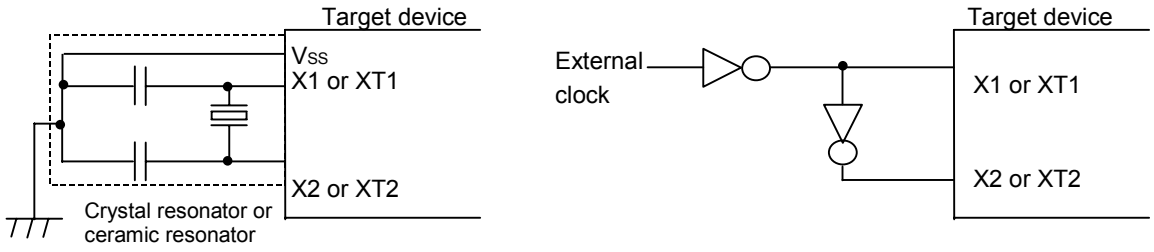
(1) Clock already mounted on emulation board
(2) Clock mounted by user
(3) Pulse input from the target system

If the target system includes a clock oscillator, select either “(1) Clock already mounted on emulation board” or “(2) Clock mounted by user”. For a clock oscillator, the target device is connected to a resonator and the target device’s internal oscillator is used. An example of the external circuit is shown in part (a) of Figure 3-3. During emulation, the clock oscillator that is mounted on the target system is not used. Instead, the clock that is mounted on the emulation board, which is installed for the IE-78K0S-NS or IE-78K0S-NS-A, is used.
If the target system includes an external clock, select either “(1) Clock already mounted on emulation board”, “(2) Clock mounted by user”, or “(3) Pulse input from the target system”. For an external clock, a clock signal is supplied from outside of the target device and the target device’s internal oscillator is not used. An example of the external circuit is shown in part (b) of Figure 3-3.

Caution The IE system will hang up if the main system clock is not supplied correctly. In addition, input a rectangular pulse from the target system. It is not necessary to input clock to X2 and XT2 pins. The program does not operate if a crystal resonator is connected directly to X1 (in case of main system clock) or XT1 (in case of subsystem clock).

Figure 3-3. External Circuits Used as System Clock Oscillator

(a) Clock oscillator **(b) External clock**



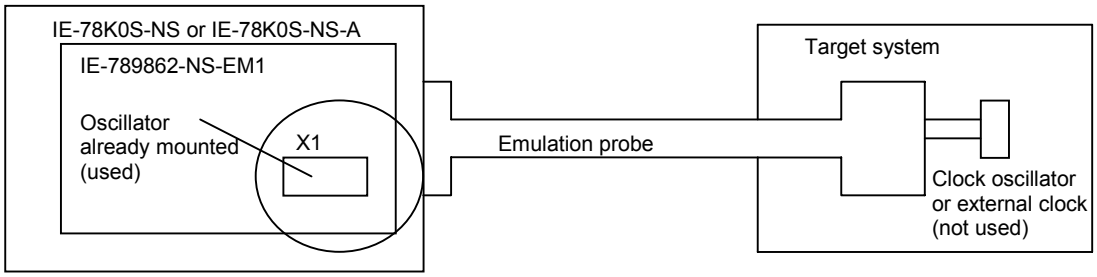
(1) Clock already mounted on emulation board

The oscillator that is already mounted in the IE-789488-NS-EM1 can be used.

(a) Main system clock

The 5.0 MHz crystal oscillator (X1) is already mounted on the emulation board.

Figure 3-4. When Using Clock Already Mounted on Emulation Board (Main System Clock)

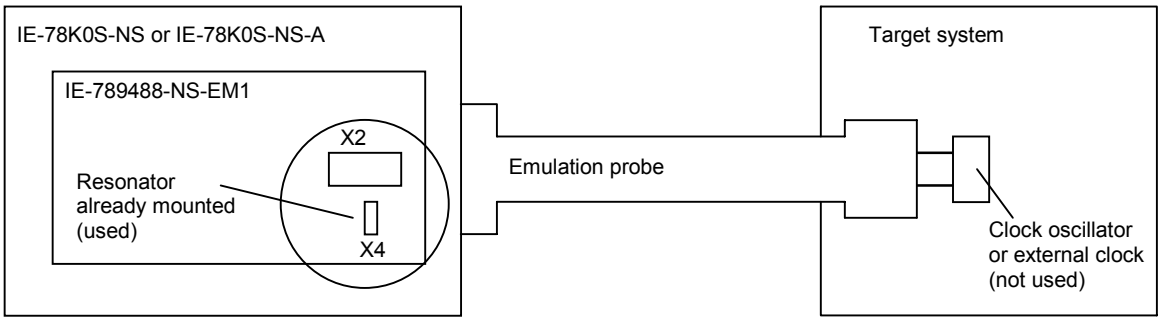


Remark The clock that is supplied by the IE-789488-NS-EM1's oscillator (encircled in the figure) is used.

(b) Subsystem clock

The 32.768 kHz crystal resonator (XTC1) is already mounted on the emulation board.

Figure 3-5. When Using Clock Already Mounted on Emulation Board (Subsystem Clock)



Remark The clock that is supplied by the IE-789488-NS-EM1's resonator (encircled in the figure) is used.

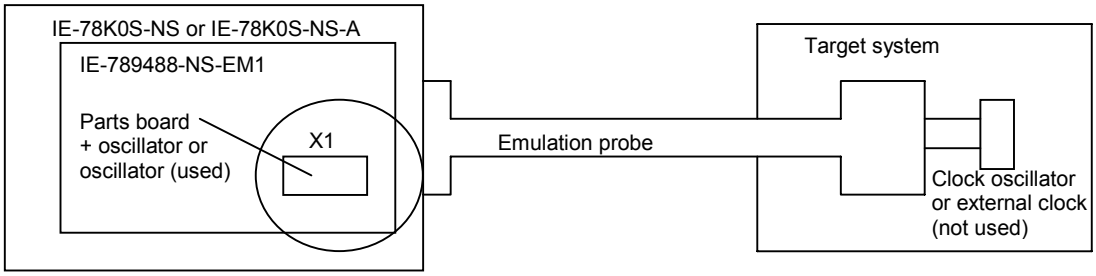
(2) Clock mounted by user

The user is able to mount any clock supported by the set specifications on the IE-789488-NS-EM1. This method is useful when using a different frequency from that of the pre-mounted clock.

(a) Main system clock

Remove the crystal oscillator (X1) that is already mounted on the emulation board, and mount either the parts board on which the resonator to be used is mounted or an oscillator.

Figure 3-6. When Using Clock Mounted by User (Main System Clock)

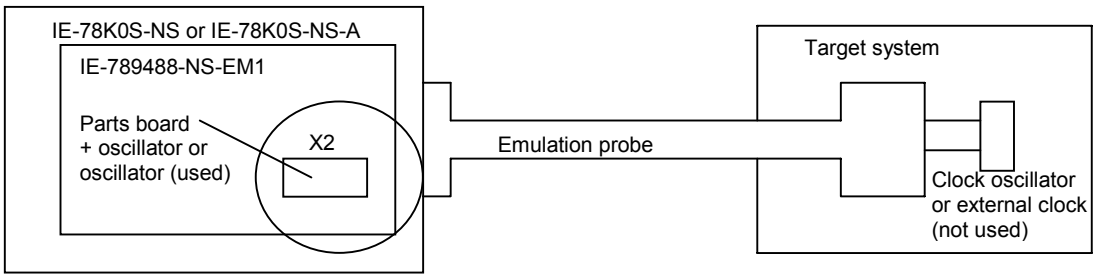


Remark The clock that is supplied by the IE-789488-NS-EM1's oscillator (encircled in the figure) is used.

(a) Subsystem clock

Remove the parts board (X2) that is already mounted on the emulation board, and mount either the parts board on which the resonator to be used is mounted or an oscillator.

Figure 3-7. When Using Clock Mounted by User (Subsystem Clock)

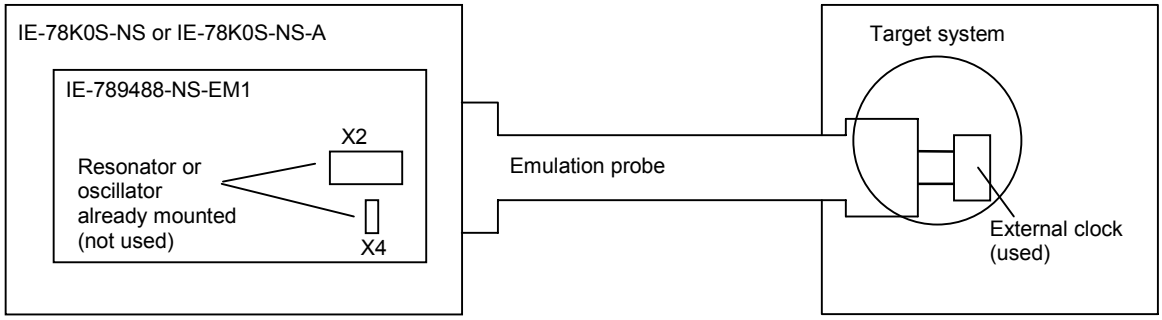


Remark The clock that is supplied by the IE-789488-NS-EM1's oscillator (encircled in the figure) is used.

(3) When using a pulse input from the target system

The external clock can be used for both the main system clock and subsystem clock on the target system via an emulation probe.

Figure 3-8. When Using Pulse Input from Target System



Remark The clock that is supplied by the external clock (encircled in the figure) is used.

3.5.2 Main system clock settings

The settings of the IE-789488-NS-EM1's main system clock are shown in Table 3-7.

Table 3-7. Main System Clock Settings

Frequency of Main System Clock		IE-789488-NS-EM1 X1Socket	CPU Clock Source Selection (ID78K0S-NS)
(1) Clock already mounted on emulation board	5.0 MHz	Oscillator	Internal
(2) Clock mounted by user	Other than 5.0 MHz	Oscillator assembled	
(3) Pulse input from the target system		Oscillator (not used)	External

Caution When using an external clock, open the configuration dialog box when starting the integrated debugger (ID78K0S-NS) and select "External" in the area (Clock) for selecting the CPU's clock source (this selects the user's clock).

Remark The IE-789488-NS-EM1's factory settings are those listed above under "when using clock already mounted on emulation board".

(1) When using clock already mounted on emulation board

When the IE-789488-NS-EM1 is shipped, a 5.0 MHz crystal oscillator is already mounted in the IE-789488-NS-EM1's X1 socket. When using the factory-set mode settings, there is no need to make any hardware settings.

When starting the integrated debugger (ID78K0S-NS), open the configuration dialog box and select "Internal" in the area (Clock) for selecting the CPU's clock source (this selects the emulator's internal clock).

(2) When using clock mounted by user

The settings of either (a) or (b) described in the following pages are required, depending on the type of clock to be used.

When starting the integrated debugger (ID78K0S-NS), open the configuration dialog box and select “Internal” in the area (Clock) for selecting the CPU’s clock source (this selects the emulator’s internal clock).

(a) When using a ceramic or crystal resonator

♦ Necessary items

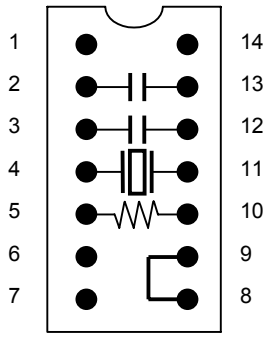
- Ceramic or crystal resonator
- Resistor Rx
- Solder kit
- Capacitor CA
- Capacitor CB

<Procedure>

<1> Solder the target ceramic or crystal resonator, resistor Rx, capacitor CA, and capacitor CB (all with suitable oscillation frequencies) onto the supplied parts board as shown below.

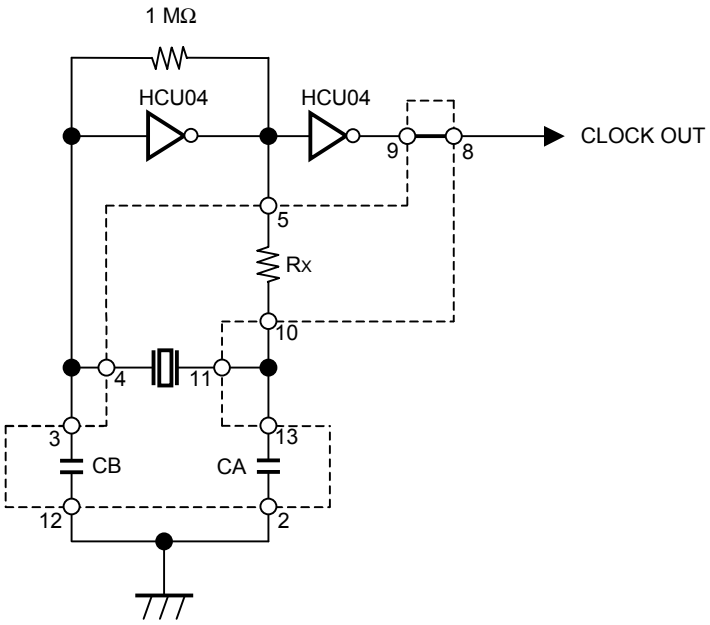
Figure 3-9. Connections on Parts Board (Main System Clock)

Parts board (X1)



Pin No.	Connection
2-13	Capacitor CA
3-12	Capacitor CB
4-11	Ceramic or crystal resonator
5-10	Resistor Rx
8-9	Shorted

Circuit Diagram



Remark The section enclosed by dotted lines indicates the section to be mounted on the parts board.

<2> Prepare the IE-789488-NS-EM1.

<3> Remove the crystal oscillator that is mounted in the IE-789488-NS-EM1's socket (X1).

<4> Connect the parts board (<1> above) to the socket (X1) from which the crystal oscillator was removed in <3>. Check the pin 1 mark to make sure the board is mounted in the correct direction.

<5> Make sure that the parts board is wired as shown in Figure 3-9 above.

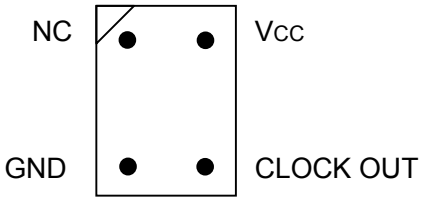
<6> Install the IE-789488-NS-EM1 in the IE-78K0S-NS or IE-78K0S-NS-A.

(b) When using a crystal oscillator

♦ Necessary items

• Crystal oscillator (with pin configuration as shown in Figure 3-10)

Figure 3-10. Crystal Oscillator (Main System Clock)



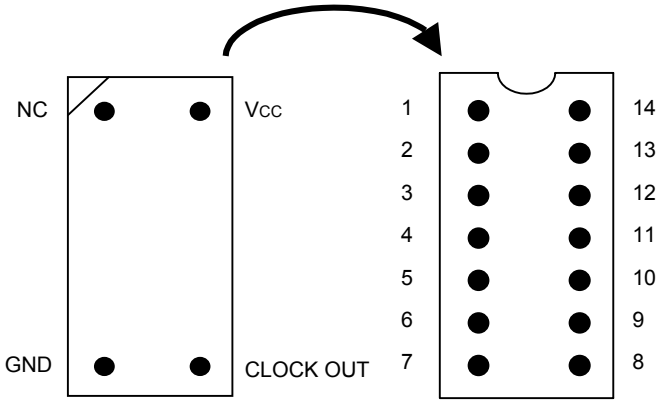
<Procedure>

<1> Prepare the IE-789488-NS-EM1.

<2> Remove the crystal oscillator from the X1socket on the IE-789488-NS-EM1.

<3> Mount the new crystal oscillator in the X1socket from which the crystal oscillator was removed in <2>. At this time, insert the crystal oscillator pin into the socket pin as indicated below.

Figure 3-11. Correspondence Between Crystal Oscillator and Socket (Main System Clock)



Crystal Oscillator Pin	Socket Pin No.
NC	1
GND	7
CLOCK OUT	8
Vcc	14

<4> Install the IE-789488-NS-EM1 in the IE-78K0S-NS or IE-78K0S-NS-A.

(3) When using a pulse input from the target system

There is no need to make any hardware settings.

When starting the integrated debugger (ID78K0S-NS), open the configuration dialog box and select “External” in the area (Clock) for selecting the CPU’s clock source (this selects the user clock).

3.5.3 Subsystem clock settings

The settings of the IE-789488-NS-EM1’s subsystem clock are shown in Table 3-8.

Table 3-8. Subsystem Clock Settings

Frequency of Subsystem Clock		IE-789488-NS-EM1	
		X2 Socket	SW1
(1) Clock already mounted on emulation board (XTC1)	32.768 kHz	6-8 shorted	2-3 shorted
(2) Clock mounted by user	Other than 32.768 kHz	Oscillator assembled	
(3) Pulse input from the target system		Oscillator not used	1-2 shorted

Caution Set JP1 to switch between the clock on the board and external clock when the power of the IE-78K0S-NS or IE-78K0S-NS-A is off.

Remark The IE-789488-NS-EM1’s factory settings are those listed above under “when using clock already mounted on emulation board”.

(1) When using clock already mounted on emulation board

When the IE-789488-NS-EM1 is shipped, a 32.768 kHz crystal resonator (X4) and parts board on which pins 6 and 8 are shorted are already mounted on the IE-789488-NS-EM1. Set the jumper (SW1) to 2-3 shorted.

There is no need to make any settings in the integrated debugger (ID78K0S-NS).

(2) When using clock mounted by user

The settings of either (a) or (b) described in the following pages are required, depending on the type of clock to be used. Set the jumper (JP1) on the IE-789488-NS-EM1 to 2-3 shorted.

There is no need to make any settings in the integrated debugger (ID78K0S-NS).

Caution When a clock mounted by the user is used, the clock to be used is not multiplied by 4 even if the use of the x4 circuit is specified. Instead, the clock on the board (X3: 131.072 kHz (4.194304/32)) is selected by the IE system.

(a) When using a ceramic or crystal resonator

♦ Necessary items

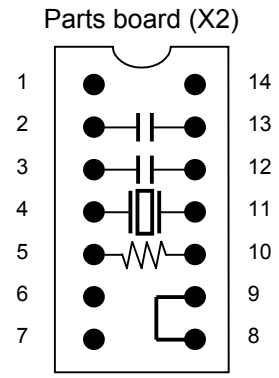
- Ceramic or crystal resonator
- Resistor Rx
- Capacitor CA
- Capacitor CB
- Solder kit

<Procedure>

<1> Prepare the IE-789488-NS-EM1.

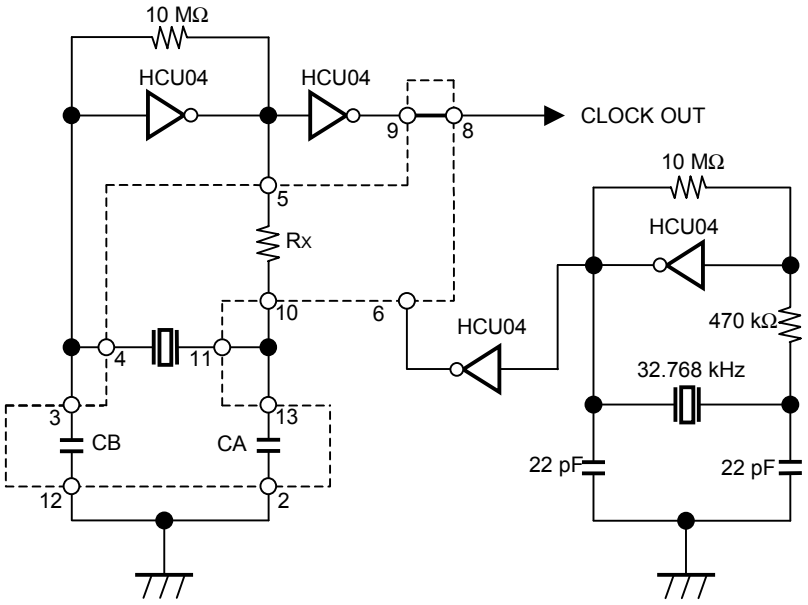
<2> Solder the target crystal resonator, resistor Rx, capacitor CA, and capacitor CB (all with suitable oscillation frequencies) onto the supplied parts board as shown below.

Figure 3-12. Connections on Parts Board (Subsystem Clock)



Pin No.	Connection
2-13	Capacitor CA
3-12	Capacitor CB
4-11	Ceramic or crystal resonator
5-10	Resistor Rx
8-9	Shorted

Circuit Diagram



Remark The section enclosed by dotted lines indicates the section to be mounted on the parts board.

<3> Make sure that the parts board (X2) is wired as shown in Figure 3-12 above.

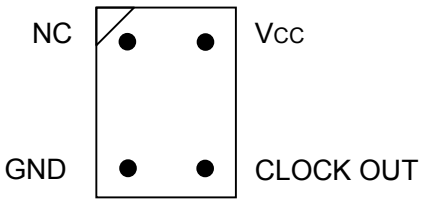
<4> Install the IE-789488-NS-EM1 in the IE-78K0S-NS or IE-78K0S-NS-A.

(b) When using a crystal oscillator

♦ Necessary items

• Crystal oscillator (with pin configuration as shown in Figure 3-13)

Figure 3-13. Crystal Oscillator (Subsystem Clock)



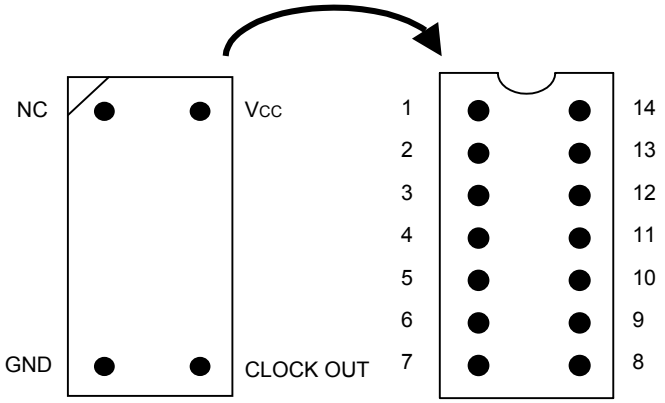
<Procedure>

<1> Prepare the IE-789488-NS-EM1.

<2> Remove the parts board from the X2 socket on the IE-789488-NS-EM1.

<3> Mount the crystal oscillator in the X2 socket from which the parts board was removed in <2>. At this time, insert the crystal oscillator pin into the socket pin as indicated below.

Figure 3-14. Correspondence Between Crystal Oscillator and Socket (Subsystem Clock)



Crystal Oscillator Pin	Socket Pin No.
NC	1
GND	7
CLOCK OUT	8
V_{CC}	14

<4> Install the IE-789488-NS-EM1 in the IE-78K0S-NS or IE-78K0S-NS-A.

(3) When using a pulse input from the target system

Set JP1 on the IE-789488-NS-EM1 to 1-2 shorted.

There is no need to make any settings in the integrated debugger (ID78K0S-NS).

Caution When a clock mounted by the user is used, the clock to be used is not multiplied by 4 even if the use of the x4 circuit is specified. Instead, the clock on the board (X3: 131.072 kHz (4.194304/32)) is selected by the IE system.

3.6 Settings of Subsystem Clock x4 Circuit

When using the subsystem clock x4 circuit, the settings vary depending on whether the target to be emulated is a flash memory version or a mask ROM version. Set as described below.

The settings to specify the use of the subsystem clock x4 circuit for a mask ROM version and a flash memory version are shown in Table 3-9.

- For the flash memory version, the setting can be made using bit 0 (SCT) of the SSCK register.
  For details, refer to the user's manual of the target device.
- For the mask ROM version, the setting can be made using a mask option.
  Set the jumper switches (SW3 and SW20).

Table 3-9. Subsystem Clock x4 Circuit Settings

<table>
<tr><th></th><th>Subsystem Clock</th><th colspan="4">Settings</th></tr>
<tr><td rowspan="2">Flash memory version</td><td>Original frequency of subsystem clock 32.768 kHz (changeable)</td><td rowspan="2">SW3</td><td rowspan="2">1-2 (default)</td><td rowspan="2">Bit 0 (SCT) of SSCK register</td><td>0</td></tr>
<tr><td>Subsystem clock x4 131.072 kHz (fixed)</td><td>1</td></tr>
<tr><td rowspan="2">Mask ROM version</td><td>Original frequency of subsystem clock 32.768 kHz (changeable)</td><td rowspan="2">SW3</td><td rowspan="2">2-3</td><td rowspan="2">SW20</td><td>2-3 (default)</td></tr>
<tr><td>Subsystem clock x4 131.072 kHz (fixed)</td><td>1-2</td></tr>
</table>

Cautions 1. Set SW when the power of the IE-78K0S-NS or IE-78K0S-NS-A is off.

2. The SW20 setting is valid only when the mask ROM version is selected (SW3 2-3 shorted).

3. Use SW20 with the default setting (2-3 shorted) when the flash memory version is selected (SW3 1-2 shorted). This can be changed using bit 0 (SCT) of the SSCK register. For details, refer to the user's manual of the target device.

4. The setting to use the subsystem clock x4 circuit is disabled when using the external clock.

3.7 Setting of Mask Option

3.7.1 Mask option of port 5

The mask option of P50 to P53 can be used to connect a 30 kΩ pull-up resistor using a DIP switch (SW2).

Set the mask options in the mask option setting dialog box of the integrated debugger (ID78K0S-NS). This setting is not necessary when reading a project file because the read contents are reflected in the mask option setting dialog box.

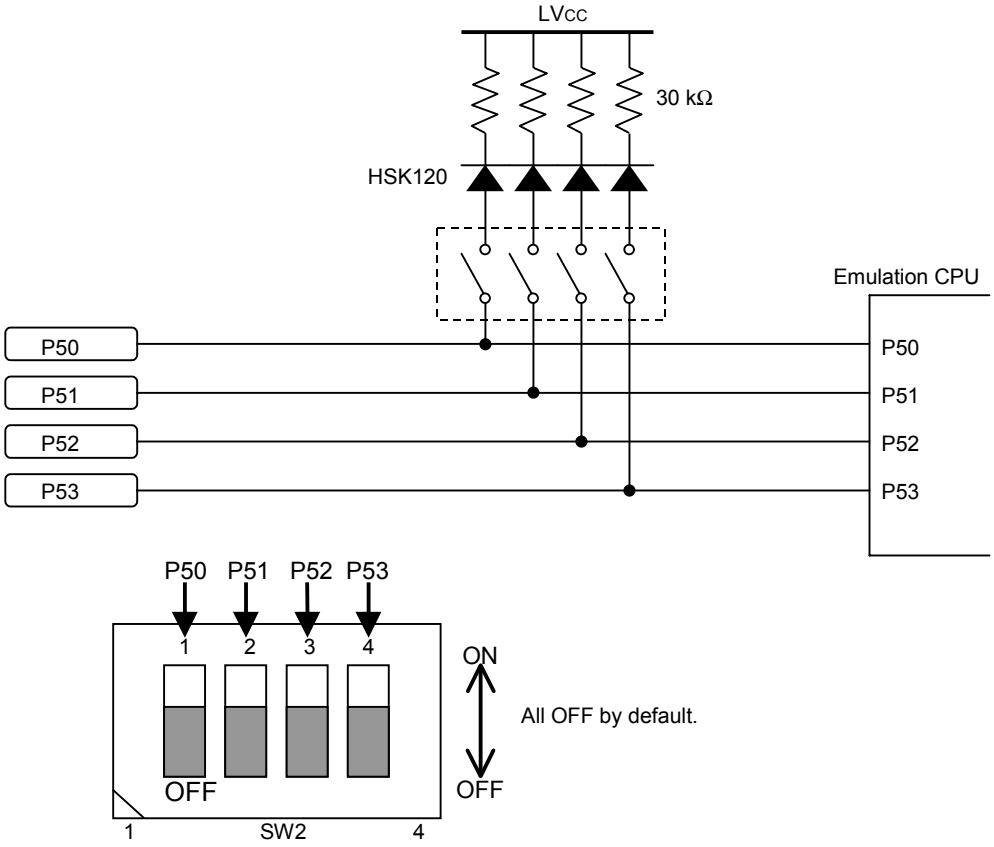
See ID78K Series Integrated Debugger Ver. 2.30 or Later User's Manual (U15185E) for details of how to use mask options.

Table 3-10. SW2 Settings

	SW2			
	1	2	3	4
Connected to:	P50	P51	P52	P53

The pins are pulled up to the target voltage (LV_{CC}) when the DIP switch is turned on, and disconnected when the DIP switch is turned off. Set ports with no connection destination to OFF.

Figure 3-15. Mask Option Setting of Port 5



3.7.2 Mask option for pin functions

In the IE-789488-NS-EM1, ports and segments can be switched using jumper switch.

The jumper switch settings are shown in Table 3-11.

Table 3-11. Port/Segment Switching Setting

Port/Segment	Jumper Switch	Setting
P87	SW8	1-2
S27		1-3, 2-4 (default)
P86	SW9	1-2
S26		1-3, 2-4 (default)
P85	SW10	1-2
S25		1-3, 2-4 (default)
P84	SW11	1-2
S24		1-3, 2-4 (default)
P83	SW12	1-2
S23		1-3, 2-4 (default)
P82	SW13	1-2
S22		1-3, 2-4 (default)
P81	SW14	1-2
S21		1-3, 2-4 (default)
P80	SW15	1-2
S20		1-3, 2-4 (default)
P73	SW19	1-2
S19		1-3, 2-4 (default)
P72	SW18	1-2
S18		1-3, 2-4 (default)
P71	SW17	1-2
S17		1-3, 2-4 (default)
P70	SW16	1-2
S16		1-3, 2-4 (default)

Cautions 1. Segments are selected by default (1-3, 2-4 shorted).

2. Set SW when the power of the IE-78K0S-NS or IE-78K0S-NS-A is off.

3. When ports are selected, set SW to 3-4 open (if set to 3-4 shorted, the waveforms of the other LCD pins are distorted).

4. In the flash memory version, set jumper switch in addition to setting the port function registers (PF7 and PF8).

3.7.3 Mask option for subsystem clock x4 circuit

The settings to specify the use of the subsystem clock x4 circuit for a mask ROM version are shown below.

The mask option settings are shown in Table 3-12.

Table 3-12. Subsystem Clock x4 Circuit Mask Option Setting

Function	Location	Setting
Mask ROM version selection	SW3	2-3
Subsystem clock x4 (SCTON = 1)	SW20	1-2
Original frequency of subsystem clock (SCTON = 0)		2-3 (default)

Caution Set SW when the power of the IE-78K0S-NS or IE-78K0S-NS-A is off.

3.8 External Trigger

To set an external trigger, connect it to the IE-789488-NS-EM1's check pin, EXTOUT pin and EXTIN pin.
See the IE-78K0S-NS User's Manual (U13549E) or IE-78K0S-NS-A User's Manual (U15207E) for descriptions of usage and pin characteristics.

(1) EXTOUT

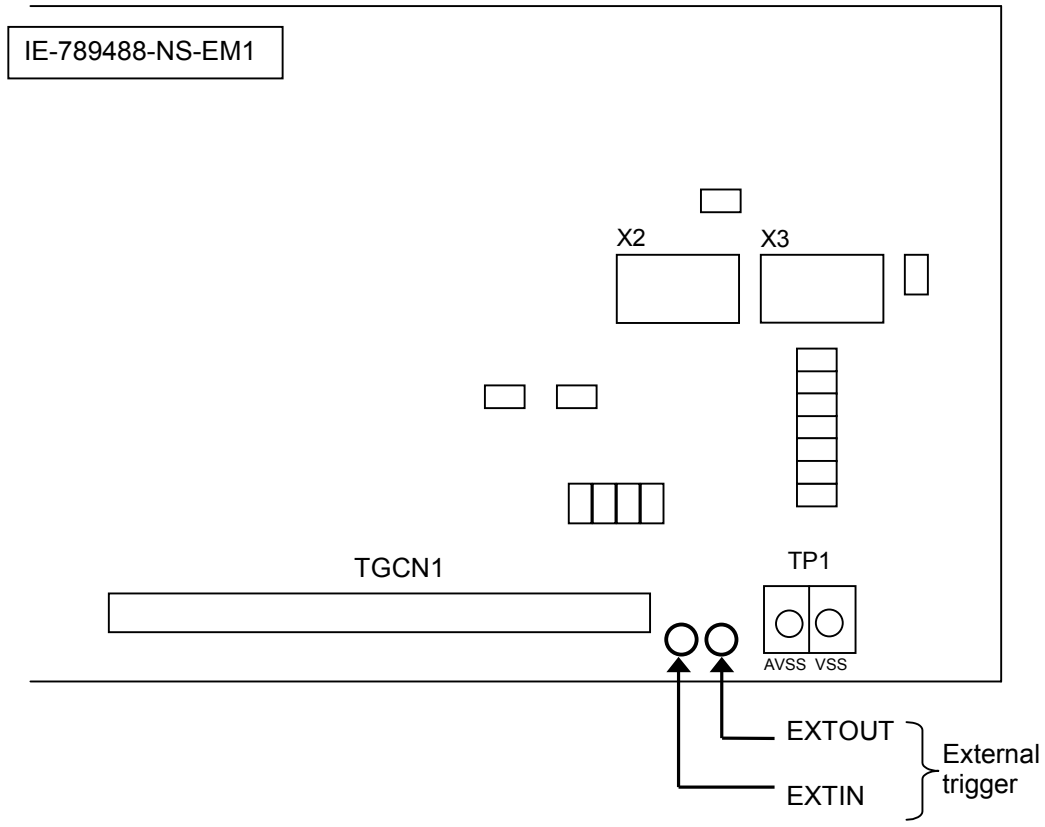
A low-level pulse is output from the IE-789488-NS-EM1's EXTOUT pin for 1.3 μs upon the occurrence of a break event.

Caution Because this is an open-drain output, a pull-up resistor should be connected on the target system.

(1) EXTIN

An event signal can be input from the IE-789488-NS-EM1's EXTIN pin. Input a high-level pulse signal for 2 CPU operating clocks or longer.

Figure 3-16. External Trigger Input Position



CHAPTER 4 DIFFERENCES BETWEEN TARGET DEVICES AND TARGET INTERFACE CIRCUITS

This chapter describes differences in electrical characteristics between the target device and the target interface circuit.

The target interface circuit of the IE system consists of an emulation CPU, TTL, CMOS-IC, and other emulation circuits. Differences in electrical characteristics between the target device and the target interface circuit occur due to the existence of a protection circuit.

(1) Signals input/output to/from the pin emulator (target voltage operation)
(2) Signals input from the target system via a gate
(3) Signals related to LCD
(4) Other signals

The differences with the target device are classified into the following (1) to (4) and explained in the following pages. Alternate function pins are treated in the same way. There is no circuit in the IE system.

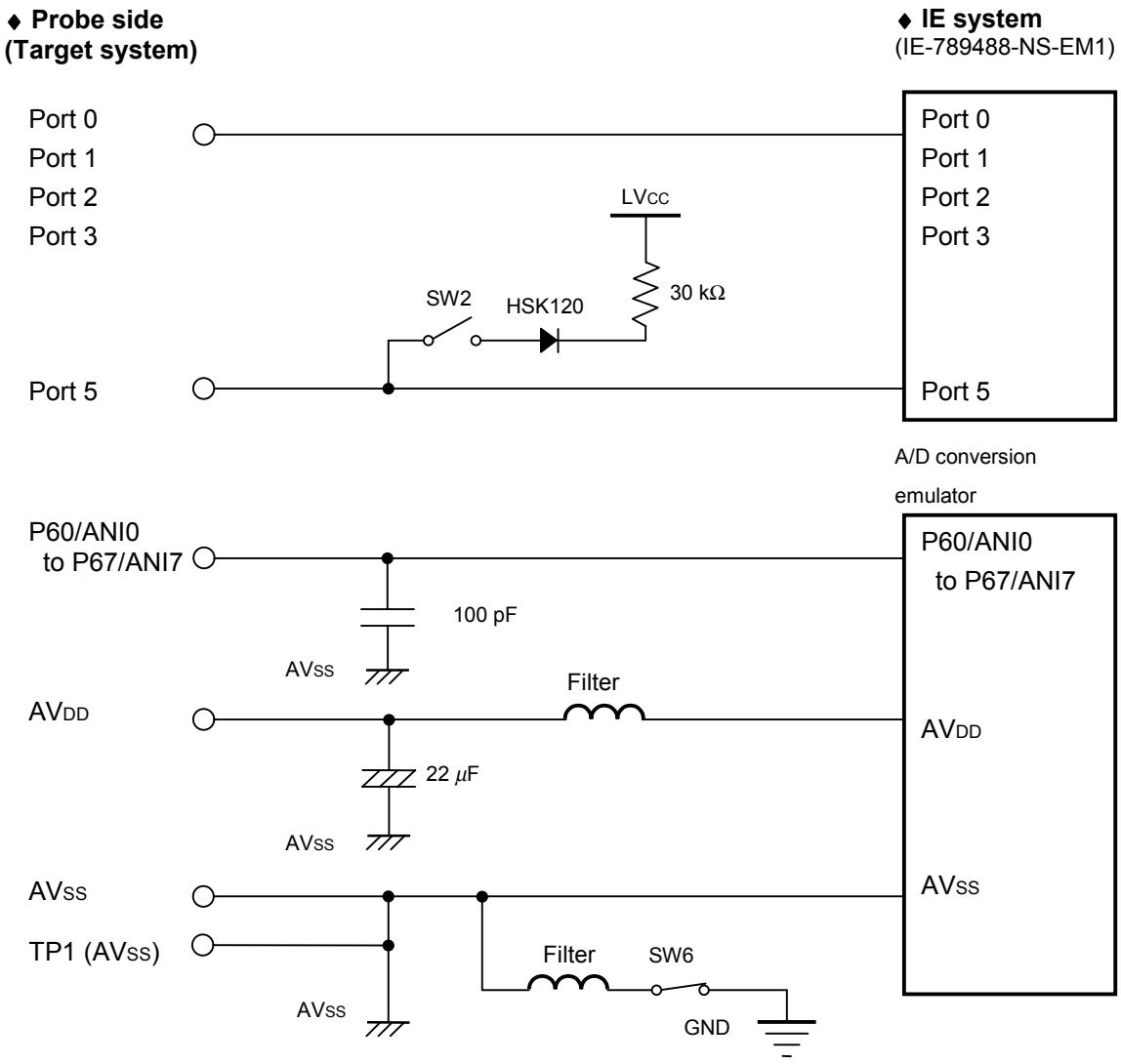
(1) Signals directly input/output to/from the pin emulator (target voltage operation)

Refer to Figure 4-1 Equivalent Circuit of Emulation Circuit (1). A 1 MΩ pull-down resistor is connected to signals related to ports 0 and 1 in the IE-78K0S-NS and IE-78K0S-NS-A. A 30 kΩ pull-up resistor is connected to signals related to ports 5 using the switch (SW2).

- Signals related to port 0
- Signals related to port 1
- Signals related to port 2
- Signals related to port 3
- Signals related to port 5
- Signals related to port 6/ANI
- AV_{DD} pin
- AV_{SS} pin

  The AV_{SS} pin from the target system can be connected to the pin board (TP1) to reinforce GND. The digital and analog ground can be isolated by the switch (SW6).

Figure 4-1. Equivalent Circuit of Emulation Circuit (1)



(2) Signals input from the target system via a gate

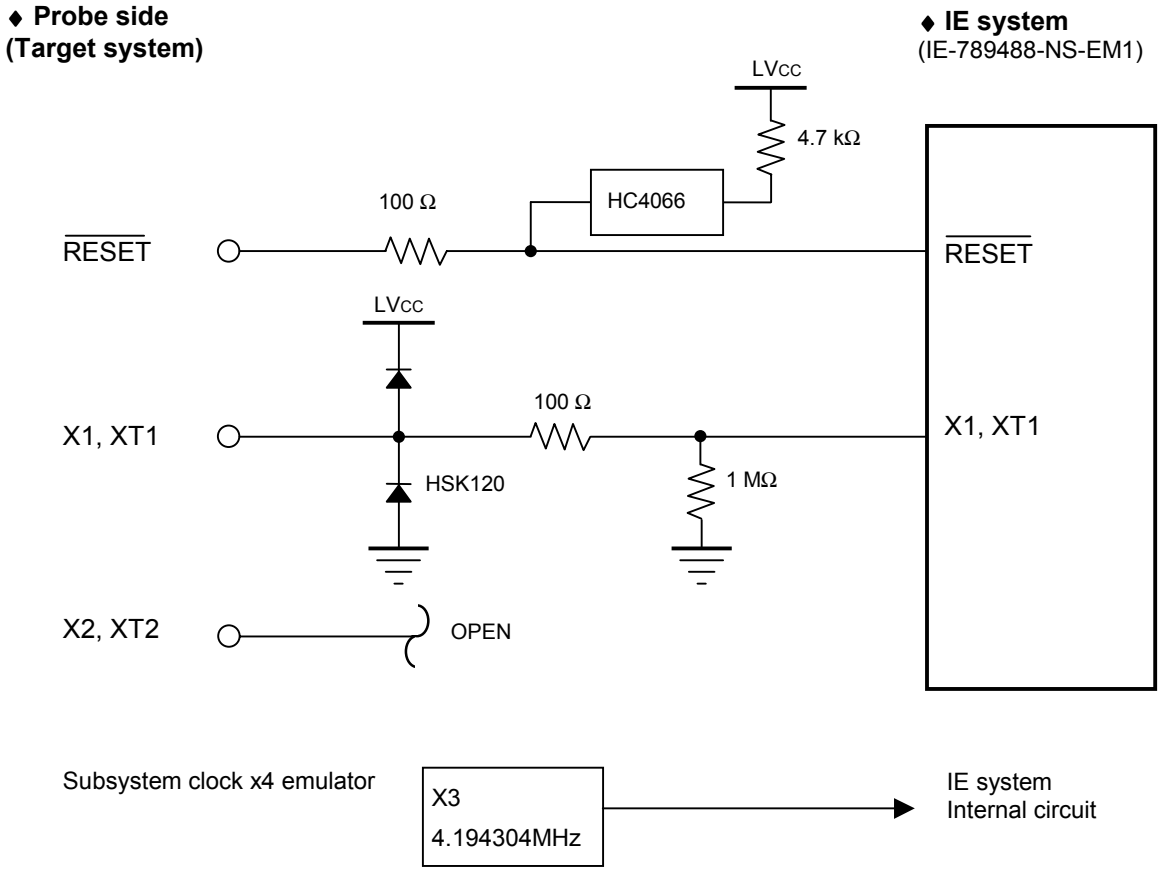
Since the following signals are input via a gate of the emulation device, their timing shows a delay compared to that of the μPD789479, 789489 Subseries. Refer to Figure 4-2 Equivalent Circuit of Emulation Circuit (2).

- Signals related to $\overline{\text{RESET}}$
- Signals related to clock input

  The XT1 pin is not connected to the x4 circuit.

  The IE-789488-NS-EM1 does not use the X2 and XT2 pins.

Figure 4-2. Equivalent Circuit of Emulation Circuit (2)



(3) Signals related to LCD

Refer to Figure 4-3 Equivalent Circuit of Emulation Circuit (3).

- Signals related to port 7/S16 to S19

  Port/segment can be switched via setting S16 to S19.
- Signals related to port 8/S20 to S27

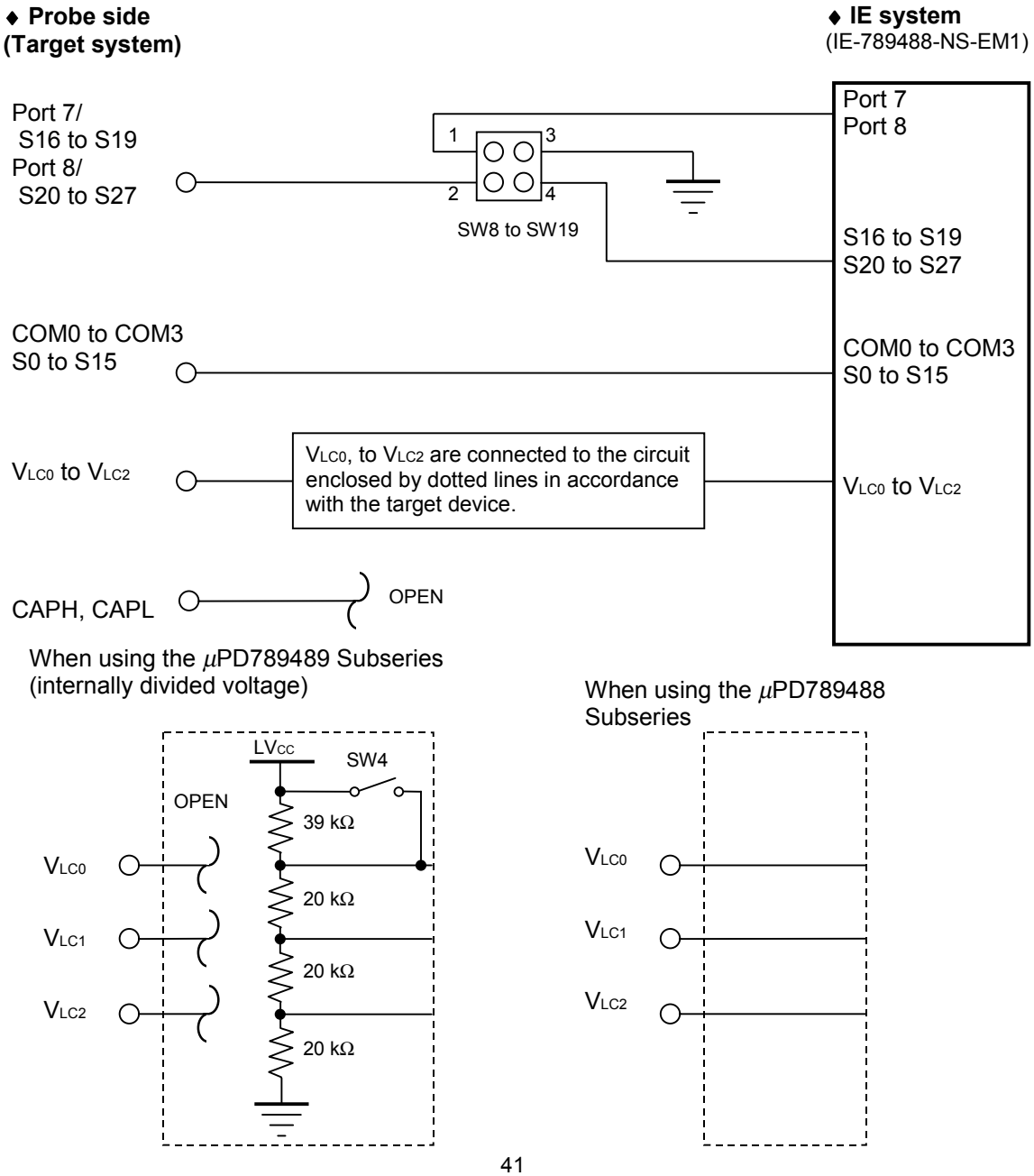
  Port/segment can be switched via setting S8 to S15.
- Signals related to LCD (COM0 to COM3)

  The target subseries can be switched by V_{LC0} to V_{LC2} by setting J9.

  Panel voltage of the μPD789489 Subseries can be set by setting SW4
- CAPH, CAPL signals (μPD789489 Subseries only)

  The IE-789488-NS-EM1 does not use these signals.

Figure 4-3. Equivalent Circuit of Emulation Circuit (3)



(4) Other signals

Refer to Figure 4-4 Equivalent Circuit of Emulation Circuit (4).

- V_{DD} pin

When the target system is connected, the target interface power (LV_{CC}) is supplied from the V_{DD} pin.

When the target system is connected, the emulator operates with the internal supply voltage (5 V).

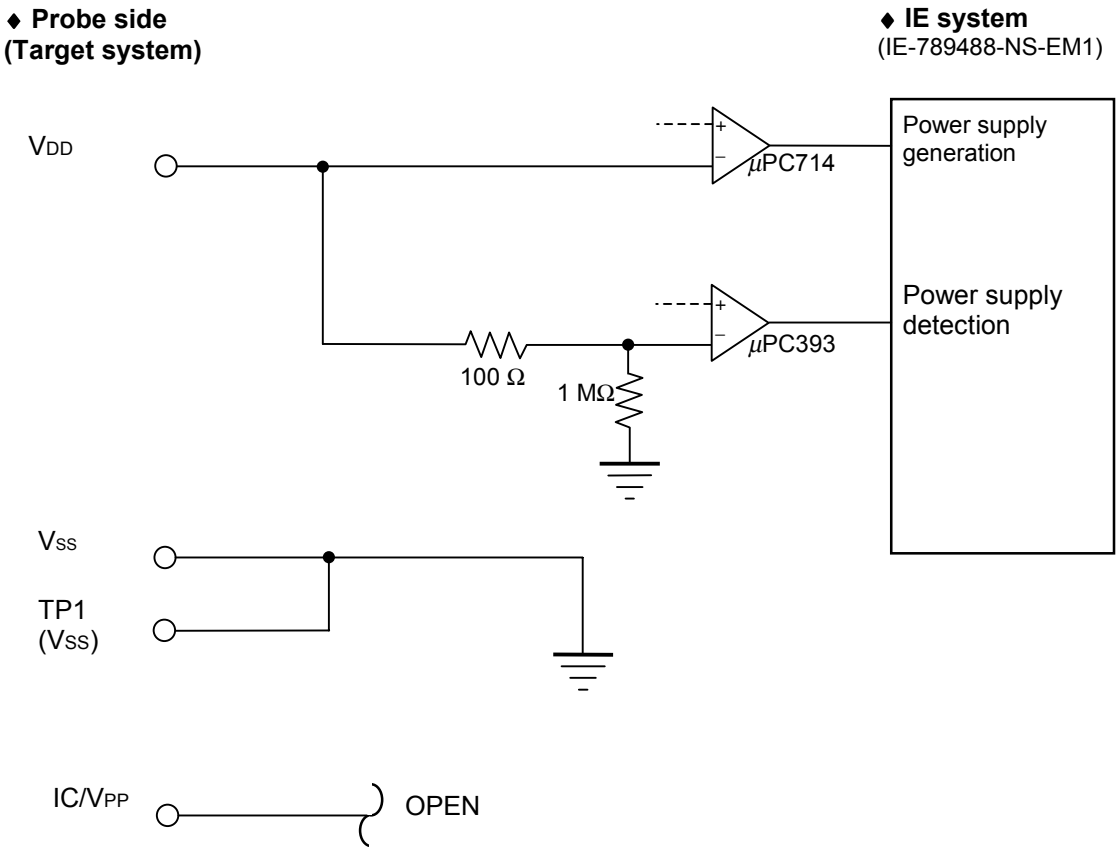
- V_{SS} pin

The V_{SS} pin is connected to GND inside the IE-789488-NS-EM1. The V_{SS} pin from the target system can be connected to the pin board (TP1) to reinforce GND.

- IC/V_{PP} pin

The IE-789488-NS-EM1 does not use the IC/V_{PP} pin.

Figure 4-4. Equivalent Circuit of Emulation Circuit (4)



CHAPTER 5 CAUTIONS

This chapter describes differences between the target device and the IE system specifications.

The emulation circuit of the IE system consists of an EMULATION CPU, TTL, CMOS-IC, and other circuits. Therefore, there are differences between the target device and the IE system specifications.

- Emulation specification when the x4 subsystem clock is selected (1)

  When the x4 subsystem clock is selected, $f_{XTT}/2$ is fixed to 131.072 kHz and f_{XT} is fixed to 32.768 kHz, and these values cannot be changed. Therefore, “using the clock mounted by user” or “using the external clock” cannot be selected.

- Emulation specification when the x4 subsystem clock is selected (2)

  The x4 subsystem clock cannot be stopped by HALT. As a result, the IE-789488-NS-EM1 starts operation one subsystem clock earlier after HALT is released.

- Emulation specification for the port/segment switching mask option

  The port and segment cannot be switched even if the port function registers (PF7 and PF8) are set so.

  In addition to the port function register settings, set SW8 to SW19 in the IE-789488-NS-EM1. For details of the SW settings, refer to **3.7.2 Mask option for pin functions**.

- LCD function specification when emulating the μPD78948x (1)

  It is possible to access bit 6 (VAON0) of LCD display mode register 0 (LCDM0), but the access is not valid. The voltage boost operation is enabled by setting the 9489 mode (J9: 2-3). For details of the jumper setting, refer to **3.3.1 Jumper setting for selecting subseries**.

- LCD function specification when emulating the μPD78948x (2)

  It is possible to access bit 0 (GAIN) of LCD voltage boost control register 0 (LCDVA0), but the access is not valid. The voltage selected by the SW4 setting (LCD panel voltage setting) is always used as the panel voltage. For details of the SW setting, refer to **3.3.2 LCD emulation setting for μPD789489 Subseries**.

APPENDIX A EMULATION PROBE PIN CORRESPONDENCE TABLE

Table A-1. Pin Correspondence of Emulation Probe

Emulation Probe Pin No.	TGCN1 Pin No.	Emulation Probe Pin No.	TGCN1 Pin No.
1	114	31	60
2	113	32	55
3	108	33	56
4	107	34	49
5	104	35	50
6	103	36	45
7	100	37	46
8	99	38	41
9	94	39	42
10	93	40	35
11	30	41	8
12	29	42	7
13	24	43	14
14	23	44	13
15	20	45	18
16	19	46	17
17	16	47	22
18	15	48	21
19	10	49	28
20	90	50	27
21	37	51	92
22	43	52	91
23	44	53	98
24	47	54	97
25	48	55	102
26	51	56	101
27	52	57	106
28	57	58	105
29	58	59	112
30	59	60	111
61	83	71	62
62	77	72	65
63	78	73	66
64	73	74	71
65	74	75	72
66	69	76	75
67	70	77	76
68	63	78	79
69	64	79	80
70	61	80	85

Remarks 1. NP-H80GK-TQ, NP-80GK, NP-H80GC-TQ, NP-80GC-TQ, and NP-80GC are products of Naito Densei Machida Mfg. Co., Ltd.

2. The numbers in the Emulation Probe Pin No. column refer to the corresponding pin number of the emulation probe.

APPENDIX B CAUTIONS ON TARGET SYSTEM DESIGN

The following shows a diagram of the connection conditions between the emulation probe, conversion connector, and conversion socket. Design your system making allowances for conditions such as the form of parts mounted on the target system as shown below.

Table B-1. Distance from ICE to Conversion Socket

Emulation Probe	Conversion Socket	Distance from ICE to Conversion Socket
NP-80GC	EV-9200GC-80	170 mm
NP-80GC-TQ	TGC-080SBP	170 mm
NP-H80GC-TQ		370 mm
NP-80GK	TGK-080SDP	170 mm
NP-H80GK-TQ		370 mm

Figure B-1. Distance from ICE to Conversion Socket (1/2)

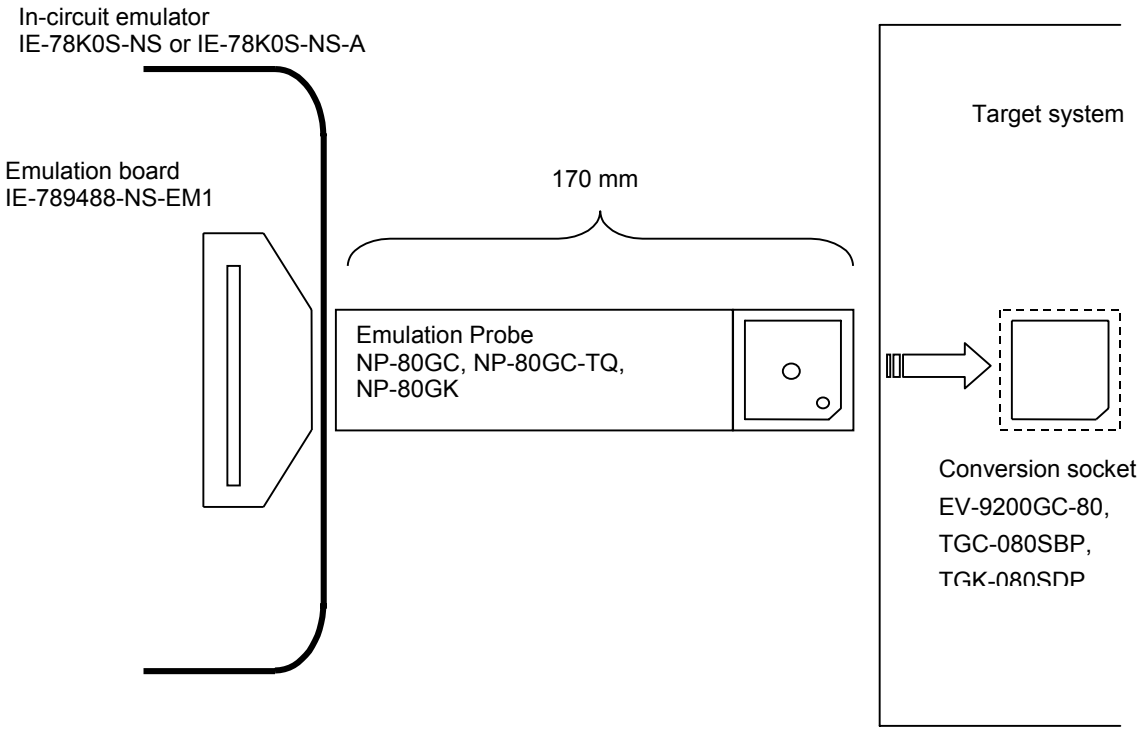


Figure B-1. Distance from ICE to Conversion Socket (2/2)

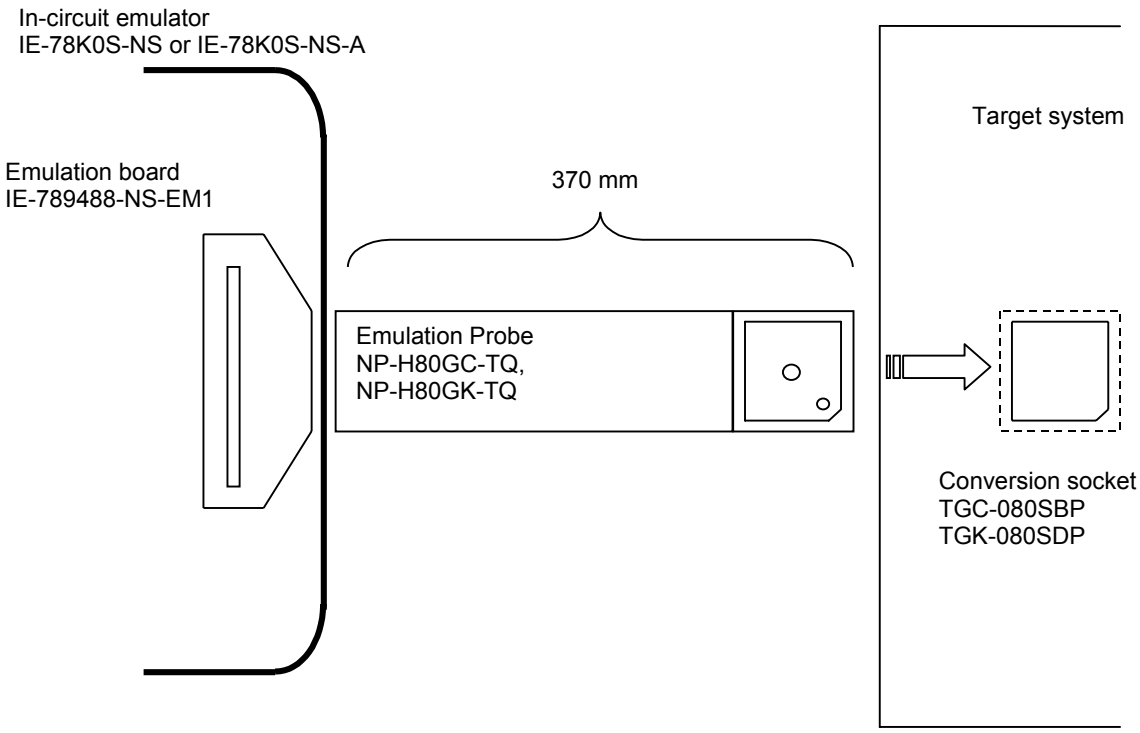


Figure B-2. Conditions for Target System Connection (1)

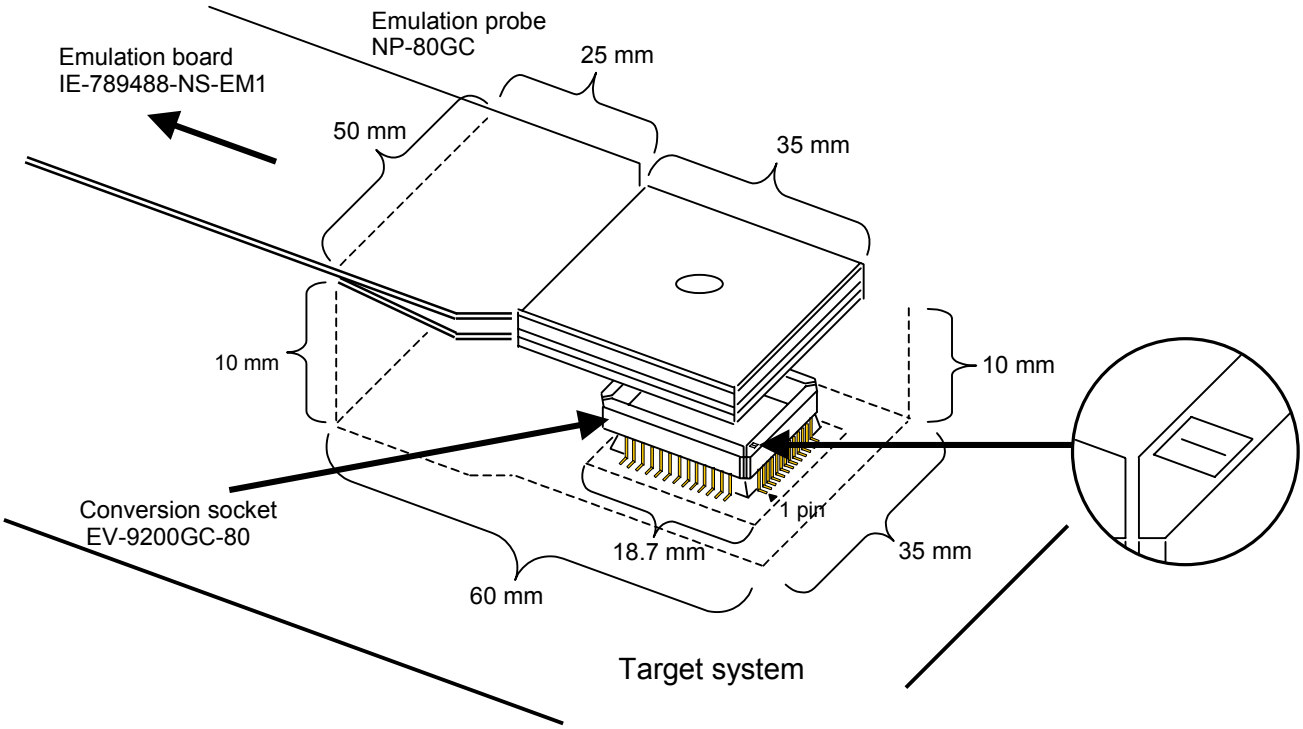


Figure B-3. Conditions for Target System Connection (2)

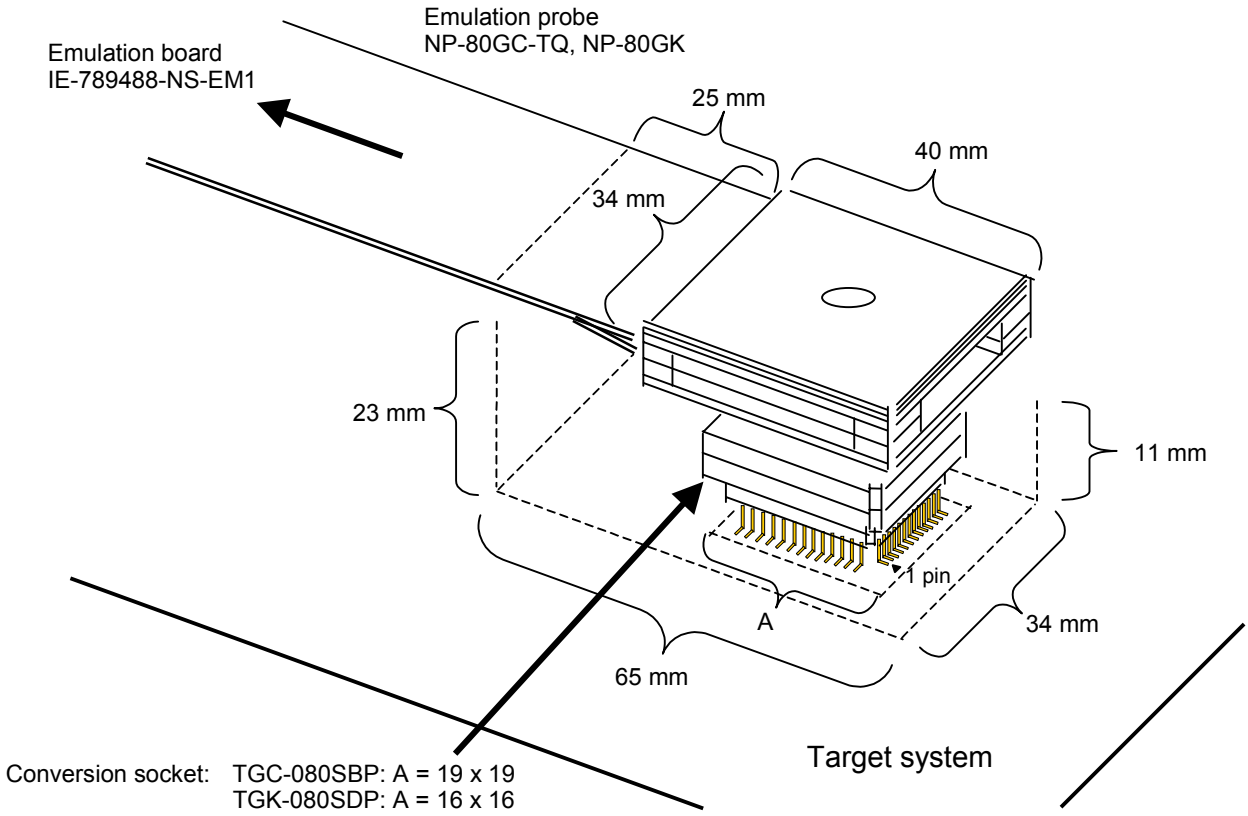
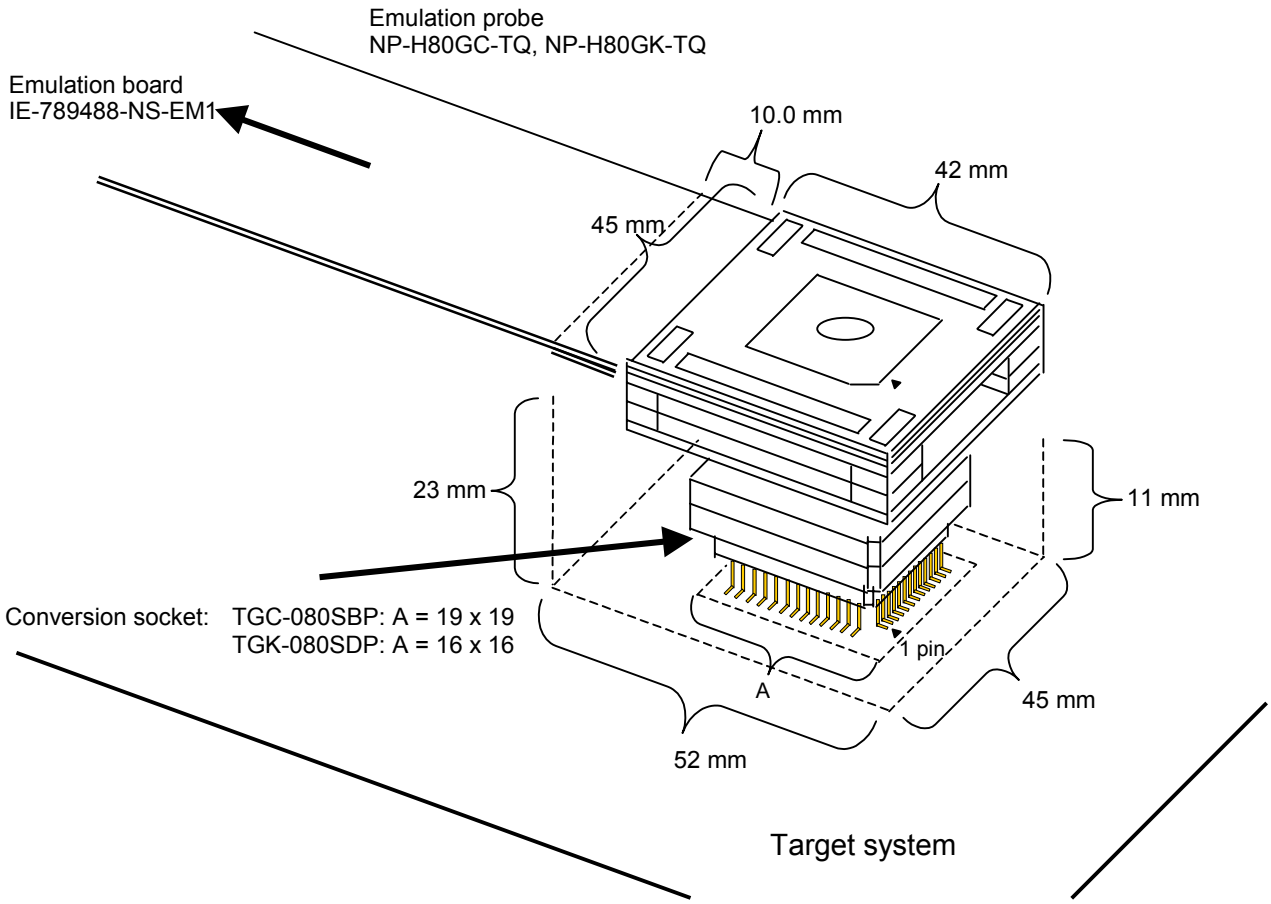


Figure B-4. Conditions for Target System Connection (3)



Remark NP-H80GK-TQ, NP-80GK, NP-H80GC-TQ, NP-80GC-TQ, and NP-80GC are products of Naito Densei Machida Mfg. Co., Ltd.

TGK-080SDP and TGC-080SBP are products of Tokyo Eletech Corporation.