

CUSTOMER NOTIFICATION

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IE-780862-NS-EM1
(Control Code A, B, C)
Operating Precautions

Be sure to read this document before using the product.

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Notes on Using IE-780862-NS-EM1

1. Product Version

Product name: IE-780862-NS-EM1

Control Code ^{Note}	Remark
A	–
B	–
C	–

Note The “control code” is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased. If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.

2. Product History

No.	Bugs and Changes/Additions to Specifications	Control Code		
		A	B	C
1	Bug in port 1	×	√	√
2	Bug in watchdog timer in standby mode	×	×	√

×: Applicable, √: Not applicable or already corrected

3. Details of Bugs and Added Specifications

No.1 Bug in port 1

[Description]

When P1 is used as an alternate-function output port (SCK10, SO10, TOH1, MCGO, or TOH0),

(1) the pin level of the alternate function is read when the value of P1 is read.

(The value of P1 is correctly read when P1 is used for other than the alternate function.)

(2) if data is written to a P1 bit not being used as an alternate-function output pin using a bit manipulation instruction (SET1 or CLR1), the output level of the alternate function may be fixed to high level.

[Workaround]

(1) There is no workaround.

(2) Use the MOV instruction.

[Action]

This bug has been corrected in IE-780862-NS-EM1 control code B.

No.2 Bug in watchdog timer in standby mode

[Description]

The watchdog timer operation does not stop even if SoftwareStop (Ring-OSC can be stopped by software) is set for the mask option LowspeedRing in the debugger and the HALT or STOP instruction is executed, as long as the operation clock to the watchdog timer does not stop. As a result, a reset signal is generated.

[Workaround]

There is no workaround. This bug has been corrected in IE-780862-NS-EM1 control code C.

4. Restrictions

No.1 Restrictions on port function

[Description]

- (1) The initial values of P23 to P20 are undefined when the IE-780862-NS-EM1 is not connected to the target system.
- (2) The output timing (write timing) of the port is 1 CPUCLK earlier than that in the real chip.
(1 CPUCLK: CLK after PCC elapsed)

[Workaround]

There is no workaround.

No.2 Restrictions on A/D converter

[Description]

- (1) The power-fail function of the A/D converter cannot be emulated using the IE-780862-NS-EM1.
- (2) The read time taken for the response by the A/D converter retry function is different from that of the real chip. (No waits are generated by a retry request in the IE system.)
- (3) The operation guaranteed range is 3.0 to 5.5 V.
- (4) Bit 0 of the ADM register cannot be read.
- (5) The least significant bit of the A/D conversion result register (ADCR) is fixed to 0 when bit 5 (FR2) of the A/D converter mode register (ADM) is set to 1.

[Workaround]

There is no workaround.

No.3 Restrictions on clock function

[Description]

- (1) Set the external/internal main clock in the Configuration dialog box of the debugger when the debugger is started. After that, do not change the setting.
- (2) The initial value of the SFR PCC differs between the target device and IE system.
Target device: 00H IE system: 04H

[Workaround]

- (1) There is no workaround.
- (2) Set 00H when the target device is started or reset.

No.4 Handling of the $\overline{\text{RESET}}$ pin differs from that in the target device.

[Description]

The handling of the $\overline{\text{RESET}}$ pin differs from that in the target device.

Target device: Do not pull up

IE system: Pull up with 4.7 k Ω in the IE system

[Workaround]

There is no workaround.

Correction is planned in line with upgrading the integrated debugger ID78K0-NS.

No.5 Even if RESET is set to MASK in the Configuration dialog box of the ID78K0-NS, the values of the RESF, LVIM, and LVIS registers are initialized when a reset is input from the target system to the IE system.

[Workaround]

There is no workaround.

No.6 The values of the RESF, LVIM, and LVIS registers cannot be initialized using the CPU reset button of the integrated debugger ID78K0-NS.

[Workaround]

The initialization conditions of the RESF, LVIM, and LVIS registers are as follows.

(1) Initialization conditions of the RESF register

- Reset from the target system
- Internal reset by comparing the power supply voltage and the detected voltage of the POC circuit

(2) Initialization conditions of the LVIM and LVIS registers

- Reset from the target system
- Internal reset by comparing the power supply voltage and the detected voltage of the POC circuit
- Clock monitor reset using the clock monitor emulation switch (SW2)
- Reset by the watchdog timer

No.7 Since a 10 to 100 k Ω pull-up resistor is connected to the port pins, port pins become +5 V high level (input state) between when power is applied to the IE system and when the ID78K0-NS is activated (the debug screen is displayed).

Relevant port pins

- P00 to P02
- P20 to P23
- AV_{REF}

Leakage current value of each port pin: 3 μ A max.

[Workaround]

There is no workaround.

5. Cautions

Use the IE-78K0-NS (control code L or later) or IE-78K0-NS-A (control code E or later). Even if using the product with the latest control code, emulation cannot be performed correctly (the integrated debugger may hang up) when used in combination with IE-78K0-NS control code A to C.

NEC Electronics will provide separate support for IE-78K0-NS control code A to C, so please contact an NEC Electronics sales representative or distributor.

The “control code” is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.