CUSTOMER NOTIFICATION

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IE-780354-NS-EM1

Preliminary User's Manual

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Major Revisions in This Edition

Ver.	Page	Description
1st	-	Newly created.
2nd	p. 25	Change of chapter 5 title from Cautions to Restrictions Addition of No.5 item
	p. 26	Addition of CHAPTER 6 CAUTIONS

INTRODUCTION

Product Overview

The IE-780354-NS-EM1 is designed to be used with the IE-78K0-NS or IE-78K0-NS-A to debug the following target devices that belong to the 78K0 Series of 8-bit single-chip microcontrollers.

- μPD780343, 780343Y, 780344, 780344Y, 780353, 780353Y, 780354, 780354Y
- μPD78F0354, 78F0354Y

Target Readers

This manual is intended for engineers who will use the IE-780354-NS-EM1 with the IE-78K0-NS or IE-78K0-NS-A to perform system debugging.
Engineers who use this manual are expected to be thoroughly familiar with the target device's functions and use methods and to be knowledgeable about debugging.

Organization

When using the IE-780354-NS-EM1, refer to not only this manual (supplied with the IE-780354-NS-EM1) but also the manual that is supplied with the IE-78K0-NS or IE-78K0-NS-A.
When using the IE-78K0-NS in combination with the IE-78K0-NS-PA, it is functionally equal to the IE-78K0-NS-A. In such a case, therefore, read the IE-78K0-NS-A in this document as IE-78K0-NS + IE-78K0-NS-PA.

IE-78K0-NS(-A) User's Manual	IE-780354-NS-EM1 User's Manual
• Basic specifications • System configuration • External interface functions	• General • Part names • Installation • Differences between target devices and target interface circuits

Purpose

This manual's purpose is to explain various debugging functions that can be performed when using the IE-780354-NS-EM1.

Terminology The meanings of certain terms used in this manual are listed below.

Term	Meaning
Emulation device	This is a general term that refers to the device in the emulator that is used to emulate the target device. It includes the emulation CPU.
Emulation CPU	This is the CPU block in the emulator that is used to execute user-generated programs.
Target device	This is the device (a real chip) that is the target for emulation.
Target system	This includes the target program and the hardware provided by the user. When defined narrowly, it includes only the hardware.
IE system	This refers to the combination of the IE-78K0-NS or IE-78K0-NS-A and the IE-780354-NS-EM1.

Conventions

Data significance: Higher digits on the left and lower digits on the right

Note: Footnote for item marked with **Note** in the text

Caution: Information requiring particular attention

Remark: Supplementary information

CONTENTS

CHAPTER 1 GENERAL

The IE-780354-NS-EM1 is a development tool for efficient debugging of hardware or software when using one of the following target devices that belong to the 78K0 Series of 8-bit single-chip microcontrollers.

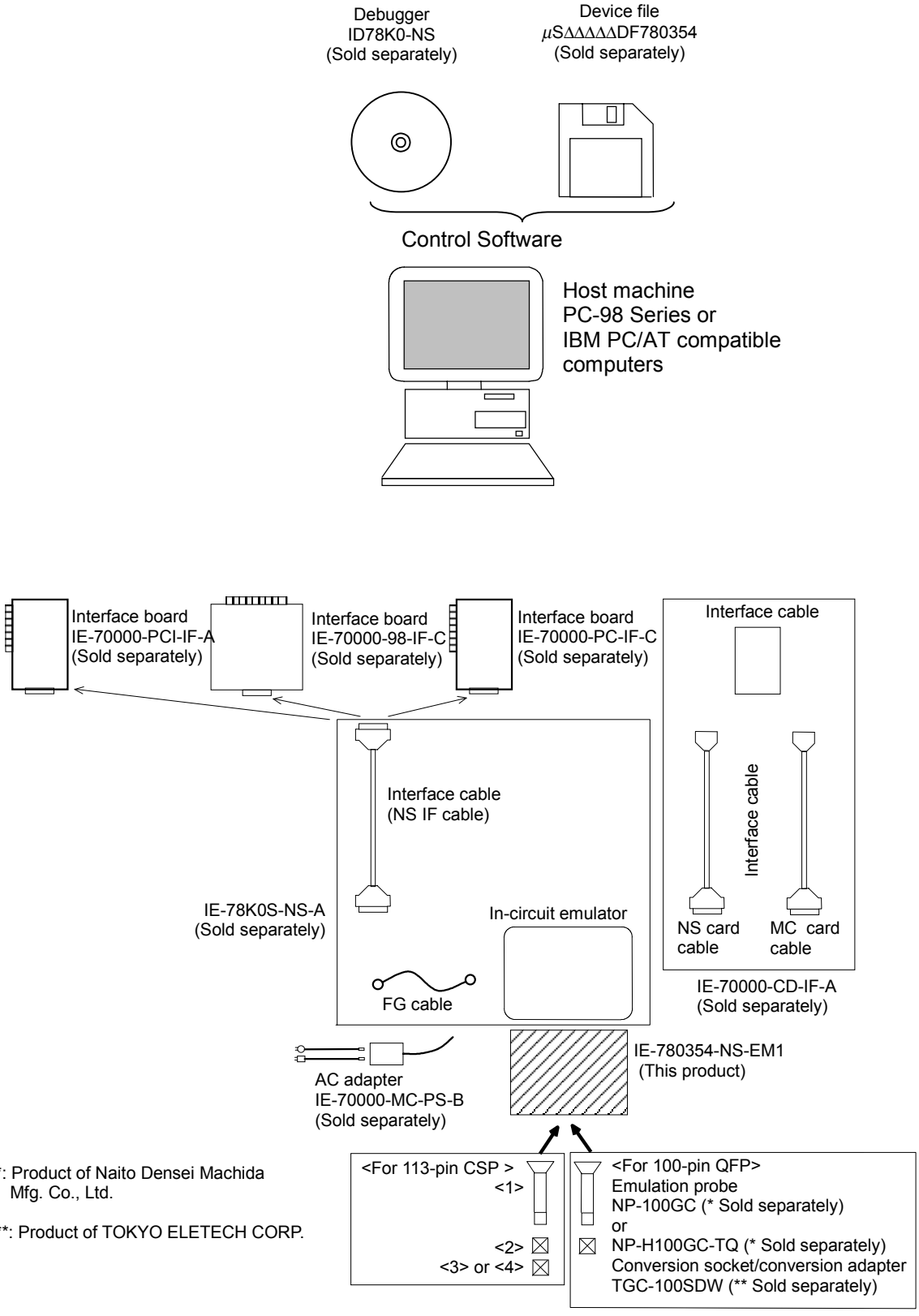
This chapter describes the IE-780354-NS-EM1 system configuration and basic specifications.

- Target device
  - μPD780343, 780343Y, 780344, 780344Y, 780353, 780353Y, 780354, 780354Y
  - μPD78F0354, 78F0354Y

1.1 System Configuration

Figure 1-1 illustrates the IE-780354-NS-EM1 system configuration.

Figure 1-1. System Configuration



Refer to the following pages for the configuration of the emulation probe for 113-pin CSP (<1>) and the conversion socket/conversion adapter (<2>, <3>, <4>).

Part numbers for the emulation probe for 113-pin CSP (<1>) and conversion socket/conversion adapter (<2>, <3>, <4>) are shown below.

<1> NP-113F1-DA3

<2> LSPACK113A1110NO1

<3> CSSOCKET113A1110NO1 (with guide pin)

<4> CSSOCKET113A1110NO1N (without guide pin)

<2> and <3> are supplied with <1>. <1> is a product of Naito Densei Machida Mfg. Co., Ltd.
<2>, <3>, <4> are products of TOKYO ELETECH CORPORATION.

The following socket set (Naito Densei Machida Mfg. Co., Ltd.) is available.

< Socket set>

- 113F1-DA3 socket set

{ LSPACK113A1110NO1
{ CSSOCKET113A1110NO1

1.2 Hardware Configuration

Figures 1-2 and 1-3 show the IE-780354-NS-EM1's position in the basic hardware configuration.

Figure 1-2. Basic Hardware Configuration (1) (When IE-78K0-NS Is Used)

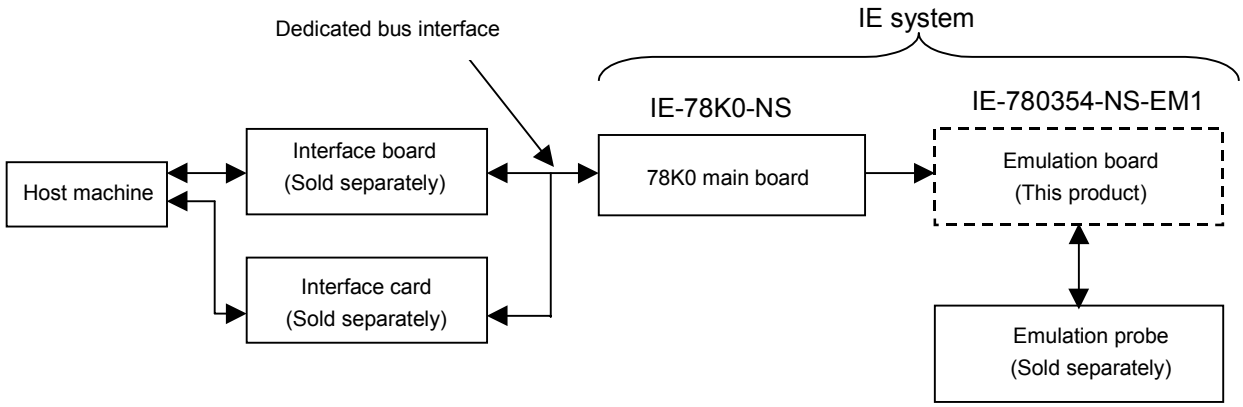
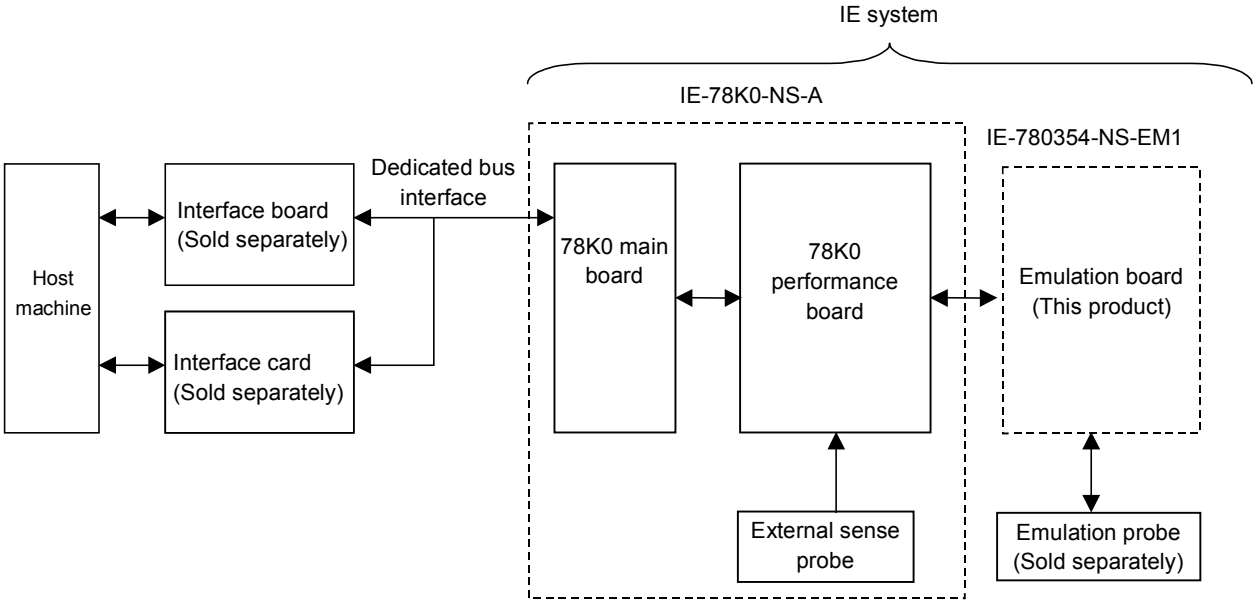


Figure 1-3. Basic Hardware Configuration (2) (When IE-78K0-NS-A Is Used)



1.3 Basic Specifications

< Basic Specifications >

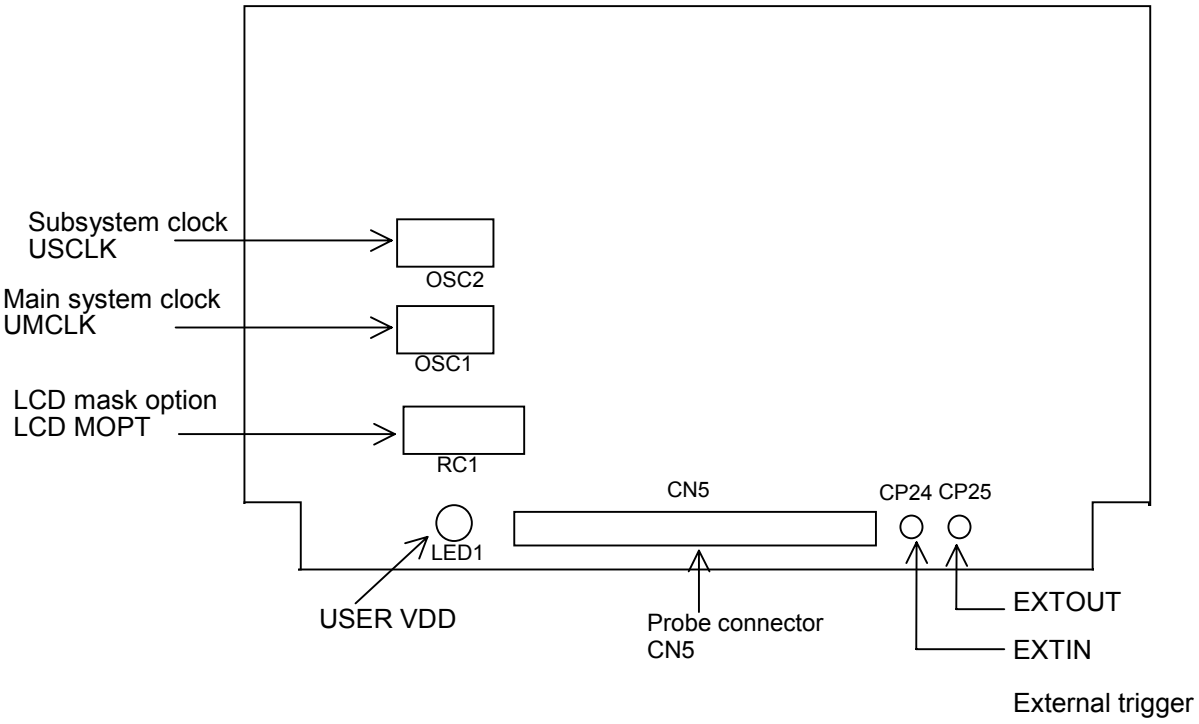
Parameter	Description
Target device	μPD780343, 780343Y, 780344, 780344Y, 780353, 780353Y, 780354, 780354Y μPD78F0354, 78F0354Y
System clock	Main system clock: 10.0 MHz Subsystem clock: 32.768 kHz (131.072 kHz for x4 subsystem clock)
Main system clock supply	Internal: Mounted on the emulation board (10.0 MHz) or mounted by user on the parts board External: Input from the target system via an emulation probe
Subsystem clock supply	Internal: Mounted on the emulation board (1.048576 MHz) or mounted by user on the parts board External: Input from the target system via an emulation probe
Low voltage	V_{DD} = 1.8 to 5.5 V (same as the target device)

CHAPTER 2 PART NAMES

This chapter introduces the part names of the IE-780354-NS-EM1 main unit.
The packing box contains the emulation board (IE-780354-NS-EM1), package details, user's manual, and guarantee card.
If there are any missing or damaged items, please contact an NEC sales representative.
Fill out and return the guarantee card that comes with the main unit.

2.1 Names of Parts on Board

< IE-780354-NS-EM1 Board >



CHAPTER 3 INSTALLATION

This chapter describes methods for connecting the IE-780354-NS-EM1 to the IE-78K0-NS or IE-78K0-NS-A and emulation probe. Mode setting methods are also described.

Caution Connecting or removing parts to or from the target system, or making switch or other setting changes must be carried out after the power supply to both the IE system and the target system has been switched off.

3.1 Connection

(1) Connection with IE-78K0-NS or IE-78K0-NS-A main unit

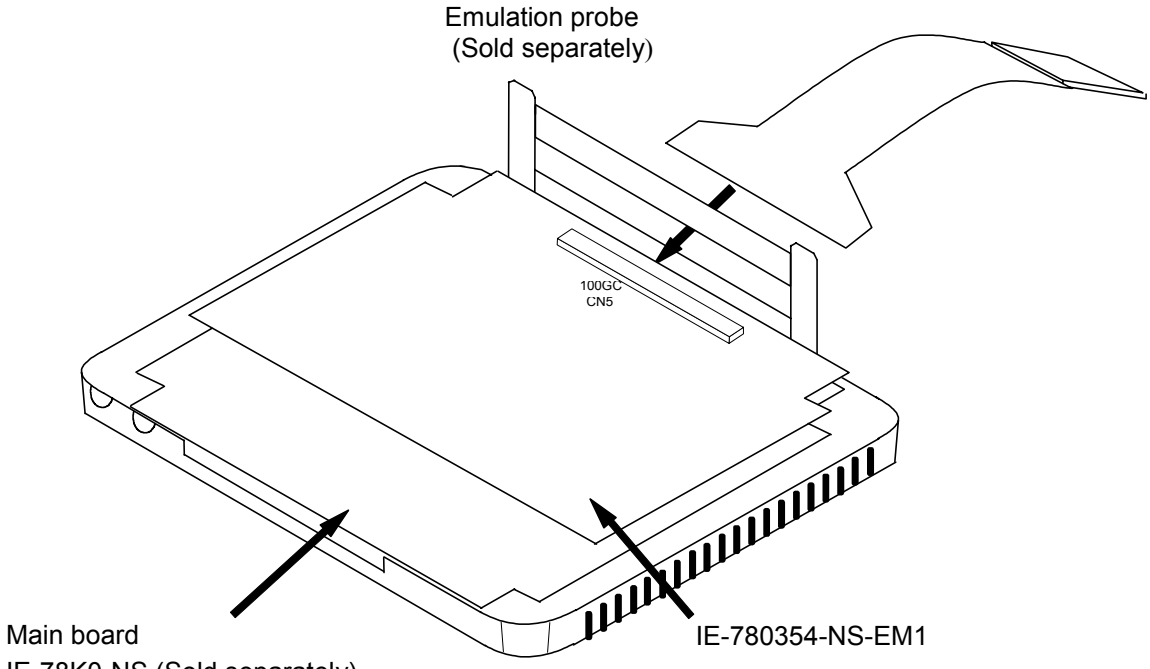
See the IE-78K0-NS User's Manual (U13731E) for a description of how to connect the IE-780354-NS-EM1 to the IE-78K0-NS.

See the IE-78K0-NS-A User's Manual (U14889E) for a description of how to connect the IE-780354-NS-EM1 to the IE-78K0-NS-A.

(2) Connection with emulation probe

See the IE-78K0-NS User's Manual (U13731E) or IE-78K0-NS-A User's Manual (U14889E) for a description of how to connect an emulation probe to the IE-780354-NS-EM1.

Caution Incorrect connection may damage the IE system. For more details on connection, see the user's manual for each emulation probe.



3.2 Clock Settings

3.2.1 When using a user clock

(a) Main system clock

A 10.0 MHz crystal oscillator is mounted on the UMCLK socket (OSC1) of the IE-780354-NS-EM1 at shipment.

The frequency of the main system clock can be changed in the following three ways.

- Replace the crystal oscillator (UMCLK socket)
- Configure an oscillator (UMCLK socket)
- Input a clock from the target system (X1 pin)

Note An abnormal main system clock supply will cause the IE system to hang up.

(b) Subsystem clock

A 1.048576 MHz crystal oscillator is mounted on the USCLK socket (OSC2) of the IE-780354-NS-EM1 EM1 at shipment.

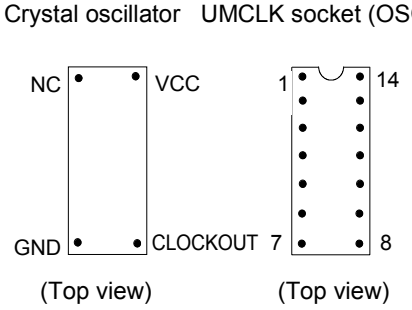
The frequency of the subsystem clock can be changed in the following three ways.

- Mount a crystal oscillator (USCLK socket)
- Configure an oscillator (USCLK socket)
- Input a clock from the target system (XT1 pin)

3.2.2 When using a crystal oscillator

(a) Main system clock

When using a crystal oscillator for the main system clock, install a crystal oscillator with the following pin configuration in the UMCLK socket (OSC1) as shown in the diagram.

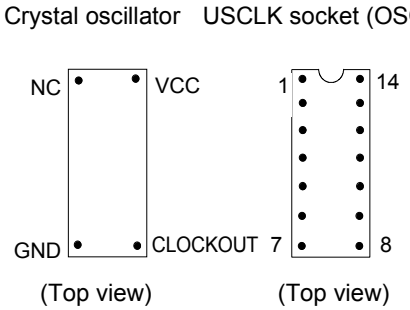


Crystal Oscillator Pin	Socket Pin No.
NC	1
GND	7
CLOCK OUT	8
Vcc	14

(b) Subsystem clock

When using a crystal oscillator for the subsystem clock, install a crystal oscillator with the following pin configuration in the USCLK socket (OSC2) as shown in the diagram.

Set the oscillator frequency to x32 the frequency used in the actual chip.



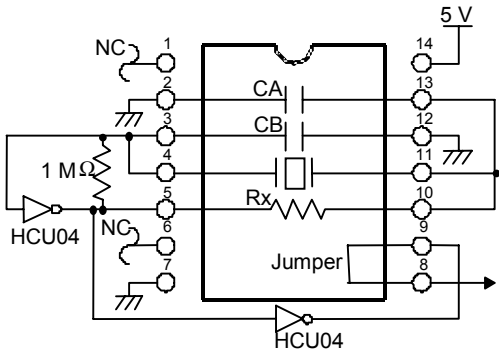
Crystal Oscillator Pin	Socket Pin No.
NC	1
GND	7
CLOCK OUT	8
Vcc	14

3.2.3 When using a ceramic resonator or crystal oscillator

(a) Main system clock

The circuit configuration is as follows when using a ceramic resonator or crystal resonator for the main system clock. Mount a resonator, resistor and capacitors with the required frequency in the UMCLK socket (OSC1).

UMCLK socket (OSC1)



(Top View)

Pin No.	Connection
2-13	Capacitor CA
3-12	Capacitor CB
4-11	Resonator
5-10	Resistor Rx
8-9	Shorted

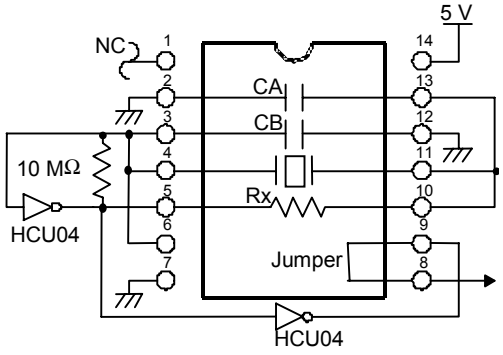
Remark NC = No Connection

(b) Subsystem clock

The circuit configuration is as follows when using a ceramic resonator or crystal resonator for the subsystem clock. Mount a resonator, resistor and capacitors with the required frequency in the USCLK socket (OSC2).

Set the frequency in the USCLK socket (OSC2) to x32 the frequency used in the actual chip.

USCLK socket (OSC2)



(Top View)

Pin No.	Connection
2-13	Capacitor CA
3-12	Capacitor CB
4-11	Resonators
5-10	Resistor Rx
8-9	Shorted

Remark NC = No Connection

3.2.4 When using a clock from the target system

(a) Main system clock

When using a clock supplied from target system for the main system clock, input the necessary clock from the X1 pin.

Switch the clock from the target system and the clock from the UMCLK socket (OSC1) by using the integrated debugger (ID78K0-NS).
Refer to the ID78K0-NS User's Manual (U14379E) for details.

Note Input a rectangular pulse for the clock from the target system.
It is not necessary to supply a clock to the X2 pin.

(b) Subsystem clock

When using a clock supplied from target system for the subsystem clock, input the necessary clock from the XT1 pin.
The frequency of the clock supplied from target system should be x4 the frequency used in the actual chip.

Switch the clock from the target system and the clock from the USCLK socket (OSC2) by using a jumper (JP8) of the IE-78K0-NS or IE-78K0-NS-A. Refer to the IE-78K0-NS User's Manual (U13731E) or IE-78K0-NS-A User's Manual (U14889E) for details of the jumper position.

<JP8 settings>

1-2 shorted: Supplied from the USCLK socket

3-4 shorted: Supplied from the target system

Note Input a rectangular pulse for the clock from the target system.
It is not necessary to supply a clock to the XT2 pin.

3.3 LCD Booster Circuit Settings

At shipment, an LCD driving booster circuit is mounted on the parts board on the LCD MOPT socket (RC1) on the IE-780354-NS-EM1.

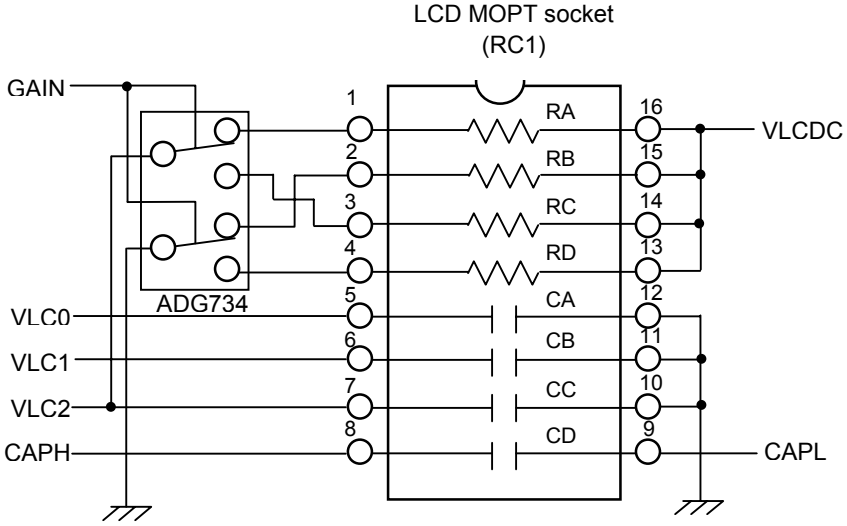
When changing the LCD driving booster circuit, mount the required resistors and capacitors on the parts board included with the IE-780354-NS-EM1, and mount the parts board on the LCD MOPT socket (RC1).

Fix the capacitors CA, CB, CC, and CD to 0.47 μF.

Change RA and RB when gain adjustment is set to x1.0 (GAIN = 0). Change RC and RD when gain adjustment is set to x1.5 (GAIN = 1).

The LCD driving booster circuit has the configuration shown below.

Note The booster circuit on the target system cannot be used.
Change RA/RB or RC/RD so that the gain adjustment is set to x1.0 or x1.5; otherwise the IE system may be damaged.



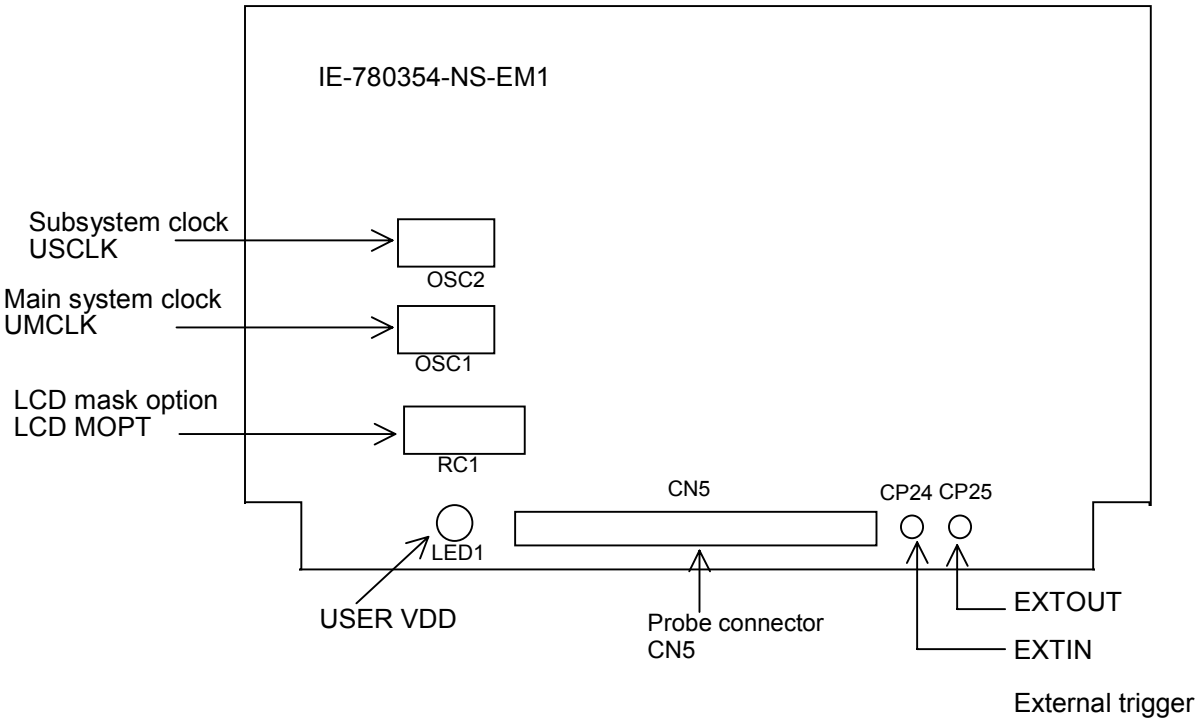
Connected Pins	Parts Used	Parts Board at Shipment	
1-16	Resistor RA	Short	Sets gain adjustment to x1.0
2-15	Resistor RB	3 MΩ	
3-14	Resistor RC	1 MΩ	Sets gain adjustment to x1.5
4-13	Resistor RD	2 MΩ	
5-12	Capacitor CA	0.47 μF (fixed)	
6-11	Capacitor CB	0.47 μF (fixed)	
7-10	Capacitor CC	0.47 μF (fixed)	
8-9	Capacitor CD	0.47 μF (fixed)	

3.4 External Trigger

To set an external trigger, connect it to the IE-780354-NS-EM1's check pin, EXTIN pin, and EXTOUT pin as shown below.

See the ID78K0-NS User's Manual (U14379E) for descriptions of usage.

See the IE-78K0-NS User's Manual (U13731E) or IE-78K0-NS-A User's Manual (U14889E) for descriptions of pin characteristics.



3.5 Jumper Settings of IE-78K0-NS

When using the IE-780354-NS-EM1 in combination with the IE-78K0-NS, set each jumper of the IE-78K0-NS as shown below. For the positions of the jumpers, refer to the IE-78K0-NS User's Manual (U13731E).

Setting of Jumpers on IE-78K0-NS

	JP2	JP3	JP4	JP6	JP7	JP8
Setting	2-3 short	1-2 short	1-2 short	3-4 short	1-2 short	1-2 short

3.6 Jumper Settings of IE-78K0-NS-A

When using the IE-780354-NS-EM1 in combination with the IE-78K0-NS-A, set each jumper of the IE-78K0-NS-A as shown below. For the positions of the jumpers, refer to the IE-78K0-NS-A User's Manual (U14889E).

Setting of Jumpers on IE-78K0-NS-A

	JP2	JP3	JP4	JP6	JP7	JP8
Setting	2-3 short	1-2 short	1-2 short	3-4 short	1-2 short	1-2 short

Setting of Jumpers on G-78K0H Option Board on IE-78K0-NS-A

	J1
Setting	2-3 short

CHAPTER 4 DIFFERENCES BETWEEN TARGET DEVICES AND TARGET INTERFACE CIRCUITS

This chapter describes the differences between the signal lines of the target device (μPD780343/43Y/44/44Y/53/53Y/54/54Y and μPD78F0354/54Y) and these of the IE-780354-NS-EM1's target interface circuit.

The target device consists of CMOS circuits, whereas the IE-780354-NS-EM1's target interface circuit consists of emulation circuits such as the emulation CPU, TTL, and CMOS-IC.

At the time of debugging by connecting the IE system and the target system, the IE system performs the emulation as if the actual target device is operating on the target system, however, in reality, it is the IE system that performs the emulation, thus producing a slight differences.

(1) Signals that are input/output from an emulation CPU μPD7880
(2) Signals that are input/output from an emulation CPU μPD78F0338
(3) Signals that are input/output from emulation CPUs μPD7880 and 78F0338
(4) Other signals

Regarding the signals in (1) to (4) above, the circuits of the IE system are shown below.

(1) Signals that are input/output from emulation CPU μPD7880

Refer to Figure 4-1 Equivalent Circuit of Emulation Circuit (1).

- P02 to P00
- P07 to P04
- P27 to P20
- P35 to P30
- P43 to P40
- P73 to P70
- X1
- XT1
- RESET_

(2) Signals that are input/output from emulation CPU μPD78F0338

Refer to Figure 4-2 Equivalent Circuit of Emulation Circuit (2).

- P17 to P10
- S11 to S0
- COM3 to COM0
- SCOM0
- AVREF
- AVSS

(3) Signals that are input/output from emulation CPUs μPD7880 and 78F0338

Refer to Figure 4-3 Equivalent Circuit of Emulation Circuit (3).

- P87 to P80/S19 toS12
- P97 to P90/S27 to S20
- P107 to P100/S35 to S28
- P113 to P110/S39 to S36
- P03/INTP3/ADTRG

(4) Other signals

Refer to Figure 4-4 Equivalent Circuit of Emulation Circuit (4).

- VLC2 to VLC0
- CAPH, CAPL, X2, XT2, VDD0, VDD1, VSS0, VSS1, VPP

Note The processing of the pins in (1) and (2) and their the alternate function pins is the same.

There is no circuit in the IE system.

Figure 4-1. Equivalent Circuit of Emulation Circuit (1)

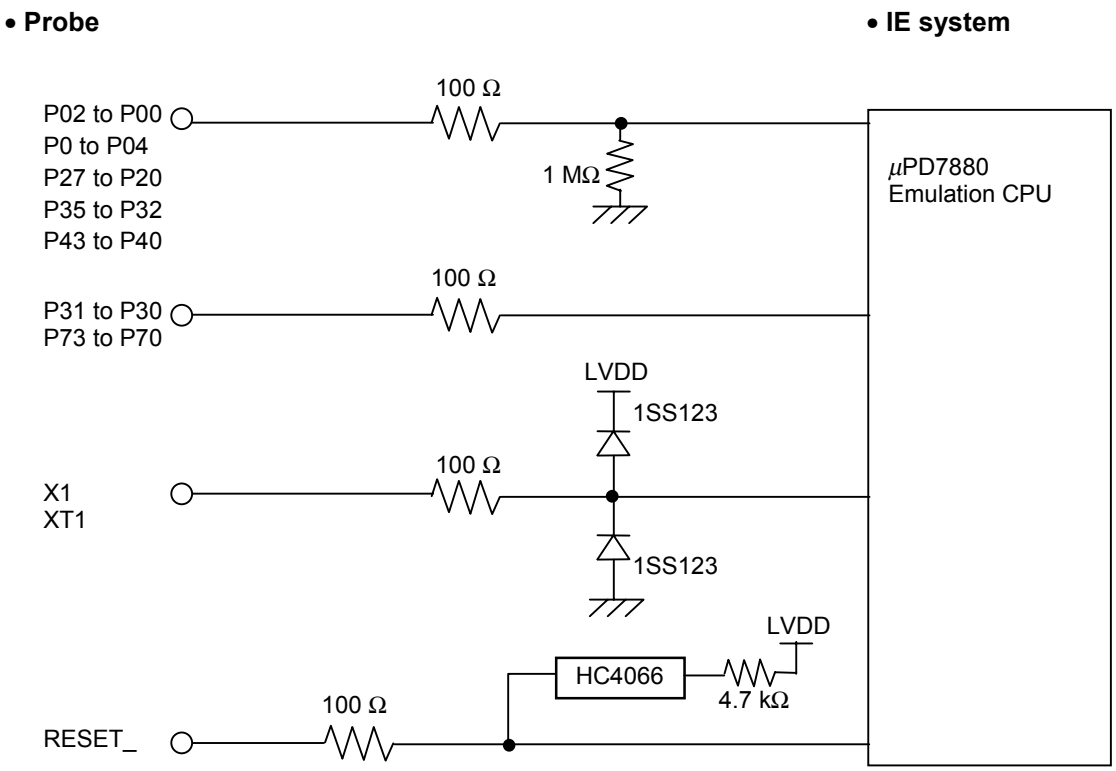


Figure 4-2. Equivalent Circuit of Emulation Circuit (2)

Figure 4-3. Equivalent Circuit of Emulation Circuit (3)

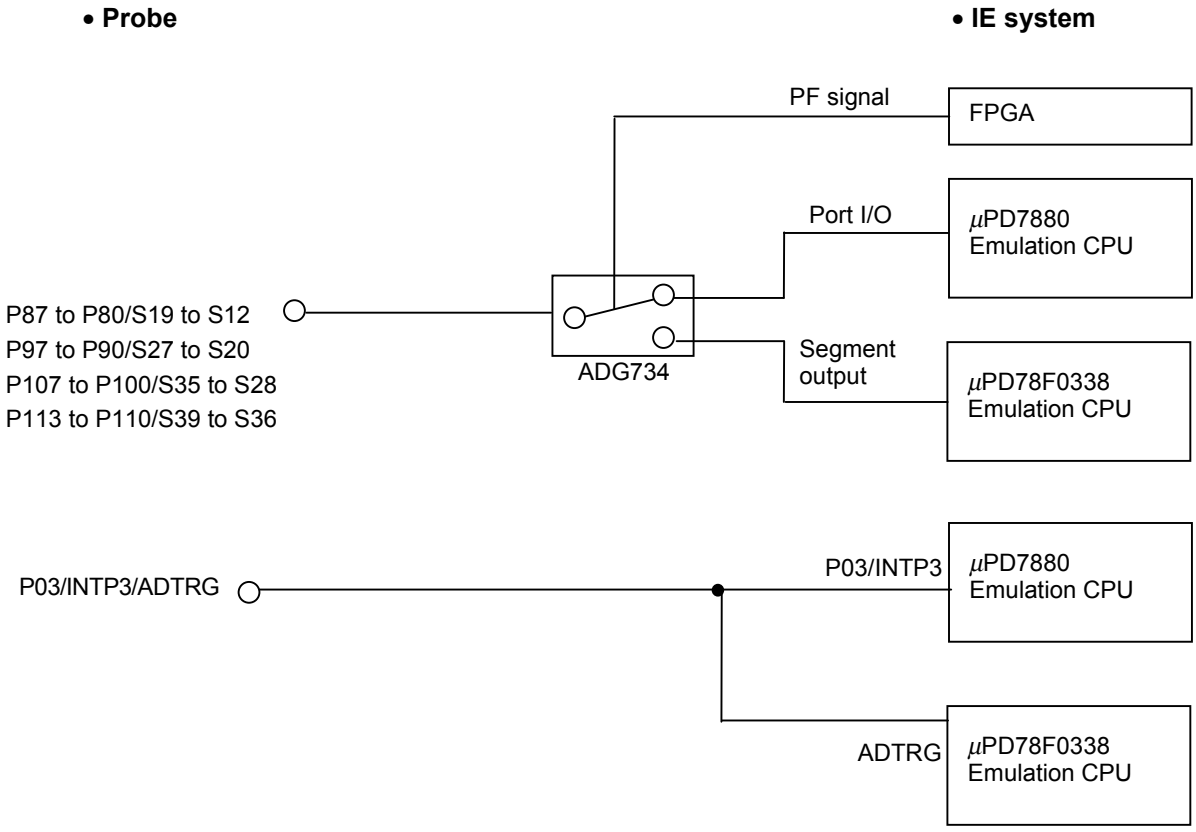
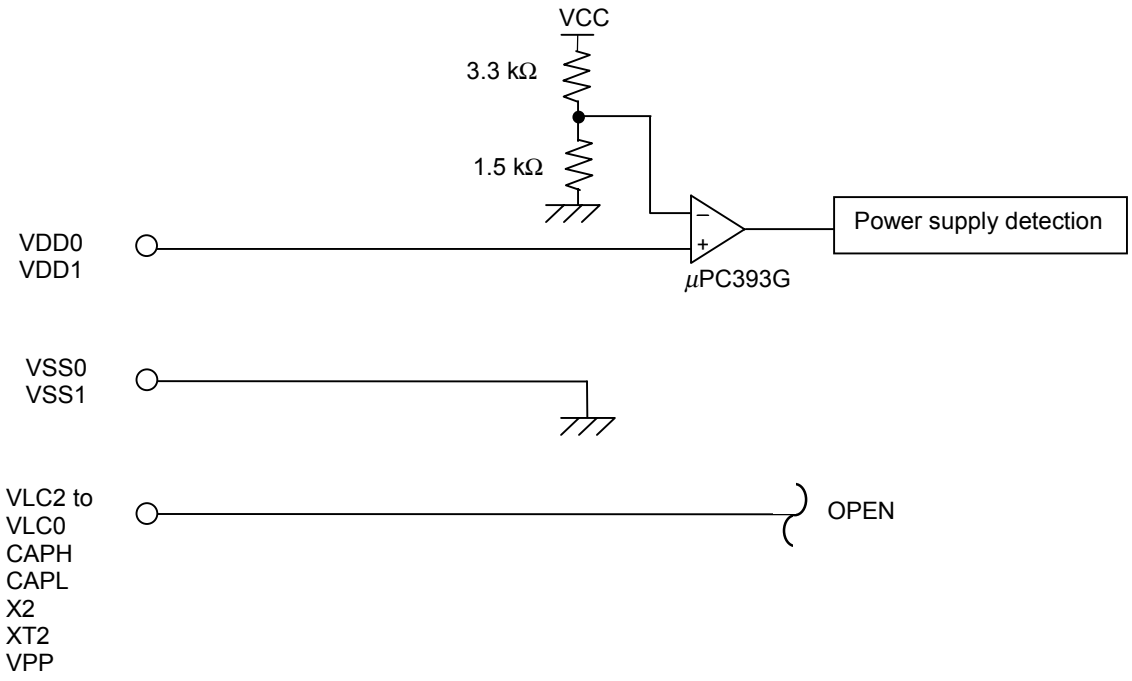


Figure 4-4. Equivalent Circuit of Emulation Circuit (4)



CHAPTER 5 RESTRICTIONS

This chapter explains the usage restrictions of the IE-780354-NS-EM1.
The emulation function of the target device and the IE-780354-NS-EM1 differs in terms of the following points.

1. Set data to the SCT flag (bit 0 of the SSCK register) after reset release and before setting the CSS flag (bit 4 of the PCC register) to 1. The SCT flag can only be cleared by a reset.

2. When the CPU is operating at x4 subsystem clock, a wait equivalent to 1 subsystem clock cycle is not inserted in the emulator after HALT instruction release. (A wait equivalent to 1 subsystem clock cycle is inserted in the target device.)

3. When a target device is not connected, the initial value of P17 to P10, P30, P31, and P73 to P70 is undefined.

4. The port output (write timing) is one clock earlier than that in the target device.

5. When the 8-bit timer (TM51) and watch timer (WTN0) are operated with the subsystem clock, an interrupt may occur one clock earlier than the timing in the target device specification.
   Correction is planned in device file version E1.00h or later.

CHAPTER 6 CAUTIONS

This chapter explains the cautions on using the IE-780354-NS-EM1.

1. Connection with the IE-78001-R-A is not supported.
   (If connected, the port trace result will not be displayed correctly.)

2. Use device file E1.00h or later.
   (In E1.00g or earlier, the mask option function for P30, P31, P70 to P73 cannot be used.)

APPENDIX A EMULATION PROBE PIN CORRESPONDENCE TABLE

Table A-1. Pin Correspondence of NP-100GC and NP-H100GC-TQ (1/2)

Emulation Device Pin	CN5 Pin No.	Emulation Device Pin	CN5 Pin No.
1	118	26	34
2	117	27	37
3	114	28	38
4	113	29	43
5	108	30	44
6	107	31	47
7	104	32	48
8	103	33	51
9	100	34	52
10	99	35	57
11	94	36	58
12	93	37	59
13	30	38	60
14	29	39	55
15	24	40	56
16	23	41	49
17	20	42	50
18	19	43	45
19	16	44	46
20	15	45	41
21	10	46	42
22	9	47	35
23	6	48	36
24	5	49	31
25	33	50	32

Remarks 1. The 100GC and NP-H100GC-TQ are products of Naito Densei Machida Mfg. Co., Ltd.

2. The numbers in the Emulation Device Pin column refer to the pin number of the emulation probe.

3. The numbers in the CN5 Pin No. column refer to the pin number of the emulation probe on the IE system side.

Table A-1. Pin Correspondence of NP-100GC and NP-H100GC-TQ (2/2)

Emulation Device Pin	CN5 Pin No.	Emulation Device Pin	CN5 Pin No.
51	4	76	88
52	3	77	83
53	8	78	84
54	7	79	77
55	14	80	78
56	13	81	73
57	18	82	74
58	17	83	69
59	22	84	70
60	21	85	63
61	28	86	64
62	27	87	61
63	92	88	62
64	91	89	65
65	98	90	66
66	97	91	71
67	102	92	72
68	101	93	75
69	106	94	76
70	105	95	79
71	112	96	80
72	111	97	85
73	116	98	86
74	115	99	89
75	87	100	90

Remarks 1. The 100GC and NP-H100GC-TQ are products of Naito Densei Machida Mfg. Co., Ltd.

2. The numbers in the Emulation Device Pin column refer to the pin number of the emulation probe.

3. The numbers in the CN5 Pin No. column refer to the pin number of the emulation probe on the IE system side.

Table A-2. Pin Correspondence of NP-113F1-DA3 (1/2)

Emulation Device Pin	CN5 Pin No.	Emulation Device Pin	CN5 Pin No.
A1	–	J3	6
B1	117	K3	38
C1	–	L3	–
D1	107	A4	76
E1	103	B4	79
F1	93	C4	85
G1	24	D4	108
H1	16	E4	30
J1	–	F4	29
K1	33	G4	19
L1	–	H4	44
A2	90	J4	52
B2	118	K4	43
C2	114	L4	47
D2	113	A5	66
E2	104	B5	71
F2	94	C5	80
G2	23	D5	75
H2	15	E5	–
J2	5	H5	60
K2	34	J5	57
L2	37	K5	48
A3	–	L5	51
B3	89	A6	61
C3	86	B6	64
D3	100	C6	72
E3	99	D6	65
F3	20	H6	55
G3	10	J6	50
H3	9	K6	58

Remarks 1. The NP-113F1-DA3 is a product of Naito Densei Machida Mfg. Co., Ltd.

2. The numbers in the Emulation Device Pin column refer to the pin number of the emulation probe.

3. The numbers in the CN5 Pin No. column refer to the pin number of the emulation probe on the IE system side.

Table A-2. Pin Correspondence of NP-113F1-DA3 (2/2)

Emulation Device Pin	CN5 Pin No.	Emulation Device Pin	CN5 Pin No.
L6	59	H9	22
A7	69	J9	36
B7	74	K9	31
C7	63	L9	–
D7	62	A10	83
H7	45	B10	88
J7	42	C10	115
K7	49	D10	105
L7	56	E10	97
A8	73	F10	28
B8	77	G10	18
C8	70	H10	7
D8	78	J10	8
E8	101	K10	4
F8	91	L10	32
G8	92	A11	–
H8	14	B11	87
J8	35	C11	–
K8	41	D11	106
L8	46	E11	98
A9	–	F11	27
B9	84	G11	17
C9	116	H11	13
D9	111	J11	–
E9	112	K11	3
F9	102	L11	–
G9	21		

Remarks 1. The NP-113F1-DA3 is a product of Naito Densei Machida Mfg. Co., Ltd.

2. The numbers in the Emulation Device Pin column refer to the pin number of the emulation probe.

3. The numbers in the CN5 Pin No. column refer to the pin number of the emulation probe on the IE system side.