Microcontroller Technical Information

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IE-703288-G1-EM1 In-Circuit Emulator Emulation Board for V850ES/SG1, V850ES/SG2, V850ES/SJ2, V850ES/SG3, and V850ES/SJ3 Usage Restrictions		Document No.	ZBG-CD-07-0019	1/2
		Date issued	March 30, 2007	
		Issued by	Development Tool Group Multipurpose Microcomputer Systems Division 4th Systems Operations Unit NEC Electronics Corporation	
Related documents	IE-703288-G1-EM1 User's Manual: U16697EJ1V0UM	Notification classification	√	Usage restriction
				Upgrade
				Document modification
				Other notification

1. Affected product

Product	Outline	Control Code[Note]
IE-703288-G1-EM1	In-circuit emulator emulation board for V850ES/SG1, V850ES/SG2, V850ES/SJ2, V850ES/SG3, and V850ES/SJ3	A, B, C, D, E, F, G

2. Restriction details

Restriction No. 21 has been added. See the attachment for details.

3. Workarounds

See the attachment for details.

4. Modification schedule

Please regard restriction No. 21 as a permanent restriction.

5. List of usage restrictions

See the attachment for details.

Note The "control code" is the second digit from the left in the 10-digit serial number. If the product has been upgraded, the version can be checked by the board version.
See the attachment for the identification method for the control code

6. Document revision history

Document Number	Date Issued	Description
SBG-DT-03-0099-E	January 14, 2003	Newly created.
SBG-DT-03-0315	December 11, 2003	Addition of erroneous description corrections (No. 7 to No. 11)
ZBG-CD-04-0060	September 10, 2004	Addition of bug (No. 18) Addition of expanded specification (No. 19)
ZBG-CD-06-0022	March 24, 2006	Addition of bug (No. 20) Addition of **4. Supported Devices** Addition of **5. Special Notes on Emulating V850ES/SG3 and V850ES/SJ3**
ZBG-CD-07-0019	March 30, 2007	Addition of restriction (No. 21) Addition of (3) for **5. Special Notes on Emulating V850ES/SG3 and V850ES/SJ3**

Notes on Using IE-703288-G1-EM1

This document describes restrictions applicable only to the emulator and restrictions that are planned for correction in the emulator.

Refer to the following documents for the restrictions in the target device.

- User's manual of target device
- Restrictions notification document for target device

Also refer to the user's manual of the emulator for cautions on using the emulator.

1. Product Version

Control Code[Note]	Board Version	Peripheral EVA Chip
A	V1.00	μPD70F3289Y DS 1.0
B	V1.01	μPD70F3289Y DS 1.0
C	V1.02	μPD70F3289Y V1.1
D	V1.03	μPD70F3269Y DS 1.0
E	V1.04	μPD70F3289Y V2.1
F	V1.15	μPD70F3289Y V2.1
	V1.16	μPD70F3289Y DS 2.2, rank E
G	V1.26	μPD70F3289Y DS 2.2, rank E

Employ an IE-V850ES-G1 with a control code of F or later when using this emulation board.

2. Product History

No.	Bugs and Changes/Additions to Specifications	Control Code[Note]						
		A	B	C	D	E	F	G
1	ROM correction function cannot be emulated	Permanent restriction						
2	Restriction on use-prohibited area	Permanent restriction						
3	Bug in port mode control registers	×	○	○	○	○	○	○
4	Emulation CPU in which bugs have been corrected temporarily	○	×	○	○	○	○	○
5	Bug in port 9 N-ch open-drain output	×	×	○	○	○	○	○
6	Improvement of conversion accuracy of A/D converter and D/A converter	×	×	×	○	○	○	○
7	Bug in CAN transmission/reception	×	×	×	×	○	○	○
8	Restriction when reset by watchdog timer or external reset occurs	×	×	×	×	○	○	○
9	Bug in watchdog timer during break	Permanent restriction						
10	Bug in 16-bit timer M during break	Permanent restriction						
11	Bug in 16-bit timer M compare register	Permanent restriction						
12	Bug in accessing UAnRX register during break	Permanent restriction						
13	Bug in accessing DR register during break	Permanent restriction						
14	Bug in accessing CBnRX register during	Permanent restriction						
15	Bug in accessing C0RGPT register during break	Permanent restriction						
16	Bug in accessing C0TGPT register during break	Permanent restriction						
17	Bug in accessing C0GNCTRL register during break	Permanent restriction						
18	Restriction on RESF register	×	×	×	×	×	○	○
19	Expansion of operating frequency specification	×	×	×	×	×	○	○
20	Bug occurs if emulator continuously accesses a peripheral I/O register for which a CPU wait may occurs	×	×	×	×	×	×	○
21	Restriction on CLKOUT output in standby mode	Permanent restriction						

×: Applicable, ○: Not applicable or already corrected

Note The “control code” is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If the product has been upgraded, the version can be checked by the board version.

3. Details of Bugs and Added Specifications

No. 1 ROM correction function cannot be emulated

[Description]

The ROM correction function cannot be emulated.

[Workaround]

There is no workaround. Please regard this issue as a permanent restriction.

No. 2 Restriction on use-prohibited area

[Description]

A fail-safe break does not occur even if the program is executed or an access occurs in the use-prohibited area of the target device.

[Workaround]

A break can be generated when the program is executed or an access occurs by setting a break on the debugger under the following conditions.

Please regard this issue as a permanent restriction.

* This restriction and workaround are described in detail on the next page.

No. 2 Restriction on use-prohibited area (in detail)

Target Device	D703260(Y) D703270(Y) D703280(Y)	D703261(Y), D70F3261(Y) D703271(Y), D70F3271(Y) D703281(Y), D70F3281(Y) D703264(Y), D70F3264(Y) D703274(Y), D70F3274(Y) D703284(Y), D70F3284(Y)	D703262(Y) D703272(Y) D703282(Y) D703265(Y) D703275(Y) D703285(Y) D703287(Y)	D703263(Y), D70F3263(Y) D703273(Y), D70F3273(Y) D703283(Y), D70F3283(Y) D703266(Y), D70F3266(Y) D703276(Y), D70F3276(Y) D703286(Y), D70F3286(Y) D703288(Y), D70F3288(Y)
Restriction A fail-safe break does not occur even if the program is executed or an access occurs in the use-prohibited area of the target device described on the right.	(1) 0x3FF8000 to 0x3FF8FFF	(2) 0x60000 to 0x7FFFF (3) 0x3FF0000 to 0x3FF6FFF	(4) 0x3FF0000 to 0x3FF4FFF	(5) 0xA0000 to 0xFFFFF (6) 0x3FF0000 to 0x3FF2FFF
Workaround A break can be generated when the program is executed occurs by setting a break on the debugger under the conditions described on the right.	Area (1) • Event status: Execution • Address: 0x3ff8000 to 0x3ff8fff (Two execution events are used by setting the above conditions.)	Area (2) • Event status: Execution • Address: 0x60000 to 0x7ffff Area (3) • Event status: Execution • Address: 0x3ff0000 to 0x3ff6fff (Four execution events are used by setting the above conditions.)	Area (4) • Event status: Execution • Address: 0x3ff0000 to 0x3ff4fff (Two execution events are used by setting the above conditions.)	Area (5) • Event status: Execution • Address: 0xa0000 to 0xfffff Area (6) • Event status: Execution • Address: 0x3ff0000 to 0x3ff2fff (Four execution events are used by setting the above conditions.)
A break can be generated when an access occurs by setting a break on the debugger under the conditions described on the right.	Area (1) • Event status: R/W • Access size: No Condition • Address: 0x3ff8000 to 0x3ff8fff (Two access events are used by setting the above conditions.)	Area (3) • Event status: R/W • Access size: No Condition • Address: 0x3ff0000 to 0x3ff6fff (Two access events are used by setting the above conditions.)	Area (4) • Event status: R/W • Access size: No Condition • Address: 0x3ff0000 to 0x3ff4fff (Two access events are used by setting the above conditions.)	Area (6) • Event status: R/W • Access size: No Condition • Address: 0x3ff0000 to 0x3ff2fff (Two access events are used by setting the above conditions.)

No. 3 Bug in port mode control registers

[Description]

All the peripheral I/O register values become undefined if any of the following bits of the port mode control registers is set to 1.

Bits 2 and 3 of the PCM0 register

Bits 0 to 5 of the PCM3 register

[Workaround]

Do not set the above bits of the port mode control registers to 1.

This issue has been corrected in control code B and later.

No. 4 Emulation CPU in which bugs have been corrected temporarily

[Description]

Bugs have been corrected temporarily in the emulation CPU.

Compared to the ordinary CPU, however, this emulation CPU is degraded in terms of reliability and durability.

[Workaround]

There is no workaround. This issue has been corrected in control code C and later.

No. 5 Bug in port 9 N-ch open-drain output

[Description]

When each bit of ports 90 to 915 is set to N-ch open-drain output and each output of ports 90 to 915 is set to “1 output”, the pin voltage becomes an intermediate potential between the voltage pulled up by the target side and EV_{DD}.

[Workaround]

There is no workaround. This issue has been corrected in control code C and later.

No. 6 Improvement of conversion accuracy of A/D converter and D/A converter

[Description]

The conversion accuracy of the A/D converter and D/A converter has been improved (conventional error: approx. 8%).

This improvement has been implemented in control code D and later.

No. 7 Bug in CAN transmission/reception

[Description]

(a) Illegal message reception

The receive message may not be stored normally when a transmit request is set (by setting the TRQx flag) by setting an extension ID during reception (data field or later).

As a result, extension IDs (ID15 to ID0) of the receive message buffer are erroneously recognized upon comparison between the receive message buffer ID setting and the receive message ID. If they match, the receive data is illegally written to the next buffer to the matched receive message

buffer (MSG#n) (MSG#(n+1)). However, MSG#0 will never be written illegally.

(b) Illegal message transmission

The operations shown below may occur when a conflict between an internal operation during transmission/reception or upon completion of transmission/reception and a write to the transmit request flag (TRQx) occurs.

- If the transmit request flag for message buffer 0 (MSG#0) is written, transmission is not performed or data in MSG#1 is transmitted illegally.
- If multiple transmit requests have been set by an extension ID, the priority judgment of the subsequent messages becomes illegal.

[Workaround]

Implement the following software settings.

(a) Use the standard ID setting (not the extension ID).

(b) Set message buffer 0 (MSG#0) as the receive buffer.

* In automatic block transmission mode, however, MSG#0 can be used as the transmit buffer. This issue has been corrected in control code E and later.

No. 8 Restriction when reset by watchdog timer or external reset occurs

[Description]

Access to the I/O register becomes illegal when a reset by the watchdog timer or an external reset occurs.

A correct value cannot be read during read, and cannot be written during write.

[Workaround]

The normal status is restored by pressing the CPU reset button on the debugger.

This issue has been corrected in control code E and later.

No. 9 Bug in watchdog timer during break

[Description]

When both the following conditions (a) and (b) are satisfied and a break occurs, the watchdog timer does not stop and a reset or a non-maskable interrupt occurs. If a reset occurs, the debugger hangs up.

(a) The main clock or subclock is selected as the source clock for the watchdog timer

(b) The internal oscillator is stopped (RSTOP flag =1)

[Workaround]

Implement (a) or (b) below.

(a) Use the Internal oscillation clock as the source clock.

(b) Do not stop the internal oscillator.

Please regard this issue as a permanent restriction.

No. 10 Bug in 16-bit timer M during break

[Description]

When a break occurs while the following both (a) and (b) are satisfied, timer M does not stop even if the Peripheral Break function has been set to “Break”.

(a) INTWT, internal oscillation clock (f_R/8), or subclock is selected as the source clock of timer M.

(b) The main clock is stopped by setting the MCK flag.

* The Peripheral Break function is not supported by the debugger ID850 V2.51.

[Workaround]

Implement (a) or (b) below to stop timer M during a break using the Peripheral Break function.

(a) Use the main clock (fxx, fxx/2, fxx/4, fxx/64, or fxx/512) as the source clock.

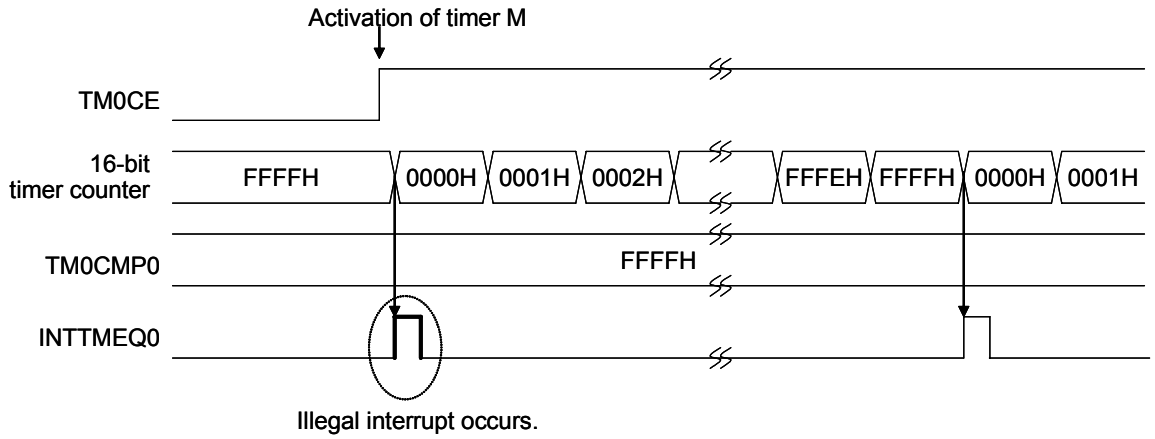
(b) Do not stop main clock oscillation.

Please regard this issue as a permanent restriction.

No. 11 Bug in 16-bit timer M compare register

[Description]

An illegal interrupt occurs after timer M activation when TMM0 compare register 0 (TM0CMP0) is set to FFFFH. See the figure below for details.



[Workaround]

Do not set the TM0CMP0 register to FFFFH.

Please regard this issue as a permanent restriction.

No. 12 Bug in accessing UAnRX register during break

[Description]

An overrun error occurs under the following conditions (a) to (c).

(a) If a break occurs after reading the UART receive buffer register (UAnRX) and the UAnRX register is displayed in the I/O register window of the debugger, an overrun error occurs when UART reception is performed next time.

(b) If a software break occurs immediately after reading the UART receive buffer register (UAnRX), an overrun error occurs when UART reception is performed next time regardless of whether or

not the UAnRX register is displayed in the I/O register window.

(c) If DMA transfer from the UART receive buffer register (UAnRX) is performed during a break[Note], an overrun error occurs when UART reception is performed next time.

Note Including breaks by the RAM monitor function or DMM function. However, the real-time RAM monitor function does not cause this issue because it does not set breaks.

Remark An overrun error also occurs when UART receives data multiple times during a break. This is an emulator specification.

[Workaround]

(a) Do not display the UAnRX register in the I/O register window.

(b) Set a hardware break when setting a break immediately after reading the UAnRX register.

(c) There is no workaround.

Please regard issues (a), (b), and (c) as permanent restrictions.

No. 13 Bug in accessing DR register during break

[Description]

An overrun error occurs under the following conditions (a) and (b).

(a) If a software break occurs immediately after reading the IEBus data register (DR), an overrun error occurs when IEBus reception is performed next time regardless of whether or not the UAnRX register is displayed in the I/O register window.

(b) If DMA transfer from the IEBus data register (DR) is performed during a break[Note], an overrun error occurs when IEBus reception is performed next time.

Note Including breaks by the RAM monitor function or DMM function. However, the real-time RAM monitor function does not cause this issue because it does not set breaks.

Remark An overrun error also occurs when UART receives data multiple times during a break. This is an emulator specification.

[Workaround]

(a) Set a hardware break when setting a break immediately after reading the DR register.

(b) There is no workaround.

Please regard issues (a) and (b) as permanent restrictions.

No. 14 Bug in accessing CBnRX register during break

[Description]

When the CSIBn receive data register (CBnRX) is read, it usually starts the next reception operation. Under the following conditions (a) and (b), however, the next reception operation is not started even if CBnRX is read.

(a) If a software break occurs immediately after reading the CSIBn receive data register (CBnRX).

(b) If DMA transfer from the CSIBn receive data register (CBnRX) is performed during a break[Note].

As a result, communication stops or the DMA controller stops.

Note Including breaks by the RAM monitor function or DMM function. However, the real-time RAM monitor function does not cause this issue because it does not set breaks.

[Workaround]

(a) Set a hardware break when setting a break immediately after reading the CBnRX register.

(b) There is no workaround.

Please regard issues (a) and (b) as permanent restrictions.

No. 15 Bug in accessing C0RGPT register during break

[Description]

Under the following conditions (a) and (b), the read pointer (RGPT) that should be incremented is not incremented, and the same data as previously read is read.

(a) If a software break occurs immediately after reading the CAN0 module receive history list register (C0RGPT).

(b) If DMA transfer from the CAN0 module receive history list register (C0RGPT) is performed during a break[Note].

Note Including breaks by the RAM monitor function or DMM function. However, the real-time RAM monitor function does not cause this issue because it does not set breaks.

[Workaround]

(a) Set a hardware break when setting a break immediately after reading the C0RGPT register.

(b) There is no workaround.

Please regard issues (a) and (b) as permanent restrictions.

No. 16 Bug in accessing C0TGPT register during break

[Description]

Under the following conditions (a) and (b), the read pointer (TGPT) that should be incremented is not incremented, and the same data as previously transmitted is transmitted.

(a) If a software break occurs immediately after reading the CAN0 module transmit history list register (C0TGPT).

(b) If DMA transfer from the CAN0 module transmit history list register (C0TGPT) is performed during a break[Note].

Note Including breaks by the RAM monitor function or DMM function. However, the real-time RAM monitor function does not cause this issue because it does not set breaks.

[Workaround]

(a) Set a hardware break when setting a break immediately after reading the C0TGPT register.

(b) There is no workaround.

Please regard issues (a) and (b) as permanent restrictions.

No. 17 Bug in accessing C0GNCTRL register during break

[Description]

When a register access is performed in the following sequence, a forcible shutdown that should not take place normally may occur after the sequence is complete.

[Sequence for bug occurrence]

(1) The EFSD bit of the CAN0 module control register (C0GMCTRL) is set.

(2) An I/O register[Note] is accessed.

(3) The GOM bit of the CAN0 module control register (C0GMCTRL) is cleared.

Note I/O register access except for clearing the GOM bit of the C0GMCTRL register

Conditions under which a forcible shutdown takes place are shown below.

(a) If a break occurs immediately after the I/O register access in (2) occurs

(b) If a break by the RAM monitor function or DMM function occurs immediately after the I/O register access in (2) occurs

(c) Stepwise execution is performed for the I/O register access in (2)

[Workaround]

Be sure to set the EFSD bit and clear the GOM bit successively when executing a forcible shutdown.

Do not perform register access in the above sequence when not performing a forcible shutdown.

Please regard this issue as a permanent restriction.

No. 18 Restriction on RESF register

[Description]

The WDT2RF bit of the RESF register is not set to 1 when a reset by the watchdog timer occurs.

[Workaround]

There is no workaround.

This issue has been corrected in control code F and later.

No. 19 Expansion of operating frequency specification

[Description]

The maximum operating frequency has been expanded to 32 MHz (before expansion: 20 MHz).

This specification expansion is implemented only in the following product combination.

IE-703288-G1-EM1: Control code F and later

IE-V850ES-G1: Control code F and later

No. 20 Bug occurs if the emulator continuously accesses a peripheral I/O register for which a CPU wait may occur

[Description]

The IE-703288-G1-EM1 may deadlock if it continuously accesses a peripheral I/O register for which a CPU wait may occur.

[Workaround]

There is no workaround.

This issue has been corrected in control code G and later.

No. 21 Restriction on CLKOUT output in standby mode

[Description]

If standby mode (IDLE1, IDLE2, STOP, or Sub-IDLE mode) is entered during CLKOUT output, the operation of the real device and the emulator varies as shown below. It does not vary in HALT mode.

- Real device: The CLKOUT pin outputs low level.
- Emulator: The CLKOUT pin outputs clock.

[Workaround]

If outputting CLKOUT in standby mode (IDLE1, IDLE2, STOP, or Sub-IDLE mode) may cause problems, be sure to set the CLKOUT pin so that it outputs a low level before the mode is shifted from CLKOUT output mode to standby mode using the following procedure.

(1) Clear bit 1 of the port CM mode control register (PMCCM) to 0 (switches to I/O port)

(2) Clear bit 1 of the port CM mode register (PMCM) to 0 (sets output port)

(3) Clear bit 1 of the port CM register (PCM) to 0 (low-level output)

When this procedure is implemented, set bit 1 of the port CM mode control register (PMCCM) to 1 immediately after standby release (switching to CLKOUT output mode) to output CLKOUT.

Please regard this issue as a permanent restriction.

4. Supported Devices

The IE-703288-G1-EM1 can be used for emulation of the following devices.

- V850ES/SG1
- V850ES/SG2
- V850ES/SJ2
- V850ES/SG3
- V850ES/SJ3

5. Special Notes on Emulating V850ES/SG3 and V850ES/SJ3

The IE-703288-G1-EM1 uses the V850ES/SJ2 as the emulation chip.
When performing emulation with the V850ES/SG3 or V850ES/SJ3, therefore, note the following differences in specifications.

(1) Rate of sampling time during conversion by A/D converter is in progress
(2) Generation factor of low-voltage detection interrupt (INTLVI)
(3) LVI circuit characteristics (detection voltage)
(4) Output frequency of internal oscillator
(5) Output resistance of D/A converter

No.	Differences	Emulator	V850ES/SG3, V850ES/SJ3
1	Rate of sampling time during conversion by A/D converter is in progress	4/26 clocks	8/26 clocks
2	Generation factor of low-voltage detection interrupt (INTLVI)	When the power supply voltage drops to lower than the detection voltage	When the power supply voltage drops/rises to lower/higher than the detection voltage
3	LVI circuit characteristics (detection voltage)	2.85 to 3.15 V (3.0 V (TYP.))	2.85 to 3.05 V (2.95 V (TYP.))
4	Output frequency of internal oscillator	200 kHz (TYP.)	220 kHz (TYP.)
5	Output resistance of D/A converter	3.5 kΩ	6.42 kΩ

6. Cautions

6.1 Caution on ID703000 (ID850)

Use V2.51 or later when using the IE-703288-G1-EM1 with the NEC Electronics debugger ID850.

6.2 General cautions on handling this product

Circumstances not covered by product guarantee

- If the product was disassembled, altered, or repaired by the customer
- If it was dropped, broken, or given another strong shock
- Use at overvoltage, use outside guaranteed temperature range, storing outside guaranteed temperature range
- If power was turned on while the power supply unit, PC interface cable, or target system connection was in an unsatisfactory state
- If the power supply cable, PC interface cable, emulation probe, or the like was bent or pulled excessively
- If a power supply cable other than the one supplied with the product is used
- If the product got wet
- If the product and target system were connected while a potential difference existed between the GND of the product and the GND of the target system
- If a connector or cable was removed while the power was being supplied to the product
- If an excessive load was placed on a connector or socket

Safety precautions

- The power supply cable supplied with the IE-V850ES-G1 is for exclusive use with the IE-V850ES-G1. Do not use it with other products.
- If used for a long time, the product may become hot (50°C to 60°C). Be careful of low temperature burns and other dangers due to the product becoming hot.
- Be careful of electrical shock. There is a danger of electrical shock if the product is used as described above in **Circumstances not covered by product guarantee**.