CUSTOMER NOTIFICATION

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IE-703220-G1-EM1

Preliminary User's Manual

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INTRODUCTION

Target Readers This manual is intended for users who design and develop application systems using the V850ES/ST2.

Purpose The purpose of this manual is to describe the proper operation of the IE-703220-G1-EM1 and its basic specifications.

Organization This manual is broadly divided into the following parts.

- Overview
- Names and functions of parts
- Cautions

How to Read This Manual

It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers. The IE-703220-G1-EM1 is used connected to the IE-V850ES-G1 in-circuit emulator. This manual explains the basic setup procedure and switch settings of the IE-V850ES-G1 when it is connected to the IE-703220-G1-EM1. For the names and functions of parts, and the connection of elements, refer to the IE-V850ES-G1 User's Manual.

To learn about the basic specifications and operation methods.

→ Read this manual in the order of the CONTENTS.

To learn the operation methods and command functions, etc., of the IE-V850ES-G1 and IE-703220-G1-EM1.

→ Read the user's manual of the debugger (sold separately) that is used.

Conventions

Note:	Footnote for item marked with **Note** in the text.	
Caution:	Information requiring particular attention.	
Remark:	Supplementary information.	
Numeral representation:	Binary	… xxxx or xxxxB
	Decimal	… xxxx
	Hexadecimal	… xxxxH

Units for representing powers of 2 (address space or memory space):

K (kilo): $2^{10} = 1,024$

M (mega): $2^{20} = 1,024^2$

Terminology The meanings of terms used in this manual are listed below.

Term	Meaning
Target device	Refers to the device targeted for emulation.
Target system	Refers to the system targeted for debugging. This includes the target program and the hardware created by the user. In the narrow sense, it means hardware only.

Related Document When using this manual, refer to the following manuals.

The related documents indicated in this publication may include preliminary versions.

However, preliminary versions are not marked as such.

- Documents related to development tools (user's manuals)

Document Name		Document Number
IE-V850ES-G1		U16313E
IE-703220-G1-EM1		This manual
CA850 (Ver.2.50 or later) [C Compiler package]	Operation	U16053E
	C Language	U16054E
	PM plus	U16055E
	Assembly Language	U16042E
ID850 (Ver.2.51) [Integrated debugger]	Operation Windows-Based	U16217E
SM850 (Ver.2.50) [System simulator]	Operation Windows-Based	U16218E
RX850 [Real-time OS]	Basics	U13430E
	Installation	U13410E
RX850 Pro [Real-time OS]	Fundamental	U13773E
	Installation	U13774E
RD850 [Task debugger]	Windows-Based	U13737E
RD850 Pro [Task debugger]	Windows-Based	U13916E
AZ850 [System performance analyzer]		U14410E

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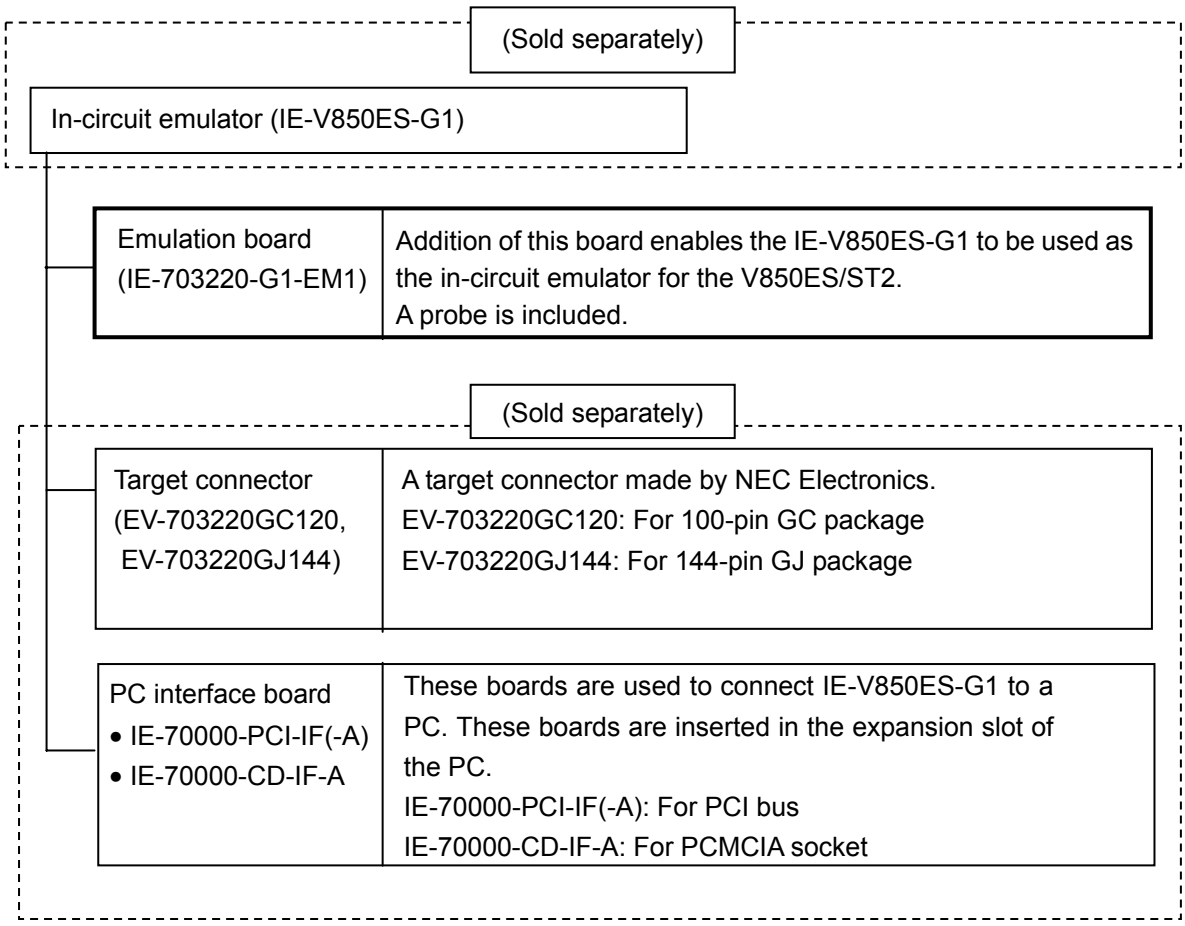
CHAPTER 1 OVERVIEW

The IE-703220-G1-EM1 is an emulation board for the IE-V850ES-G1 in-circuit emulator. By connecting the IE-703220-G1-EM1 and IE-V850ES-G1, hardware and software can be debugged efficiently in system development using the V850ES/ST2.

In this manual, the basic setup procedure and switch settings of the IE-V850ES-G1 when using the IE-703220-G1-EM1 are described. For the names and functions of the parts of the IE-V850ES-G1, and for the connection of elements, refer to the IE-V850ES-G1 User's Manual.

1.1 Hardware Configuration



1.2 Features (When Connected to IE-V850ES-G1)

- Maximum operating frequency: 34 MHz (at 3.0 to 3.6 V operation)
- The following pins can be masked.

  _RESET, NMI
- The dimensions of the IE-703220-G1-EM1 are as follows.

Parameter		Value
External dimensions	Height	35 mm
	Length	205 mm
	Width	140 mm

1.3 Function Specifications (When Connected to IE-V850ES-G1)

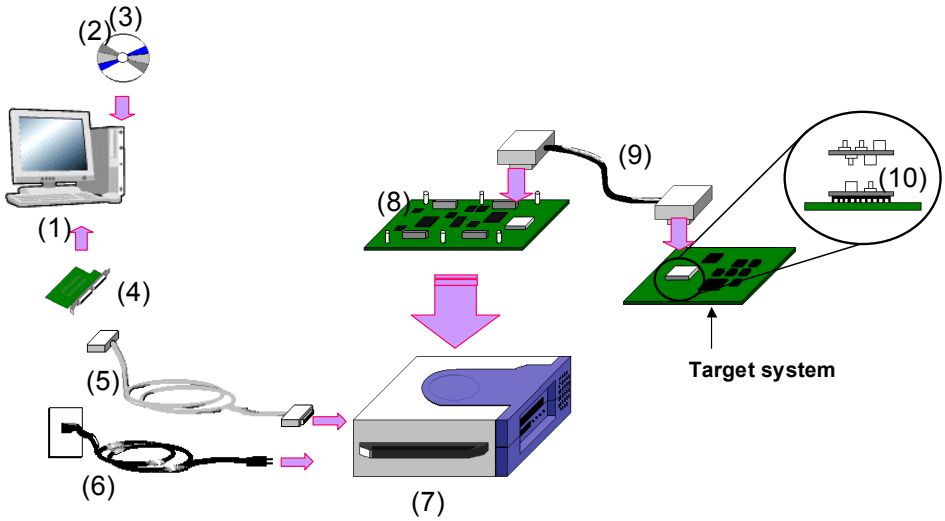
Parameter		Specification
Emulation memory capacity	Internal ROM	0 bytes
	User memory	4 MB
Coverage memory capacity for execution/pass detection	Internal ROM	0 bytes
	External memory	1 MB
Coverage memory capacity for memory access detection	External memory	1 MB
Coverage memory capacity for branching entry number counting	Internal ROM	0 bytes
	External memory	1 MB
Trace memory capacity		168 bits × 32K frames
Time measurement function		On-chip timer: 3
External logic probe		8-bit external trace possible
		Event setting for trace/break possible
Break function		Event break
		Step execute break
		Forced break
		Fail safe break • Illegal access to peripheral I/O • Access to guard space • Write to the ROM space

Caution Some of the functions may not be supported, depending on the debugger used.

1.4 System Configuration

The system configuration when connecting the IE-V850ES-G1 to the IE-703220-G1-EM1 and a PC (PC-9800 series or PC/AT compatible) is shown below.

Figure 1-1. System Configuration



Remark

<1>: PC (PC-9800 series or PC/AT compatibles)

<2>: Debugger (sold separately)

<3>: Device file

<4>: PC interface board (for PCI bus or PCMCIA: Sold separately)

<5>: PC interface cable (included with the IE-V850ES-G1 [sold separately])

<6>: Power supply cable (included with the IE-V850ES-G1 [sold separately])

<7>: In-circuit emulator (IE-V850ES-G1: Sold separately)

<8>: In-circuit emulator emulation board (IE-703220-G1-EM1: This product)

<9>: Probe (included with the IE-703220-G1-EM1)

<10>: EV-703220GC120 (sold separately) or EV-703220GJ144 (sold separately)

1.5 Packing Contents

The packing box contains the emulation board (IE-703220-G1-EM1), package details, user's manual, and guarantee card. If there are any missing or damaged items, please contact an NEC sales representative.

(a) Screws/washers: 6 sets
(6 screws and 6 washers included)

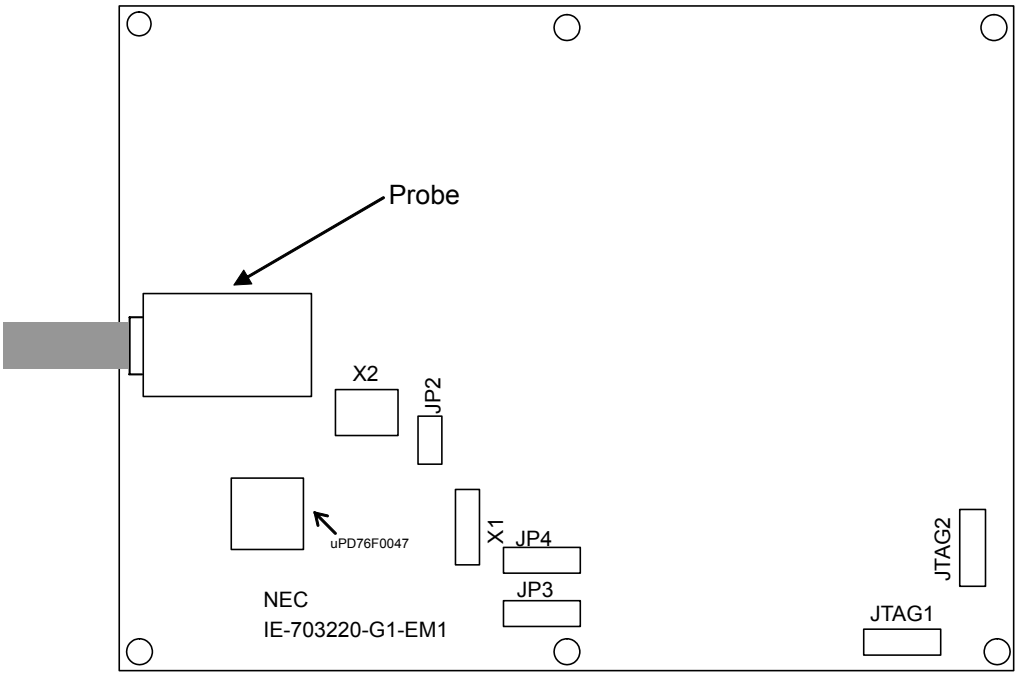
(b) 6-pin single-line socket: 1
(for mounting X1 main clock oscillator)

CHAPTER 2 NAMES AND FUNCTIONS OF PARTS

This chapter describes the names and functions of the parts in the IE-703220-G1-EM1. For details of the IE-V850ES-G1, refer to the IE-V850ES-G1 User's Manual.

2.1 Names and Functions of Parts in IE-703220-G1-EM1

Figure 2-1. Part Names of IE-703220-G1-EM1



(1) X1: This socket is used to mount the main clock oscillator. The oscillator is not mounted at shipment.
(Refer to **3.2 Clock Settings** for details.)

(2) X2: This socket is used to mount the main clock oscillator.
(Refer to **3.2 Clock Settings** for details.)

(3) JP2: This switch is used to select X1 or X2 on the IE-703220-G1-EM1 as the main clock.
(**Default setting: 2-3 shorted**)

(4) JP3: **Use the default setting (3-4 shorted).**

(5) JP4: **Use the default setting (3-4 shorted).**

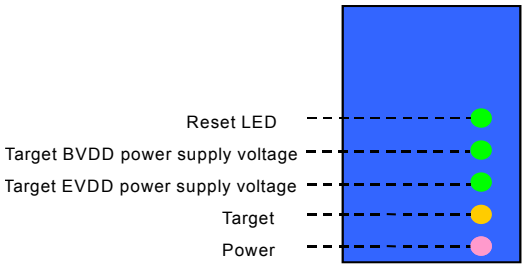
(6) JTAG1: This is a test pin for shipment inspection. Do not change the default setting.
(**Default setting: All pins are left open**)

(7) JTAG2: This is a test pin for shipment inspection. Do not change the default setting.
(**Default setting: All pins are left open**)

2.2 LEDs Controlled by IE-703220-G1-EM1

Some of the LEDs mounted on the IE-V850ES-G1 are controlled by the IE-703220-G1-EM1. Refer to the IE-V850ES-G1 User's Manual for details of the LEDs controlled by the IE-V850ES-G1.

Figure 2-1. LEDs Controlled by IE-703220-G1-EM1



(1) Reset LED

The status of the _RESET signal input from the target system is shown below.

Lit (ON): The target system is connected and the _RESET signal is active (Low level).

Extinguished (OFF): The target system is not connected or the _RESET signal is inactive (High level).

(2) Target BVDD power supply LED

The status of BVDD connected to the target system is shown below.

Lit (ON): The target system is connected and voltage is being applied to BVDD.

Extinguished (OFF): The target system is not connected or voltage is not being applied to BVDD.

(3) Target EVDD power supply LED

The status of EVDD connected to the target system is shown below.

Lit (ON): The target system is connected and voltage is being applied to EVDD.

Extinguished (OFF): The target system is not connected or voltage is not being applied to EVDD.

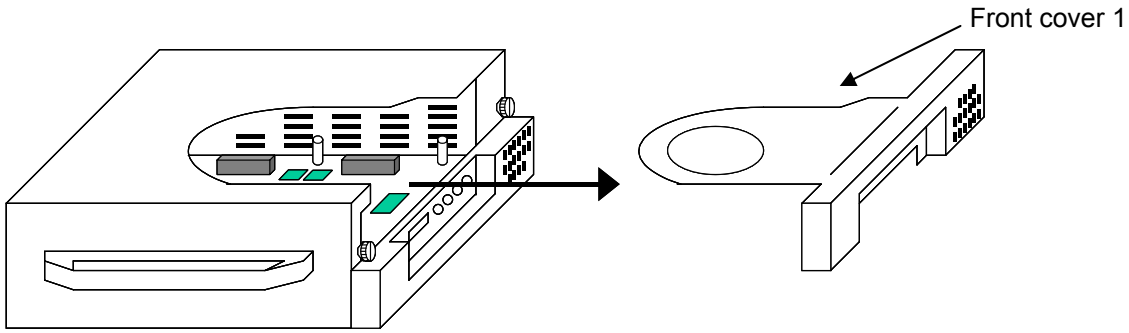
CHAPTER 3 INSTALLATION

This chapter explains how to connect the IE-703220-G1-EM1 to related products and how to exchange the resonators.

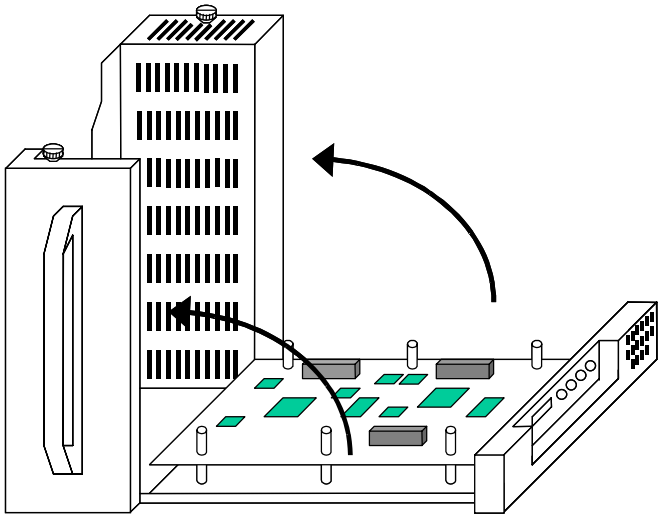
3.1 Connecting IE-V850ES-G1 and IE-703220-G1-EM1

How to connect the IE-V850ES-G1 to the IE-703220-G1-EM1 is shown below.

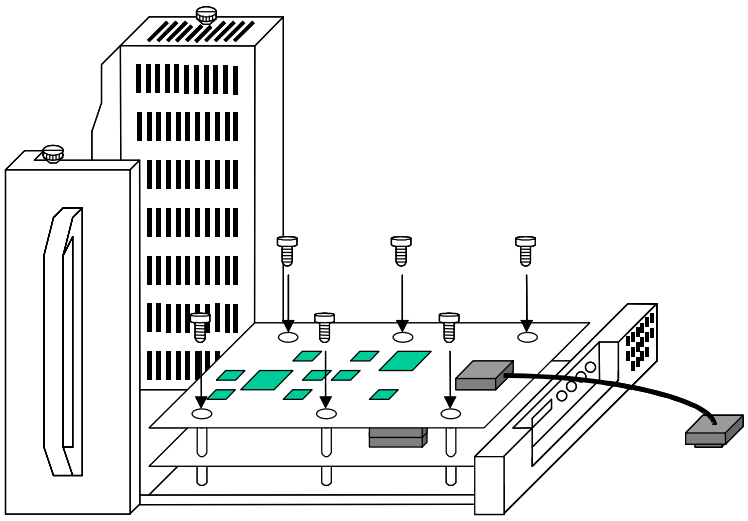
(1) Remove front cover 1 of the IE-V850ES-G1 by putting it out.



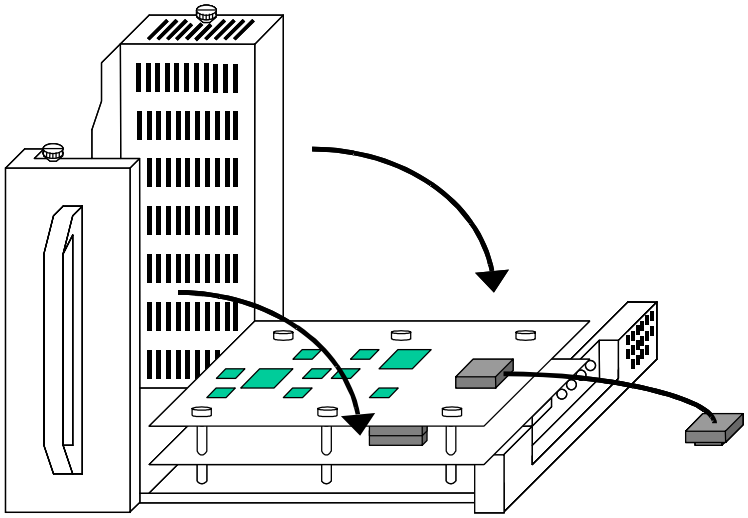
(2) Raise the main unit of the IE-V850ES-G1.



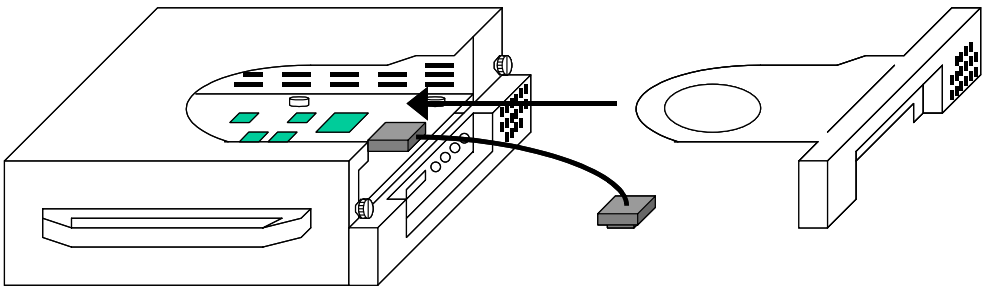
(3) Lay the IE-703220-G1-EM1 horizontally on the main board of the IE-V850ES-G1, align the boards at three connector blocks, and fix them at the six cell spacers using the six screws supplied with the IE-703220-G1-EM1.



(4) Pull down the main unit of the IE-V850ES-G1.



(5) Fix front cover 1 on the IE-V850ES-G1.



3.2 Clock Settings

The IE-703220-G1-EM1 does not support clock input from the target system.

When changing the main clock frequency, therefore, exchange the oscillator mounted on X2 on the IE-703220-G1-EM1 for another oscillator with the desired frequency, or mount the desired oscillator and capacitor in X1.

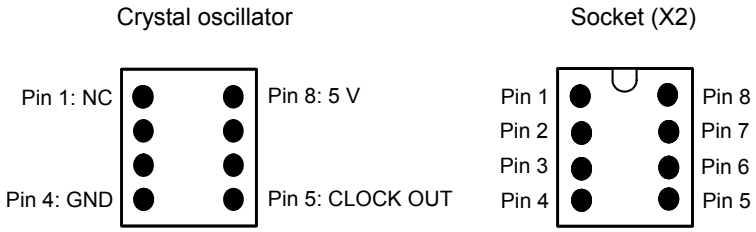
When the product is shipped, the following oscillator is mounted for the main clock.

Item	Settings
X1	No oscillator is mounted.
X2	A 16.9344 MHz oscillator is mounted.

(a) When using X2 as main clock

Mount the crystal oscillator in the socket aligning the pins as shown below.

Set JP2 to 2-3 shorted.



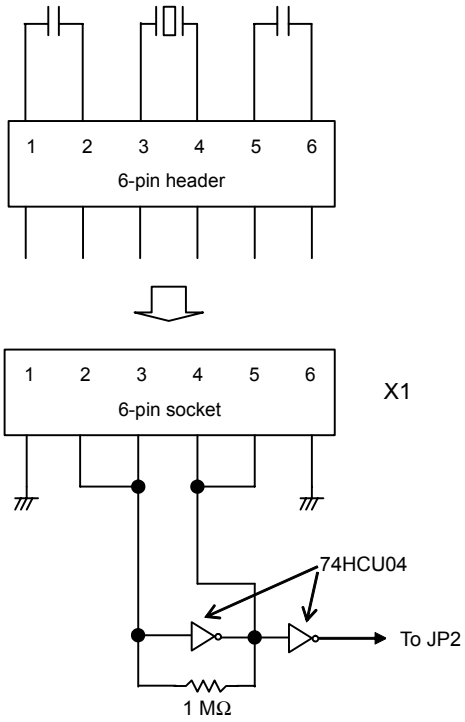
<Top view>

Crystal Oscillator Pin 8-Pin Type	Socket Pin No.
NC	1
GND	4
CLOCK OUT	5
5 V	8

(b) When using X1 as main clock

Mount the ceramic/crystal resonator and capacitor on the attached 6-pin header and mount it on the 6-pin socket on X1 as shown in the figure below.

Set JP2 to 1-2 shorted.



The IE-703220-G1-EM1 does not support clock oscillation by the resonator on the target system. Therefore, the IE-703220-G1-EM1 cannot emulate the operation between the resonator on the target system and oscillator inside the target device.

(c) JP2 setting

This switch is used to select X1 or X2 as the main clock.

Main Clock	JP2 Setting
X1	1-2 shorted
X2	2-3 shorted (at shipment)

CHAPTER 4 CAUTIONS

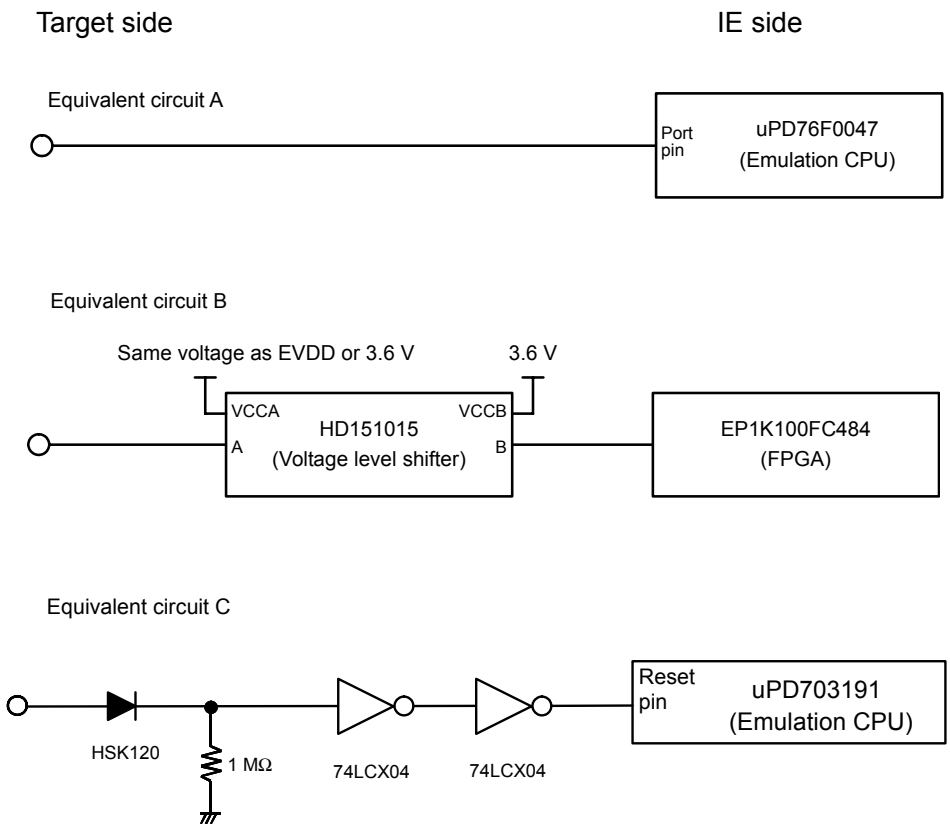
Take note of the following points when using the IE-703220-G1-EM1.

4.1 Connection to Target System

Be sure to turn off the power supply to the IE-V850ES-G1 before connecting it to the target system.

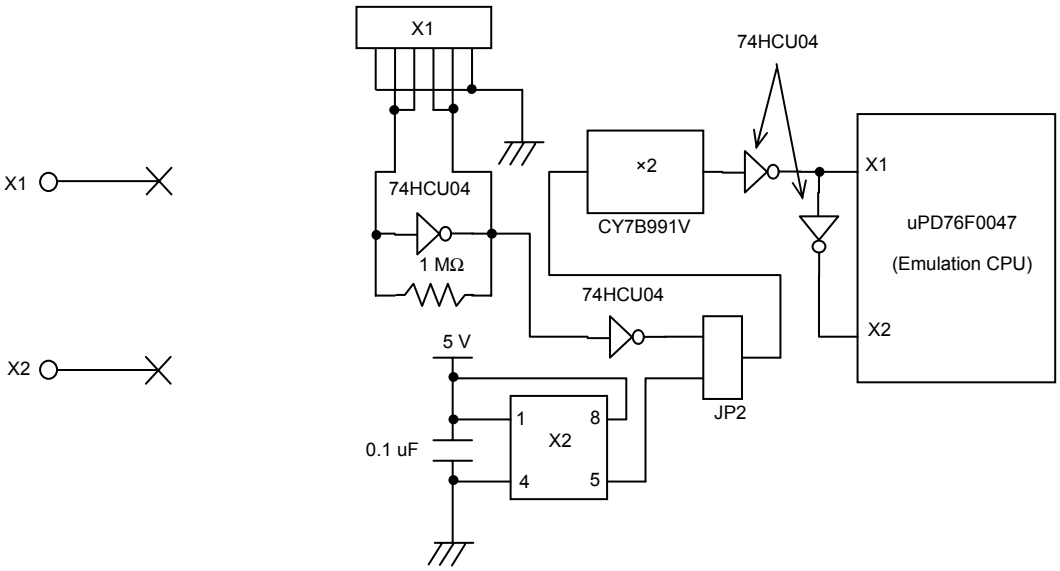
4.2 Characteristics of Target Interface

The target interface (signal to connect the in-circuit emulator and target system) operates, in terms of functions, as if the actual device is connected. In terms of characteristics, however, the operation differs from the actual device. The target interface of the IE-V850ES-G1 is any of the following equivalent circuits A to E. The processing of each target interface is shown in Tables 1 and 2.

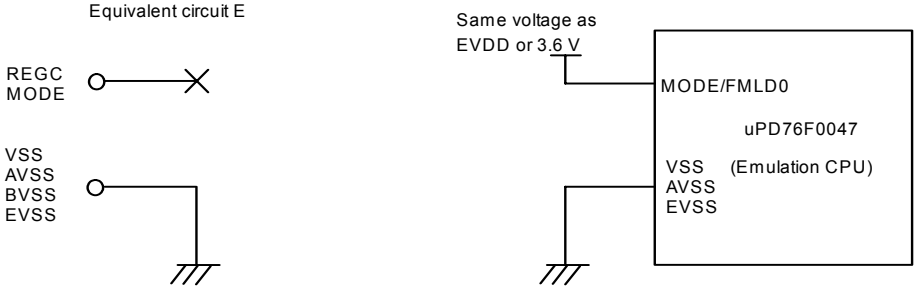


Target side IE side

Equivalent circuit D



Equivalent circuit E



Target interface for V850ES/ST2 in IE-703220-G1-EM1

Table 1. Target Interface Handling for V850ES/ST2 (120-Pin Version) in IE-703220-G1-EM1

Pin No. GC Package	Target Interface	Handling Inside In-Circuit Emulator
1	AVREF0	AVREF0
2	AVSS	Equivalent circuit E
3	P10/ANO0	Equivalent circuit A
4	P11/ANO1	Equivalent circuit A
5	AVREF1	AVREF1
6	P90	Equivalent circuit A
7	P91	Equivalent circuit A
8	P92/TIP41/TOP41	Equivalent circuit A
9	P93/TOP40	Equivalent circuit A
10	P94/TIP31/TOP31	Equivalent circuit A
11	P95/TIP30	Equivalent circuit A
12	P96/TIP21/TOP21	Equivalent circuit A
13	P97/TIP20	Equivalent circuit A
14	EVSS	Equivalent circuit E
15	EVDD	EVDD
16	P98	Equivalent circuit A
17	P99	Equivalent circuit A
18	P910	Equivalent circuit A
19	P911	Equivalent circuit A
20	P912	Equivalent circuit A
21	P913/INTP4	Equivalent circuit A
22	P914/INTP5/TIP51/TOP51	Equivalent circuit A
23	P915/INTP6/TIP50	Equivalent circuit A
24	VSS	Equivalent circuit E
25	REGC	Equivalent circuit E
26	VDD	VDD
27	X1	Equivalent circuit D
28	X2	Equivalent circuit D
29	_RESET	Equivalent circuit C
30	MODE	Equivalent circuit E
31	A21/PDH5	Equivalent circuit B
32	A20/PDH4	Equivalent circuit B
33	A19/PDH3	Equivalent circuit B
34	A18/PDH2	Equivalent circuit B
35	A17/PDH1	Equivalent circuit B
36	A16/PDH0	Equivalent circuit B
37	A15	Equivalent circuit B
38	A14	Equivalent circuit B
39	A13	Equivalent circuit B
40	A12	Equivalent circuit B
41	A11	Equivalent circuit B
42	BVSS	Equivalent circuit E
43	BVDD	BVDD
44	A10	Equivalent circuit B

Pin No. GC Package	Target Interface	Handling Inside In-Circuit Emulator
45	A9	Equivalent circuit B
46	A8	Equivalent circuit B
47	A7	Equivalent circuit B
48	A6	Equivalent circuit B
49	A5	Equivalent circuit B
50	A4	Equivalent circuit B
51	A3	Equivalent circuit B
52	A2	Equivalent circuit B
53	A1	Equivalent circuit B
54	A0	Equivalent circuit B
55	BVSS	Equivalent circuit E
56	BVDD	BVDD
57	PCT6/ASTB	Equivalent circuit B
58	_RD/PCT4	Equivalent circuit B
59	_WR1/PCT1	Equivalent circuit B
60	_WR0/PCT0	Equivalent circuit B
61	_CS0/PCS0	Equivalent circuit B
62	_CS1/PCS1	Equivalent circuit B
63	_CS2/PCS2	Equivalent circuit B
64	_CS3/PCS3	Equivalent circuit B
65	AD15	Equivalent circuit B
66	AD14	Equivalent circuit B
67	AD13	Equivalent circuit B
68	AD12	Equivalent circuit B
69	BVSS	Equivalent circuit E
70	BVDD	BVDD
71	AD11	Equivalent circuit B
72	AD10	Equivalent circuit B
73	AD9	Equivalent circuit B
74	AD8	Equivalent circuit B
75	AD7	Equivalent circuit B
76	AD6	Equivalent circuit B
77	AD5	Equivalent circuit B
78	AD4	Equivalent circuit B
79	BVSS	Equivalent circuit E
80	BVDD	BVDD
81	AD3	Equivalent circuit B
82	AD2	Equivalent circuit B
83	AD1	Equivalent circuit B
84	AD0	Equivalent circuit B
85	_WAIT/PCM0	Equivalent circuit B
86	CLKOUT/PCM1	Equivalent circuit B
87	_HLDAK/PCM2	Equivalent circuit B
88	_HLDRQ/PCM3	Equivalent circuit B
89	P39/RXDA2	Equivalent circuit A
90	P38/TXDA2	Equivalent circuit A
91	P35/TIP11/TOP11	Equivalent circuit A

Pin No. GC Package	Target Interface	Handling Inside In-Circuit Emulator
92	P34/TIP10	Equivalent circuit A
93	P33/TIP01/TOP01	Equivalent circuit A
94	P32/ASCKA0/_SCKB4/TIP00	Equivalent circuit A
95	P31/INTP7/RXDA0/SIB4	Equivalent circuit A
96	P30/TXDA0/SOB4	Equivalent circuit A
97	P42/_SCKB0	Equivalent circuit A
98	P41/SOB0	Equivalent circuit A
99	P40/SIB0	Equivalent circuit A
100	EVSS	Equivalent circuit E
101	EVDD	EVDD
102	P55/RTP05	Equivalent circuit A
103	P54/RTP04	Equivalent circuit A
104	P53/RTP03	Equivalent circuit A
105	P52/RTP02	Equivalent circuit A
106	P51/RTP01	Equivalent circuit A
107	P50/RTP00	Equivalent circuit A
108	P06/INTP3	Equivalent circuit A
109	P05/INTP2	Equivalent circuit A
110	P04/INTP1	Equivalent circuit A
111	P03/INTP0/ADTRG	Equivalent circuit A
112	P02/NMI	Equivalent circuit A
113	P77/ANI7	Equivalent circuit A
114	P76/ANI6	Equivalent circuit A
115	P75/ANI5	Equivalent circuit A
116	P74/ANI4	Equivalent circuit A
117	P73/ANI3	Equivalent circuit A
118	P72/ANI2	Equivalent circuit A
119	P71/ANI1	Equivalent circuit A
120	P70/ANI0	Equivalent circuit A

Target interface for V850ES/ST2 in IE-703220-G1-EM1

Table 2. Target Interface Handling for V850ES/ST2 (144-Pin Version) in IE-703220-G1-EM1

Pin No. GJ Package	Target Interface	Handling Inside In-Circuit Emulator
1	AVREF0	AVREF0
2	AVSS	Equivalent circuit E
3	P10/ANO0	Equivalent circuit A
4	P11/ANO1	Equivalent circuit A
5	AVREF1	AVREF1
6	EVSS	Equivalent circuit E
7	EVSS	Equivalent circuit E
8	P90	Equivalent circuit A
9	P91	Equivalent circuit A
10	P92/TIP41/TOP41	Equivalent circuit A
11	P93/TOP40	Equivalent circuit A
12	P94/TIP31/TOP31	Equivalent circuit A
13	P95/TIP30	Equivalent circuit A
14	P96/TIP21/TOP21	Equivalent circuit A
15	P97/TIP20	Equivalent circuit A
16	EVSS	Equivalent circuit E
17	EVSS	Equivalent circuit E
18	EVDD	EVDD
19	EVDD	EVDD
20	P98	Equivalent circuit A
21	P99	Equivalent circuit A
22	P910	Equivalent circuit A
23	P911	Equivalent circuit A
24	P912	Equivalent circuit A
25	P913/INTP4	Equivalent circuit A
26	P914/INTP5/TIP51/TOP51	Equivalent circuit A
27	P915/INTP6/TIP50	Equivalent circuit A
28	VSS	Equivalent circuit E
29	VSS	Equivalent circuit E
30	REGC	Equivalent circuit E
31	VDD	VDD
32	VDD	VDD
33	X1	Equivalent circuit D
34	X2	Equivalent circuit D
35	_RESET	Equivalent circuit C
36	MODE	Equivalent circuit E
37	A21/PDH5	Equivalent circuit B
38	A20/PDH4	Equivalent circuit B
39	A19/PDH3	Equivalent circuit B
40	A18/PDH2	Equivalent circuit B
41	A17/PDH1	Equivalent circuit B
42	A16/PDH0	Equivalent circuit B
43	EVSS	Equivalent circuit E
44	A15	Equivalent circuit B

Pin No. GJ Package	Target Interface	Handling Inside In-Circuit Emulator
45	A14	Equivalent circuit B
46	A13	Equivalent circuit B
47	A12	Equivalent circuit B
48	A11	Equivalent circuit B
49	BVSS	Equivalent circuit E
50	BVSS	Equivalent circuit E
51	BVDD	BVDD
52	BVDD	BVDD
53	A10	Equivalent circuit B
54	A9	Equivalent circuit B
55	A8	Equivalent circuit B
56	A7	Equivalent circuit B
57	A6	Equivalent circuit B
58	A5	Equivalent circuit B
59	A4	Equivalent circuit B
60	A3	Equivalent circuit B
61	A2	Equivalent circuit B
62	A1	Equivalent circuit B
63	A0	Equivalent circuit B
64	BVSS	Equivalent circuit E
65	BVSS	Equivalent circuit E
66	BVDD	BVDD
67	BVDD	BVDD
68	PCT6/ASTB	Equivalent circuit B
69	_RD/PCT4	Equivalent circuit B
70	_WR1/PCT1	Equivalent circuit B
71	_WR0/PCT0	Equivalent circuit B
72	BVSS	Equivalent circuit E
73	_CS0/PCS0	Equivalent circuit B
74	_CS1/PCS1	Equivalent circuit B
75	_CS2/PCS2	Equivalent circuit B
76	_CS3/PCS3	Equivalent circuit B
77	BVSS	Equivalent circuit E
78	AD15	Equivalent circuit B
79	AD14	Equivalent circuit B
80	AD13	Equivalent circuit B
81	AD12	Equivalent circuit B
82	BVSS	Equivalent circuit E
83	BVSS	Equivalent circuit E
84	BVDD	BVDD
85	BVDD	BVDD
86	AD11	Equivalent circuit B
87	AD10	Equivalent circuit B
88	AD9	Equivalent circuit B
89	AD8	Equivalent circuit B
90	AD7	Equivalent circuit B
91	AD6	Equivalent circuit B

Pin No. GJ Package	Target Interface	Handling Inside In-Circuit Emulator
92	AD5	Equivalent circuit B
93	AD4	Equivalent circuit B
94	BVSS	Equivalent circuit E
95	BVSS	Equivalent circuit E
96	BVDD	BVDD
97	BVDD	BVDD
98	AD3	Equivalent circuit B
99	AD2	Equivalent circuit B
100	AD1	Equivalent circuit B
101	AD0	Equivalent circuit B
102	_WAIT/PCM0	Equivalent circuit B
103	CLKOUT/PCM1	Equivalent circuit B
104	BVSS	Equivalent circuit E
105	_HLDAK/PCM2	Equivalent circuit B
106	_HLDRQ/PCM3	Equivalent circuit B
107	P39/RXDA2	Equivalent circuit A
108	P38/TXDA2	Equivalent circuit A
109	P35/TIP11/TOP11	Equivalent circuit A
110	P34/TIP10	Equivalent circuit A
111	P33/TIP01/TOP01	Equivalent circuit A
112	EVSS	Equivalent circuit E
113	P32/ASCKA0/_SCKB4/TIP00	Equivalent circuit A
114	P31/INTP7/RXDA0/SIB4	Equivalent circuit A
115	P30/TXDA0/SOB4	Equivalent circuit A
116	P42/_SCKB0	Equivalent circuit A
117	P41/SOB0	Equivalent circuit A
118	P40/SIB0	Equivalent circuit A
119	EVSS	Equivalent circuit E
120	EVSS	Equivalent circuit E
121	EVDD	EVDD
122	EVDD	EVDD
123	P55/RTP05	Equivalent circuit A
124	P54/RTP04	Equivalent circuit A
125	P53/RTP03	Equivalent circuit A
126	P52/RTP02	Equivalent circuit A
127	P51/RTP01	Equivalent circuit A
128	P50/RTP00	Equivalent circuit A
129	EVSS	Equivalent circuit E
130	P06/INTP3	Equivalent circuit A
131	P05/INTP2	Equivalent circuit A
132	P04/INTP1	Equivalent circuit A
133	P03/INTP0/ADTRG	Equivalent circuit A
134	P02/NMI	Equivalent circuit A
135	EVSS	Equivalent circuit E
136	EVSS	Equivalent circuit E
137	P77/ANI7	Equivalent circuit A
138	P76/ANI6	Equivalent circuit A

Pin No. GJ Package	Target Interface	Handling Inside In-Circuit Emulator
139	P75/ANI5	Equivalent circuit A
140	P74/ANI4	Equivalent circuit A
141	P73/ANI3	Equivalent circuit A
142	P72/ANI2	Equivalent circuit A
143	P71/ANI1	Equivalent circuit A
144	P70/ANI0	Equivalent circuit A

4.3 Power Application/Power off Procedure

Follow the sequence shown below when activating or terminating the emulator.

- When activating the emulator:

  Power application to the emulator → Power application to the target → Debugger activation

- When terminating the emulator:

  Debugger termination → Power shutdown to the target → Emulator power shutdown

CHAPTER 5 RESTRICTIONS

The IE-703220-G1-EM1 has the following restrictions.

5.1 Clock Generator

(1) Resonator to be connected

Oscillation by a resonator on the target system is not supported. Therefore, the clock oscillation operation on the target system cannot be emulated by the in-circuit emulator.

(2) Emulation of oscillation stabilization time after reset

Oscillation stabilization time is inserted after reset in the emulation target device, but it is not inserted in the in-circuit emulator.

(3) Operating clock after reset

The operating clock after reset is fxx/8 in the emulation target device, but in the in-circuit emulator, there may be a period in which the clock is not reset to fxx/8 (depending on the reset release timing).

5.2 Timing for Setting/Releasing Standby Mode

The timing for setting/releasing standby mode differs between the target device and the in-circuit emulator.
The differences are 1 clock or less for setting and 2 to 3 clocks for release.

5.3 Operation During Break (1)

There may be differences between the operation of the in-circuit emulator and target device because the peripheral functions of the in-circuit emulator operate during a break.
(However, the watchdog timer counter stops when the in-circuit emulator is in a break operation.)

5.4 Operation During Break (2)

The initial values of each port are undefined when the IE system is activated without being connected to the target board.