CUSTOMER NOTIFICATION

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IE-703220-G1-EM1

(Control Code: A)

Operating Precautions

Be sure to read this document before using the product.

Notes on Using IE-703220-G1-EM1

1. Product Version

Control Code	Board Version	Peripheral EVA Chip
A	V1.00	μPD76F0047GC

2. Product History

No.	Bugs and Changes/Additions to Specifications	Control Code[Note]
		A
1	ROM correction function cannot be emulated	Permanent restriction
2	Restriction on use-prohibited area	Permanent restriction
3	Restriction on accessing OSTS register	×
4	Restriction on CLKOUT output in standby mode	×
5	Restriction on INTP3 in standby mode	Permanent restriction
6	Restriction when using multiplexed bus	Permanent restriction
7	Bug in watchdog timer during break	Permanent restriction
8	Bug in 16-bit timer M compare register	Permanent restriction
9	Bug in accessing UAnRX register during break	Permanent restriction
10	Bug in accessing CBnRX register during	Permanent restriction
11	Restriction on control code of IE-V850ES-G1	Supported by IE-V850ES-G1

×: Applicable, √: Not applicable or already corrected

Note The “control code” is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.

3. Details of Bugs and Added Specifications

No.1 ROM correction function cannot be emulated

[Description]

The ROM correction function cannot be emulated.

[Workaround]

There is no workaround. Please regard this item as a permanent restriction.

No.2 Restriction on use-prohibited area

[Description]

The 48 KB area from 3FF3000H to 3FFEFFFH is assigned to the internal RAM area in the V850ES/ST2, but the internal RAM is mounted in the 60 KB area from 3FF0000H to 3FFEFFFH in the emulator. Therefore, there is a RAM that does not exist in the target device in the 12 KB space from 3FF0000H to 3FF2FFFH. Consequently, no non-map breaks can be generated when a program is executed from this area, or when the memory in this area is accessed.

[Workaround]

Set an event break to generate a break when a program is executed from this area, or when the memory in this area is accessed.

Please regard this as a permanent restriction.

No.3 Restriction on accessing OSTS register

[Description]

The OSTS register cannot be written, and 0xD0 is always read when it is read.

[Workaround]

There is no workaround. This restriction is planned for correction in the next version.

No.4 Restriction on CLKOUT output in standby mode

[Description]

Normally a low level is output in standby mode, but the clock is output if the mode is shifted from CLKOUT output mode to standby mode (software STOP or IDLE).

[Workaround]

If outputting CLKOUT in standby mode may cause problems, be sure to set the CLKOUT pin so that it outputs a low level before the mode is shifted from CLKOUT output mode to standby mode using the following procedure.

(1) Clear bit 1 of the PMCCM register to 0 (switches to I/O port)

(2) Clear bit 1 of the PMCM register to 0 (sets output port)

(3) Clear bit 1 of the PCM register to 0 (low-level output)

When this procedure is implemented, set bit 1 of the PMCCM register to 1 immediately after standby release (switching to CLKOUT output mode) to output CLKOUT.

This restriction is planned for correction in the next version.

No.5 Restriction on INTP3 in standby mode

[Description]

When the INTP3 pin is used as an external interrupt pin and a high level (active level) is input to the INTP3 pin two clocks before the standby mode (software STOP or IDLE) is set, normally this input should be ignored, but an INTP3 interrupt is generated.

If INTP3 is used as a trigger for standby release, standby mode is released.

If INTP3 is not used as a trigger for standby release, an INTP3 interrupt is generated immediately after standby mode release.

[Workaround]

Be sure to make the INTP3 pin low level two clocks before the standby mode is set.

Please regard this as a permanent restriction.

No.6 Restriction when using multiplexed bus

[Description]

The number of waits for the V850ES/ST2 must be increased when accessing the external memory while the multiplexed bus is used as shown below.

- Address setup wait: Not necessary to increase the number of waits.
- Address hold wait: Waits must be inserted.
- Data wait: The number of waits must be increased by 2.
- Idle state: Not necessary to increase the number of waits.

This restriction applies to the external memory, but does not apply to the emulation memory incorporated in the emulator.

[Workaround]

There is no workaround. Please regard this as a permanent restriction.

No.7 Bug in watchdog timer during break

[Description]

When a break occurs, the watchdog timer does not stop and a reset or a non-maskable interrupt occurs.

If a reset occurs, the debugger hangs up.

[Workaround]

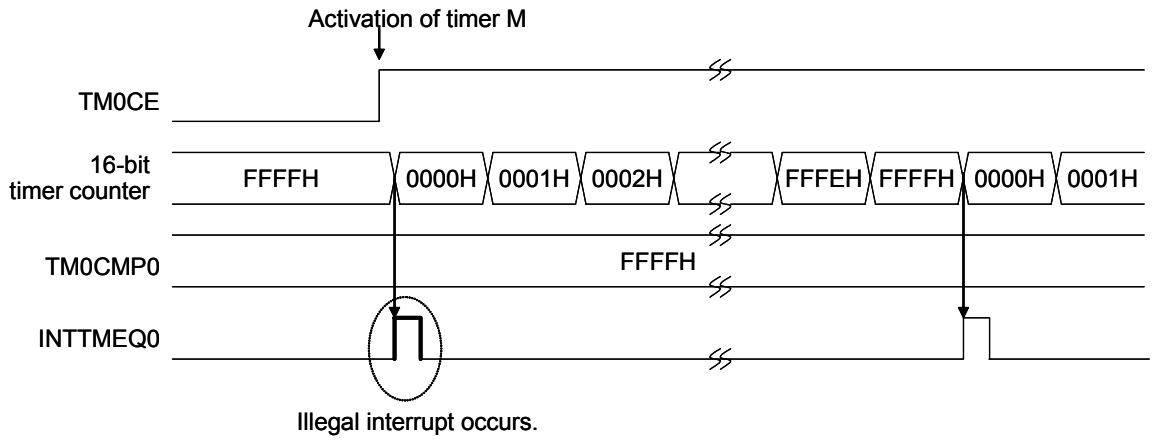
Stop the watchdog timer.

Please regard this item as a permanent restriction.

No.8 Bug in 16-bit timer M compare register

[Description]

An illegal interrupt occurs after timer M activation when the compare register TM0CMP0 is set to FFFFH. See the figure below for details.



[Workaround]

Do not set TM0CMP0 to FFFFH.

Please regard this item as a permanent restriction.

No.9 Bug in accessing UAnRX register during break

[Description]

An overrun error occurs under the following conditions (a) and (b).

(a) If a break occurs after reading the UART receive buffer register (UAnRX) and the UAnRX register is displayed in the I/O register window of the debugger, an overrun error occurs when UART reception is performed next time.

(b) If a software break occurs immediately after reading the UART receive buffer register (UAnRX), an overrun error occurs when UART reception is performed next time regardless of whether or not the UAnRX register is displayed in the I/O register window.

Remark An overrun error also occurs when UART receives data multiple times during a break. This is an emulator specification.

[Workaround]

(a) Do not display the UAnRX register in the I/O register window.

(b) Set a hardware break when setting a break immediately after reading the UAnRX register.

Please regard items (a) and (b) as permanent restrictions.

No.10 Bug in accessing CBnRX register during break

[Description]

When the CSIBn receive data register (CBnRX) is read, it usually starts the next reception operation. If a software break occurs immediately after reading CBnRX, however, the next reception operation is not started. As a result, communication stops.

[Workaround]

Set a hardware break when setting a break immediately after reading the CBnRX register.

Please regard this item as a permanent restriction.

No.11 Restriction on control code of IE-V850ES-G1

[Description]

When the IE-703220-G1-EM1 is used at a frequency of 21 MHz or higher, it does not operate if the control code of the IE-V850ES-G1 (in-circuit emulator main unit) does not match the relevant version.

[Workaround]

An upgrade to the corresponding version is provided separately. Contact the Development Tool Support Center.

E-mail: toolsupport-micom@ml.necel.com.

Please regard this item as a permanent restriction.

4. Cautions

No.1 Caution on ID703000 (ID850)

[Description]

Use V2.51 or later when using the IE-703220-G1-EM1 with the NEC Electronics debugger.