CUSTOMER NOTIFICATION

SUD-TT-0024-1-E (1/3)
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IE-703204-G1-EM1 (Control Code: A)

Operating Precautions

Be sure to read this document before using the product.

Notes on Using IE-703204-G1-EM1

1. Product Version

Part number: IE-703204-G1-EM1

Control Code	Board Version	Peripheral EVA Chip
A	V1.00	UPD70F3204Y ES1.2

2. Product History

No.	Bugs and Changes/Additions to Specification	Control Code [Note]
		A
1	Restriction on A/D converter after conversion is aborted	×
2	Restriction on PRERR flag	Permanent restriction
3	Restriction on reserved area	Permanent restriction

√: Restriction does not apply or already corrected
×: Restriction applies

Note The “control code” is the second digit from the left in the 10-digit serial number in the warranty supplied with the in-circuit emulator you purchased (if it has not been upgraded). If the in-circuit emulator has been upgraded, a label indicating the new version is attached to the in-circuit emulator and the x in V-UP LEVEL x on this label indicates the control code.

3. Details of Bugs and Additions to Specifications

No.1 Restriction on A/D converter after conversion is aborted

[Description]

When an A/D conversion is aborted (ADCS = 0) when it is in progress (ADCS = 1) and the A/D conversion is then resumed, the first conversion result (A/D conversion result register ADCRH, ADCRL) may become illegal.

[Workaround]

Do not reference the first A/D conversion result after the conversion is aborted.

No.2 Restriction on PRERR flag

[Description]

When writing to the WDTM register, the PRERR flag in the SYS register is set even if the write is performed in the specific sequence.

[Workaround]

Do not reference the PRERR flag in the program. If the PRERR flag needs to be referenced, be sure to insert processing to clear the PRERR flag after the WDTM register is written.

No.3 Restriction on reserved area

[Description]

A fail-safe break does not occur even if a program execution or access occurs for 0x3FF8000 to 0x3FFAFFF in the reserved area of the target device.

[Workaround]

Regard this as a permanent restriction.

A break can be generated when a program execution or access occurs by setting a break point on the debugger under the following conditions.

♦ Program execution to 0x3FF8000 to 0x3FFAFFF is detected.
- Event status: Execution
- Address: 0x3ff8000 to 0x3ffafff

(One execution event is used for this setting.)

♦ Access to 0x3FF8000 to 0x3FFAFFF is detected.
- Event status: R/W
- Access size: No Condition
- Address: 0x3ff8000 to 0x3ffafff

(One access event is used for this setting.)

4. Other Cautions

1) Cautions on writing to a specific register

[Description]

Write to the specific registers (PSC, PCC, WDTM, or BPS) in the following procedure.
(Refer to Attachment 1 for details.)

<Procedure to write to a specific register>

<1> Disable the DMA operation.
<2> Prepare the data to be set to the specific register in a general-purpose register.
<3> Write the data prepared in <2> to the command register (PRCMD).
<4> Write the setting data to the specific register (using the following instructions).
- Store instruction (ST/SST instruction)
- Bit manipulation instruction (SET1/CLR1/NOT1 instruction)

<5> Insert 5 NOP instructions (<5> to <9>).
<10> Enable DMA operation if necessary.

2) Cautions on using the ID703000 (ID850)

[Description]

Use V2.41 or later when using the IE-703204-G1-EM1 in combination with the NEC debugger.

1. Cautions on writing to a specific register

The specific registers are registers that are protected from an illegal data write caused by an inadvertent program loop, etc. Writing to the specific registers is performed in a specific sequence, and if an illegal write operation is detected, it is reported to the system status register (SYS). The specific registers targeted in the V850ES/SA2, SA3 are as follows.

- Power save control register (PSC)
- Processor clock control register (PCC)
- Watchdog timer mode register (WDTM)
- Backup power supply power status register (BPS)

Set data to the specific registers in the following sequence.

<Procedure to write to a specific register>

<1> Disable the DMA operation.
<2> Prepare the data to be set to the specific register in a general-purpose register.
<3> Write the data prepared in <2> to the command register (PRCMD).
<4> Write the setting data to the specific register (using the following instructions).
- Store instruction (ST/SST instruction)
- Bit manipulation instruction (SET1/CLR1/NOT1 instruction)

<5> Insert 5 NOP instructions (<5> to <9>).
<10> Enable the DMA operation if it is necessary.

[Example] In the case of the PSC register

```
        ST.B r11, PSMR [r0]    ; Sets the PSMR register
<1>     CLR1 0, DCHCn [r0]     ; DMA operation disabled, n = 0 to 3
<2>     MOV 0x02, r10
<3>     ST.B r10, PRCMD [r0]   ; Writes to the PRCMD register
<4>     ST.B r10, PSC [r0]     ; Sets the PSC register
<5>     NOP                    ; Dummy instruction
<6>     NOP                    ; Dummy instruction
<7>     NOP                    ; Dummy instruction
<8>     NOP                    ; Dummy instruction
<9>     NOP                    ; Dummy instruction
<10>    SET1 0, DCHCn [r0]     ; DMA operation enabled, n = 0 to 3
(next instruction)
```

There is no specific sequence to read a specific register.

Notes 1. No interrupt is acknowledged with a store instruction for the command register.

2. A dummy instruction is used to write to the command register, but be sure to also use the same register as the general-purpose register used to set the specific register (<4> in the example) for writing to the command register (<3> in the example). In addition, use this register when using a general-purpose register for addressing.

3. It is necessary to insert five or more NOP instructions immediately after shifting to IDLE mode or software STOP mode (the STP bit of the PSC register = 1).