CUSTOMER NOTIFICATION

SUD-DT-04-0010 (1/5)

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IE-703166-MC-EM1

(Control Code: A, B, C)

Operating Precautions

Be sure to read this document before using the product.

Notes on Using IE-703166-MC-EM1

1. Product Version

Control Code	Board Version	Peripheral EVA Chip	Remark
A	V1.00	μPD70F3166F1 (ES1.0)	
B	V1.01	μPD70F3166F1 (ES1.0)	
C	V1.02	μPD70F3166F1 (ES1.1)	

Employ an IE-V850ES-G1 with a control code of C or later when using this option board.

2. Product History

No.	Bugs and Changes/Additions to Specifications	Control Code[Note]		
		A	B	C
1	Restriction on operating frequency	×	√	√
2	Bug in CLKOUT output	×	×	√
3	Bug in pseudo separate bus output	×	×	√
4	Bug in releasing software STOP mode forcible break	×	×	√
5	Bug in clocked serial interface (CSIA) with automatic transmission/reception function	×	×	√

×: Applicable, √: Not applicable or already corrected

Note The “control code” is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If the product has been upgraded, the version can be checked by the label attached to the product.

3. Details of Bugs and Added Specifications

No.1 Restriction on operating frequency

[Description]

The maximum operating frequency is 37.5 MHz.

[Workaround]

There is no workaround.

Operation at 40.5 MHz is possible in control code B or later.

No.2 Bug in CLKOUT output

[Description]

The CLKOUT pin outputs an undivided clock (f_{CPU}) regardless of whether the value set to the bus clock division control register (DVC) is 00H ($f_{DV} = f_{CPU}$) or 01H ($f_{DV} = f_{CPU}/2$).

The base clock for the external clock (f_{DV}) is divided by the ratio set to the DVC register. There is no problem in a system in which the external bus is used asynchronous to CLKOUT.

There is no problem in accessing (data read/write) the DVC register.

[Workaround]

In a system in which the external bus is used in synchronization with CLKOUT at $f_{DV} = f_{CPU}/2$, divide the CLKOUT output by 2 using an external circuit and connect it to the target device.

This restriction has been corrected in control code C.

No.3 Bug in pseudo separate bus output

[Description]

An address is not output normally when port 9 is used as the address output bus.

[Workaround]

Use the external bus in multiplexed bus mode.

This restriction has been corrected in control code C.

No.4 Bug in releasing software STOP mode forcible break

[Description]

Software STOP mode cannot be released by a forcible break.

IDLE and HALT modes can be released by a forcible break.

Software STOP mode can be released by a reset, non-maskable interrupt, and an unmasked maskable interrupt that can operate in software STOP mode.

[Workaround]

There is no workaround.

This restriction has been corrected in control code C.

No.5 Bug in clocked serial interface (CSIA) with automatic transmission/reception function

[Description]

When writing transmit data to the buffer RAM (CBUFnm), data may not be written correctly depending on the instruction executed next to the write instruction (n = 0 or 1, m = 0 to 15).

This restriction is not applicable when using CSIA without using the buffer RAM.

[Workaround]

Implement any of the workarounds shown below by software when using the buffer RAM.

This restriction has been corrected in control code C.

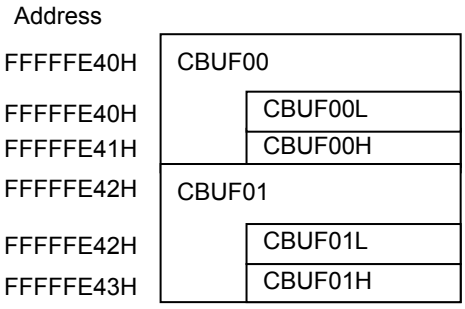
Workaround (1)

After data is written, read the data using the Half_Word access instruction (ST.H) and verify the values. If the data do not match, continue writing until the data match. At this time, it is not necessary to disable interrupts.

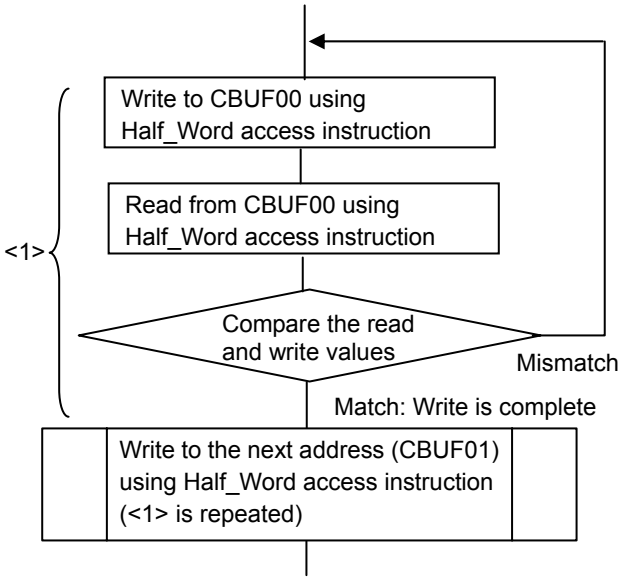
When writing an odd number of bytes, write dummy data to the buffer RAM (CBUFnmH) at the higher address. (n = 0 or 1, m = 0 to 15)

The Half_Word access instruction must be used to access registers until the compare result matches and write is confirmed.

<Example of writing to buffer RAM (CBUF00 to CBUF01)>



Buffer RAM configuration



<Example of writing only 1-byte data (to CBUF00L)>

Perform operation <1> to write data to CBUF00L (the buffer RAM at the lower address), by writing dummy data to CBUF00H (the buffer RAM at the higher address).

Workaround (2)

Disable interrupts using the DI instruction and write data to the buffer RAM using the Half_Word access instruction (ST.H) only. In addition, re-write the last 2 bytes of the written data again. Do not execute instructions other than NOP and operation instructions (arithmetic, saturate, and logical) between when data is written to the buffer RAM and when the last 2 bytes are rewritten.

When writing an odd number of bytes, write dummy data to the buffer RAM (CBUFnmH) at the higher address. (n = 0 or 1, m = 0 to 15)

Workaround (3)

Disable interrupts using the DI instruction and write data to the buffer RAM using the byte access instruction (ST.B) only. In addition, secure a time equivalent to 5 or more input clocks (f_{SCKA}) selected by bits 6 and 7 (CKSAn1 and CKSAn0) of CSISAn by executing a NOP or operation instruction (arithmetic, saturate, or logical) after the last data is written to the buffer RAM. (n = 0 or 1)

This restriction has been corrected in control code C.

4. Cautions

Refer to **CHAPTER 4** in the IE-703166-MC-EM1 User's Manual (U16688) for details of cautions.