CUSTOMER NOTIFICATION

SUD-T-4576-4-E

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IE-703107-MC-EM1
(Control Code: A, B, C)

Operating Precautions

Be sure to read this document before using the product.

Notes on Using IE-703107-MC-EM1

1. Product Version

Product name: IE-703107-MC-EM1

Control Code	Peripheral Chip	Remark
A	UPD70F3107GJ ES1.0	Board version: 1.00
B	UPD70F3107GJ ES2.0	Board version: 1.01
C	UPD70F3107AGJ rank P	Board version: 1.02

Note 1. The control code is indicated by the second character from the left in the 10-character manufacturing code beginning with E.

2. The rank of the UPD70F3107AGJ is indicated by the fifth character from the left in the manufacturing code marked on the peripheral chip.

2. Device Files

The version of the device file to be used depends on the control code for the IE-V850E-MC-A.

IE-V850-MC-A Control Code	Device File Version (μSxxxxDF703107)	Remark
B, C (CPU EVA chip: ES2.0)	V1.10	Can be supported temporarily
D or later (CPU EVA chip: ES3.0 or later)	V1.20	

3. Product History

No.	Restrictions	Control Code		
		A	B	C
1	Restriction on operating frequency	×	√	√
2	Restriction on clock direct mode	×	√	√
3	Restriction on A/D converter	×	√	√
4	Restriction on pin status for single chip mode 1 and ROMless mode 0 and 1	×	√	√
5	Restriction on IORD, IOWR signal	Note 1		
6	Restriction on SFR	Note 1		
7	Restriction in which DMA is started with an interrupt by the integrated peripheral I/O.	Note 2		
8	Restriction on DTOC register read access	×	×	√
9	Restriction on data setup on read access of SDRAM	Note 2		
10	Restriction on external interrupt	×	√	√
11	Restriction on UART	×	√	√

√: Already solved

×: Corresponding restriction exists

Notes 1. This restriction applies when using the IE-V850E-MC-A.
This restriction is not applicable to versions with control code D or later.

2. This restriction applies when using the IE-V850E-MC-A.
This restriction is not applicable to versions with control code F or later.

4. Details of Bugs and Added Specifications

(1) Restriction on operating frequency

<Description> Maximum operating frequency is 40 MHz

<Workaround> There is no workaround at this time.
The control code B product has been removed so that it can operate at 50 MHz.

(2) Restriction on clock direct mode

<Description> The emulator operates at 1/1 of the input clock when direct mode is selected for clock operation mode.

<Workaround> There is no workaround at this time.
This restriction has been removed in products with control code B or later.

(3) Restriction on A/D converter

<Description> A/D conversion may not start even if the A/D conversion operation enable bit (CE bit) of the A/D converter mode register 0 (ADM0) is set to 1.

<Workaround> Set the ADM0 register two times consecutively.
This restriction has been removed in products with control code B or later.

(4) Restriction on pin status for single chip mode 1 and ROMless mode 0 and 1

<Description> When reset is performed in single chip mode 1 or ROMless mode 0 or 1, the prescribed pins will output a specific level without going into a high impedance state. (See the following table.)

<Workaround> There is no workaround.

This restriction has been removed in products with control code B or later.

Operating Status / Pin	Current Status	After Change
	Reset (Single-Chip Mode 1, ROMless Mode 0,1)	Reset (Single-Chip Mode 1, ROMless Mode 0,1)
A0 to A15 (PAL0 to PAL15)	L	Hi-Z
A16 to A25 (PAH0 to PAH9)	L	Hi-Z
D0 to D15 (PDL0 to PDL15)	L	Hi-Z
$\overline{CS0}$ to $\overline{CS7}$ (PCS0 to PCS7)	H	Hi-Z
$\overline{RAS1}$, $\overline{RAS3}$, $\overline{RAS4}$, $\overline{RAS6}$ (PCS1, PCS3, PCS4, PCS6)	–	–
$\overline{IOWR}$ (PCS2)	–	–
$\overline{IORD}$ (PCS5)	–	–
$\overline{LWR}$, $\overline{UWR}$ (PCT0, PCT1)	H	Hi-Z
$\overline{LCAS}$, $\overline{UCAS}$ (PCT0, PCT1)	–	–
LDQM, UDQM (PCT0, PCT1)	–	–
$\overline{RD}$ (PCT4)	H	Hi-Z
$\overline{WE}$ (PCT5)	H	Hi-Z
$\overline{OE}$ (PCT6)	H	Hi-Z
$\overline{BCYST}$ (PCT7)	H	Hi-Z
$\overline{WAIT}$ (PCM0)	H	Hi-Z
CLKOUT (PCM1)	Operates	Operates
BUSCLK (PCM1)	–	–
$\overline{HLDAK}$ (PCM2)	H	Hi-Z
$\overline{HLDRQ}$ (PCM3)	–	Hi-Z
$\overline{REFRQ}$ (PCM4)	H	Hi-Z
SELFREF (PCM5)	–	Hi-Z
SDCKE (PCD0)	L	Hi-Z
SDCLK (PCD1)	Operates	Hi-Z
$\overline{SDCAS}$ (PCD2)	–	–
$\overline{LBE}$ (PCD2)	H	Hi-Z
$\overline{SDRAS}$ (PCD3)	–	–
$\overline{UBE}$ (PCD3)	H	Hi-Z
$\overline{DMAAK0}$ to $\overline{DMAAK3}$ (PBD0 to PBD3)	H	Hi-Z

Remark Hi-z: High impedance
H: High-level output
L: Low-level output
–: Input non-sampling

(5) Restriction on IORD, IOWR signal

<Description> (a) IORD and IOWR pin assignment is reversed.

- V850E/MA1 (device) pin assignment
  - 102-pin: PCS5/_CS5/_IORD
  - 105-pin: PCS2/_CS2/_IOWR
- Emulator pin assignment
  - 102-pin: PCS5/_CS5/_IOWR
  - 105-pin: PCS2/_CS2/_IORD

(b) Ordinarily, IORD and IOWR signals become active during a read/write cycle and DMA flyby transfer, but in this case they become active only during DMA flyby transfer.

<Workaround> (a) Reverse IORD and IOWR in the target system.

(b) There is no workaround at this time.

Both (a) and (b) apply when using the IE-V850E-MC-A, and have been removed in products with control code D or later.

(6) Restriction on SFR

<Description> (a) Although bit 2 and 3 of the PMCT register are supposed to be fixed, they can be rewritten to 0.

(b) Although bit 2 and 3 of the PMCCT register are supposed to be fixed, they can be rewritten to 1.

(c) The initial value of the PMCCT register when started in ROMless mode is 00h instead of F3h.

(Start in port mode, not control mode.)

(d) Port DL is always started in control mode immediately after starting the emulator.

<Workaround> (a) There is no workaround at this time. This restriction applies when using the IE-V850E-MC-A. Please regard it as a permanent restriction.

(b) There is no workaround at this time. This restriction applies when using the IE-V850E-MC-A. Please regard it as a permanent restriction.

(c) Write any bit to 1 if you want to use in control mode when starting in ROMless mode. This restriction is not applicable to versions with control code D or later.

(d) It is possible to change to port mode by writing 0 immediately after starting the ICE. This restriction applies when using the IE-V850E-MC-A, and has been removed in products with control code D or later.

(7) Restriction in which DMA is started with an interrupt by the integrated peripheral I/O.

<Description> A DMA request is retained if an interrupt set to trigger the start of DMA transfer is generated while DMA transfer is prohibited (including abortion by NMI or forced termination by software) when DMA transfer is started by an interrupt from the integrated peripheral I/O. The retained request, however, cannot be cleared. As a result, there is a possibility that an interrupt set to trigger the start of DMA transfer will be generated while DMA transfer is prohibited. If you do not want to start DMA transfer with this interrupt at the stage where DMA transfer is enabled, execute the instructions on the Attachment. In particular, please bear this in mind for cases where one DMA channel is used with multiple applications (start factor is changed while in progress, etc.), DMA transfer is terminated in progress, or forcibly terminated.

<Workaround> Take the following procedure.

(1) Set the DMA trigger factor register (DTFRn) to 00H to prohibit a DMA request from the integrated peripheral I/O.
(2) To perform dummy DMA transfer, set the DMA source address register (DSAn) and the DMA destination address register (DDAn) to a region that does not influence the system.
(3) Set the DMA transfer count register (DBCn) to 0000H.
(4) Set the Enn bit and the STGn bit of the DMA channel control register (DCHCn) to 1, and perform dummy DMA transfer with the software trigger. When doing this, make sure that the MLEn bit of the same register is cleared to 0. This will ensure that dummy DMA transfer is generated along with a DMA transfer completion interrupt (INTDMAn), and the Enn bit will automatically clear to 0.

Note 1: If you do not want to generate a DMA transfer completion interrupt through dummy DMA transfer, set the DMANKn bit of the interrupt control register (DMAICn) to 1 before generating dummy DMA transfer to mask the interrupt.

Note 2: If DMA transfer is reset by a DMA request from the integrated peripheral I/O after a DMA request is cleared, first set the DSAn, DDAn, and DBCn registers, then set the DTFRn register and the Enn bit of the DCHCn register (n = 0 to 3).

This restriction applies when using the IE-V850E-MC-A, and has been removed in products with control code F or later.

(8) Restriction on DTOC register read access

<Description> Both read and write access should be possible on the DTOC register, however now only write access is possible.

<Workaround> Treat the register as a read-only register.

This restriction has been removed in products with control code C or later.

(9) Restriction on data setup on read access of SDRAM

<Description> A minimum data input setup time (tSDRMK) of 10ns is required for the rise of SDCLK when reading SDRAM. (The specification for this chip is 8 ns.)

<Workaround> Ensure a data input setup time (tSDRMK) of 10 ns. Take particular care when using the emulator at 50 MHz.

This restriction applies when using the IE-V850E-MC-A, and has been removed in products with control code F or later.

Following the removal of this restriction, the minimum value of the data input setting time (tSDRMK) is 8 ns.

(10) Restriction on external interrupt

<Description> The INTPn0 pin cannot be used as an external interrupt pin.

<Workaround> Set the CEn bit of timer control register Cn0 (TMCCn0) and start timer C.

This restriction has been removed in products with control code B or later.

(11) Restriction on UART

<Description> When the CAEn bit of asynchronous serial interface mode register n (ASIMn) is 0, a low level is output from the TXDn pin. As a result, the transmission destination side will malfunction at UART activation.

<Workaround> Set the port pin that has an alternate function with the TXDn pin to output port modeand output a high level from that pin. Then, set the CAEn bit to 1 and set the port to the control mode (TXDn pin).

This restriction has been removed in products with control code B or later.

5. Other Cautions

(1) Caution regarding continuous UART transfer

<Description>

The UART in this product has a two-stage buffer configuration consisting of a transmit buffer (TXBn) and a transmit shift register, each of which includes a status flag that indicates the status of the buffer (the TXBFn and TXSFn bits of the ASIFn register). If these two bits are read simultaneously, although "10" changes to "01", depending on the timing, "11" or "00" may be inadvertently read out because the timing at which "10" changes to "01" is in the period in which data is transferred from the transmit buffer to the transmit shift register. As a result, illegal operation may occur in a program that reads data from the TXBFn and TXSFn bits simultaneously.

<Workaround>

When performing continuous transmission, be sure to read only the ASIFn register's TXBFn bit.

(2) Caution regarding SDRAM controller

<Description>

A refresh cycle may be executed for the SDRAM immediately after the RFNn bit of the SDRAM refresh control register (RFSn) is set (1: refresh operation enabled). However, operations during or immediately after the refresh cycle generated at that time are not affected and that subsequent refresh cycles are executed normally at the set interval. (n = 1, 3, 4, 6)

<Workaround>

Operations during or immediately after the refresh cycle generated by the RFSn register's setting are not affected, and subsequent refresh cycles are executed normally at the set interval. However, in applications in which this bug causes problems, take workarounds by setting the RFSn register using the following procedure.

(1) Set the BTn1 and BTn0 bits of the BCTn register to 01 (page ROM connected) while the MEn bit is set (1). (n = 0 to 7)
(2) Set the RENn bit of the RFSn register (1) to enable refresh. (n = 1, 3, 4, 6)
(3) Set the BTn1 and BTn0 bits of the BCTn register to 11 (SDRAM connected) while the MEn bit is set (1). (n = 0 to 7)
(4) Set the SCRn register to initialize the SDRAM. (n = 1, 3, 4, 6)

6. IE-V850E-MC-A Dependent Restrictions

The table below lists the restrictions that apply to the IE-V850E-MC-A. The table shows whether these restrictions are applicable when used for the V850E/MA1.

IE-V850E-MC-A <List of Restrictions>

No.		Restrictions	Applicable/Not Applicable to V850E/MA1				
			IE-V850E-MC-A Applicable Control Code				
			B	C	D	E	F
Restrictions dependent on CPU functions	a-1	Interrupt aborts LD instruction immediately before JMP	×	×	–	–	–
	a-2	Restrictions on IRAM read access after start of interrupt servicing	×	×	–	–	–
	a-3	Fetching is abnormal immediately after writing to SCRn register	×	×	–	–	–
	a-4	Single, line, or single-step transfer of 2-cycle DMA	×	×	–	–	–
	a-5	Port C is not set in control mode immediately after starting in ROMless mode.	×	×	–	–	–
	a-6	Restrictions on Port DH/DL	×	×	–	–	–
	a-7	HLDAK output illegal due to conflict of self-refresh cycle and HOLDRQ in STOP mode	×	×	–	–	–
	a-8	Fetch/data access fails if hardware STOP is executed after CBR refresh of DRAM/SDRAM	×	×	–	–	–
	a-9	Restrictions on data cache	–	–	–	–	–
	a-10	PFCCM register cannot be read.	×	×	–	–	–
	a-11	VSB bus and memory controller (NB85E500/501/502) cannot be used together.	–	–	–	–	–
	a-12	Restrictions on VSB bus signal	×	×	–	–	–
	a-13	Restrictions on NPB bus signal	–	–	–	–	–
	a-14	Restrictions on memory controller (NB85E500) signal	×	×	–	–	–
	a-15	Restrictions on instruction cache	×	×	–	–	–
	a-16	Restrictions related to SDRAM access during bus hold	×	×	–	–	–
	a-17	Restrictions of self-refresh cycle by SELFREF pin	×	×	–	–	–
	a-18	Restrictions related to flyby DMA transfer to EDO DRAM	×	×	–	–	–
	a-19	Restrictions of EDO DRAM with idle state inserted	×	×	–	–	–
	a-20	Restrictions related to flyby DMA transfer	×	×	–	–	–
	a-21	Restrictions of pin status in single-step mode 1 and ROMless modes 0 and 1	×	×	–	–	–
	a-22	When executing a CALLT/SWITCH instruction, LD/SLD instruction write-back is incorrect.	×	×	×	–	–
	a-23	External bus cannot be used when emulator is used for V850E/IA1.	–	–	–	–	–
	a-24	Restriction related to the output of the _DMAAK signal	×	×	×	–	–
	a-25	Restriction related to starting DMA by built-in peripheral I/O interrupt	×	×	×	–	–
	a-26	Restriction related to EDO DRAM bus collision	×	×	×	–	–
	a-27	Restriction on the 2-way associative function of the instruction cache	–	–	–	–	–

No.		Restrictions	Applicable/Not Applicable to V850E/MA1				
			IE-V850E-MC-A Applicable Control Code				
			B	C	D	E	F
Restrictions dependent on CPU functions	a-28	Forced stop of external DMA transfer in DMA line transfer mode	×	×	×	–	–
	a-29	Restriction on reading the DCHC register when DMA 2-cycle transfer is completed	×	×	×	–	–
	a-30	Restriction related to conflict between SDRAM initialization and SELFREF input	×	×	×	–	–
	a-31	Restrictions on half-word writing to BSC, BCC, DWC0, and DWC1 registers	×	×	×	–	–
	a-32	Restriction related to SDRAM write operation	×	×	×	–	–
	a-33	Restriction on DRAM fetch immediately after block DMA transfer from DRAM to internal RAM	×	×	–	–	–
	a-34	Restriction on instruction cache 2	–	–	–	–	–
	a-35	Restriction on SLD instruction	×	×	×	×	–
	a-36	I/O that cannot be used when using a VSB bus	–	–	–	–	–
	a-37	Restriction on instruction cache 3	–	–	–	–	–
	a-38	Restriction of DMAAK signal during DMA line transfer	×	×	×	×	×
	a-39	Restriction caused by interrupt input during execution of bit manipulation instruction	×	×	×	×	–
	a-40	Restriction on hardware stop during bit manipulation instruction execution	–	–	–	–	–
	a-41	Restriction related to interruption of DMA transfer by external cause	×	×	×	×	–
	a-42	Restriction on SDCKE signal during bus hold	×	×	×	×	×

×: Restriction is applicable –: Restriction is not applicable

No.		Restrictions	Applicable/Not Applicable to V850E/MA1				
			IE-V850E-MC-A Applicable Control Code				
			B	C	D	E	F
Restrictions on debug functions	b-1	Restrictions on operating frequency	×	×	×	–	–
	b-2	Restrictions on break timing when guard area is fetched	Permanent restriction				
	b-3	Restrictions on trace in case of mis-alignment (during read access only)	×	×	–	–	–
	b-4	Restrictions on trace data on execution of HALT or STOP instruction	×	×	–	–	–
	b-5	Bit manipulation instruction (set1, clr1, not1, tst1) access data is illegally traced by tracer.	×	×	–	–	–
	b-6	Events including data conditions by access of bit manipulation instruction cannot be detected.	×	×	–	–	–
	b-7	Restrictions on HOLD status	×	×	–	–	–
	b-8	ROM contents are rewritten if emulation ROM area is accessed for write.	Permanent restriction				
	b-9	Restrictions on SFR illegal break	Permanent restriction				
	b-10	Restrictions on programmable I/O space	Permanent restriction				
	b-11	Break does not occur even if breakpoint is set.	Avoided by debugger				
	b-12	Restrictions related to access address during DMA trace	Permanent restriction				
	b-13	Restriction on DBPC and DBPSW access during a break	Permanent restriction				
	b-14	Restriction on DBTRAP instructions	Permanent restriction				
	b-15	Restriction on illegal guard break when IRAM size is 28KB	×	×	×	×	–
	b-16	Restriction on illegal trace when big endian is used	×	×	×	×	–
	b-17	Restriction on access data traced by DMA	Permanent restriction				
	b-18	Restriction on SFR read access during break	Avoided by debugger and device file				

×: Restriction is applicable –: Restriction is not applicable