Microcomputer Technical Information

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IE-703107-MC-EM1 In-Circuit Emulator Option Board for V850E/MA1, V850E/MA2 Usage Restrictions		Document No.	ZBG-CD-04-0005	1/2
		Date issued	May 17, 2004	
		Issued by	Development Tool Group Multipurpose Microcomputer Systems Division 3rd Systems Operations Unit NEC Electronics Corporation	
Related documents	IE-703107-MC-EM1 User's Manual: U14481EJ2V0UM00	Notification classification	√	Usage restriction
				Upgrade
				Document modification
				Other notification

1. Affected product

   IE-703107-MC-EM1 Control code[Note]: A, B, C, D

2. Details of restriction

   This notification concerns the following restriction. See the attachments for details.

   - No.14 Bug in _HLDAK signal output

3. Workaround

   See the attachments for details.

4. Modification schedule

   Products in which No.14 is corrected are scheduled for release as follows.

   Newly shipped products: From the shipment from April, 2004 (control code: E)

   Upgrade for already shipped products: From June, 2004

   * Note that this schedule is subject to change without notice. Contact an NEC Electronics sales representative for the detailed release schedule of modified products.

5. Restriction history

   Notes on using the IE-703107-MC-EM1, including the restriction history and detailed information, will be described on the following pages.

Note The "control code" is the second digit from the left in the 10-digit serial in the warranty supplied with the product you purchased. If the product has been upgraded, the version can be checked by the label attached to the option board.

6. Revision history

IE-703107-MC-EM1 In-Circuit Emulator Option Board for V850E/MA1, V850E/MA2 Usage Restrictions

Document Number	Issued on	Description
SBG-T-1883	January 13, 2000	Newly created.
SBG-T-2459	August 29, 2001	Addition of bugs (No.10 and No.11)
SBG-DT-03-0016	January 29, 2003	Addition of bugs (No.12 and No.13)
ZBG-CD-04-0005 (latest version)	May 17, 2004	Addition of bug (No.14)

Notes on Using IE-703107-MC-EM1

1. Product Version

Product name: IE-703107-MC-EM1

Control Code	Peripheral Chip	Board Version	Remark
A	μPD70F3107GJ ES1.0	1.00	
B	μPD70F3107GJ ES2.0	1.01	
C	μPD70F3107AGJ rank P	1.02	
D	μPD70F3107AGJ rank P	1.12	
E	μPD70F3107AGJ rank P	1.33	

Notes
1. The control code is indicated by the second character from the left in the 10-digit manufacturing code beginning with E (if the product has not been upgraded).
2. The rank of the μPD70F3107AGJ is indicated by the fifth character from the left in the manufacturing code marked on the peripheral chip.
3. The board version is indicated by Ver.X.XX following the manufacturing code of the IE-703107-MC-EM1 (if the product has been upgraded).

2. Device Files

The version of the device file to be used depends on the control code for the IE-V850E-MC-A.

IE-V850-MC-A Control Code	Device File Version (μSxxxxDF703107)	Remark
B, C (CPU EVA chip: ES2.0)	V1.10	Can be downloaded from the NEC Electronics website[Note].
D or later (CPU EVA chip: ES3.0 or later)	V1.20	

Note http://www.necel.com/micro/index_e.html

3. Product History

No.	Restrictions	Control Code				
		A	B	C	D	E
1	Restriction on operating frequency	×	√	√	√	√
2	Restriction on clock direct mode	×	√	√	√	√
3	Restriction on A/D converter	×	√	√	√	√
4	Restriction on pin status for single-chip mode 1 and ROMless modes 0 and 1	×	√	√	√	√
5	Restrictions on IORD and IOWR signals	**Note 1**				
6	Restrictions on SFR	**Note 1**				
7	Restriction in which DMA is started with an interrupt by the integrated peripheral I/O	**Note 2**				
8	Restriction on DTOC register read access	×	×	√	√	√
9	Restriction on data setup on read access of SDRAM	**Note 2**				
10	Restriction on external interrupt	×	√	√	√	√
11	Restriction on UART	×	√	√	√	√
12	Bug related to illegal write access to interrupt control registers **Note 3**	×	×	×	√	√
13	Restriction on A/D converter	Permanent restriction				
14	Bug in _HLDAK signal output	×	×	×	×	√

√: Already solved

×: Corresponding restriction exists

Notes 1. This restriction applies when using the IE-V850E-MC-A.
This restriction is not applicable to versions with control code D or later.

2. This restriction applies when using the IE-V850E-MC-A.
This restriction is not applicable to versions with control code F or later.

3. This bug has been corrected only in the combination of the IE-V850E-MC-A with control code G or later and IE-703107-MC-EM1 with control code D or later.

4. Details of Bugs and Added Specifications

No.1 Restriction on operating frequency

[Description]

Maximum operating frequency is 40 MHz.

[Workaround]

There is no workaround.

The IE-703107-MC-EM1 with control code B has been corrected so that it can operate at 50 MHz.

No.2 Restriction on clock direct mode

[Description]

The emulator operates at 1/1 of the input clock when direct mode is selected for clock operation mode.

[Workaround]

There is no workaround.

This restriction has been corrected in the IE-703107-MC-EM1 with control code B or later.

No.3 Restriction on A/D converter

[Description]

A/D conversion may not start even if the A/D conversion operation enable bit (CE bit) of the A/D converter mode register 0 (ADM0) is set to 1.

[Workaround]

Set the ADM0 register two times consecutively.

This restriction has been corrected in the IE-703107-MC-EM1 with control code B or later.

No.4 Restriction on pin status for single-chip mode 1 and ROMless modes 0 and 1

[Description]

When reset is performed in single-chip mode 1 or ROMless mode 0 or 1, the prescribed pins will output a specific level without going into a high impedance state. (See the following table.)

[Workaround]

There is no workaround.

This restriction has been corrected in the IE-703107-MC-EM1 with control code B or later.

Operating Status / Pin	Current Status	After Change
	Reset (Single-Chip Mode 1, ROMless Mode 0, 1)	Reset (Single-Chip Mode 1, ROMless Mode 0, 1)
A0 to A15 (PAL0 to PAL15)	L	Hi-Z
A16 to A25 (PAH0 to PAH9)	L	Hi-Z
D0 to D15 (PDL0 to PDL15)	L	Hi-Z
$\overline{CS0}$ to $\overline{CS7}$ (PCS0 to PCS7)	H	Hi-Z
$\overline{RAS1}$, $\overline{RAS3}$, $\overline{RAS4}$, $\overline{RAS6}$ (PCS1, PCS3, PCS4, PCS6)	–	–
$\overline{IOWR}$ (PCS2)	–	–
$\overline{IORD}$ (PCS5)	–	–
$\overline{LWR}$, $\overline{UWR}$ (PCT0, PCT1)	H	Hi-Z
$\overline{LCAS}$, $\overline{UCAS}$ (PCT0, PCT1)	–	–
LDQM, UDQM (PCT0, PCT1)	–	–
$\overline{RD}$ (PCT4)	H	Hi-Z
$\overline{WE}$ (PCT5)	H	Hi-Z
$\overline{OE}$ (PCT6)	H	Hi-Z
$\overline{BCYST}$ (PCT7)	H	Hi-Z
$\overline{WAIT}$ (PCM0)	H	Hi-Z
CLKOUT (PCM1)	Operates	Operates
BUSCLK (PCM1)	–	–
$\overline{HLDAK}$ (PCM2)	H	Hi-Z
$\overline{HLDRQ}$ (PCM3)	–	Hi-Z
$\overline{REFRQ}$ (PCM4)	H	Hi-Z
SELFREF (PCM5)	–	Hi-Z
SDCKE (PCD0)	L	Hi-Z
SDCLK (PCD1)	Operates	Hi-Z
$\overline{SDCAS}$ (PCD2)	–	–
$\overline{LBE}$ (PCD2)	H	Hi-Z
$\overline{SDRAS}$ (PCD3)	–	–
$\overline{UBE}$ (PCD3)	H	Hi-Z
$\overline{DMAAK0}$ to $\overline{DMAAK3}$ (PBD0 to PBD3)	H	Hi-Z

Remark Hi-z: High impedance

H: High-level output

L: Low-level output

–: Input non-sampling

No.5 Restrictions on IORD and IOWR signals

[Description]

(a) IORD and IOWR pin assignment is reversed.

- V850E/MA1 (device) pin assignment
  - 102-pin: PCS5/_CS5/_IORD
  - 105-pin: PCS2/_CS2/_IOWR
- Emulator pin assignment
  - 102-pin: PCS5/_CS5/_IOWR
  - 105-pin: PCS2/_CS2/_IORD

(b) Ordinarily, IORD and IOWR signals become active during a read/write cycle and DMA flyby transfer, but in this case they become active only during DMA flyby transfer.

[Workaround]

(a) Reverse IORD and IOWR in the target system.

(b) There is no workaround.

Both (a) and (b) apply when using the IE-V850E-MC-A, and have been corrected in the IE-V850E-MC-A with control code D or later.

No.6 Restrictions on SFR

[Description]

(a) Although bits 2 and 3 of the PMCT register are supposed to be fixed, they can be rewritten to 0.

(b) Although bits 2 and 3 of the PMCCT register are supposed to be fixed, they can be rewritten to 1.

(c) The initial value of the PMCCT register when started in ROMless mode is 00h instead of F3h. (Start in port mode, not control mode.)

(d) Port DL is always started in control mode immediately after starting the emulator.

[Workaround]

(a) There is no workaround. This restriction applies when using the IE-V850E-MC-A. Please regard it as a permanent restriction.

(b) There is no workaround. This restriction applies when using the IE-V850E-MC-A. Please regard it as a permanent restriction.

(c) Write any bit to 1 if you want to use in control mode when starting in ROMless mode. This restriction is not applicable to versions with control code D or later.

(d) It is possible to change to port mode by writing 0 immediately after starting the ICE. This restriction applies when using the IE-V850E-MC-A, and has been corrected in the IE-V850E-MC-A with control code D or later.

No.7 Restriction in which DMA is started with an interrupt by the integrated peripheral I/O

[Description]

A DMA request is retained if an interrupt set to trigger the start of DMA transfer is generated while DMA transfer is prohibited (including abortion by NMI or forced termination by software) when DMA transfer is started by an interrupt from the integrated peripheral I/O. The retained request, however, cannot be cleared. As a result, there is a possibility that an interrupt set to trigger the start of DMA transfer will be generated while DMA transfer is prohibited. If you do not want to start DMA transfer with this interrupt at the stage where DMA transfer is enabled, execute the instructions on the Attachment. In particular, please bear this in mind for cases where one DMA channel is used with multiple applications (start factor is changed while in progress, etc.), DMA transfer is terminated in progress, or forcibly terminated.

[Workaround]

Take the following procedure.

(1) Set the DMA trigger factor register (DTFRn) to 00H to prohibit a DMA request from the integrated peripheral I/O.

(2) To perform dummy DMA transfer, set the DMA source address register (DSAn) and the DMA destination address register (DDAn) to a region that does not influence the system.

(3) Set the DMA transfer count register (DBCn) to 0000H.

(4) Set the Enn bit and the STGn bit of the DMA channel control register (DCHCn) to 1, and perform dummy DMA transfer with the software trigger. When doing this, make sure that the MLEn bit of the same register is cleared to 0. This will ensure that dummy DMA transfer is generated along with a DMA transfer completion interrupt (INTDMAn), and the Enn bit will automatically clear to 0.

Note 1: If you do not want to generate a DMA transfer completion interrupt through dummy DMA transfer, set the DMANKn bit of the interrupt control register (DMAICn) to 1 before generating dummy DMA transfer to mask the interrupt.

Note 2: If DMA transfer is reset by a DMA request from the integrated peripheral I/O after a DMA request is cleared, first set the DSAn, DDAn, and DBCn registers, then set the DTFRn register and the Enn bit of the DCHCn register (n = 0 to 3).

This restriction applies when using the IE-V850E-MC-A, and has been corrected in the IE-V850E-MC-A with control code F or later.

No.8 Restriction on DTOC register read access

[Description]

Both read and write access should be possible on the DTOC register, however now only write access is possible.

[Workaround]

Treat the register as a read-only register.

This restriction has been corrected in the IE-703107-MC-EM1 with control code C or later.

No.9 Restriction on data setup on read access of SDRAM

[Description]

A minimum data input setup time (t_{SDRMK}) of 10ns is required for the rise of SDCLK when reading SDRAM. (The specification for this chip is 8 ns.)

[Workaround]

Ensure a data input setup time (t_{SDRMK}) of 10 ns. Take particular care when using the emulator at 50 MHz.

This restriction applies when using the IE-V850E-MC-A, and has been corrected in the IE-V850E-MC-A with control code F or later.

Following the removal of this restriction, the minimum value of the data input setting time (t_{SDRMK}) is 8 ns.

No.10 Restriction on external interrupt

[Description]

The INTPn0 pin cannot be used as an external interrupt pin.

[Workaround]

Set the CEn bit of timer control register Cn0 (TMCCn0) and start timer C.

This restriction has been corrected in the IE-703107-MC-EM1 with control code B or later.

No.11 Restriction on UART

[Description]

When the CAEn bit of asynchronous serial interface mode register n (ASIMn) is 0, a low level is output from the TXDn pin. As a result, the transmission destination side will malfunction at UART activation.

[Workaround]

Set the port pin that has an alternate function with the TXDn pin to output port mode and output a high level from that pin. Then, set the CAEn bit to 1 and set the port to the control mode (TXDn pin).

This restriction has been corrected in the IE-703107-MC-EM1 with control code B or later.

No.12 Bug related to illegal write access to interrupt control registers

[Description]

When a write access is performed to an interrupt control register (FFFFF110H to FFFFF170H) or interrupt mask register (FFFFF100H to FFFFF107H), the written value may be incorrect.

The occurrence of this bug depends on the combination of the IE-V850E-MC-A and IE-703107-MC-EM1.

[Workaround]

A tool to check whether this bug applies or not is available. See the PDF file included with the check tool for how to use the check tool and workaround when this bug occurs.

Contact the Development Tool Support Center for details.

This bug has been corrected only in the combination of the IE-V850E-MC-A with control code G or later and IE-703107-MC-EM1 with control code D or later.

No.13 Restriction on A/D converter

[Description]

This restriction occurs when the timer 1 trigger mode or external trigger mode of the A/D converter is used (this bug does not occur when the A/D trigger mode or timer 4 trigger mode is used).

Originally, only INTM000 can be the trigger to start the A/D converter in the timer 1 trigger mode, and ADTRG pin input in the external trigger mode, therefore the interrupt sources listed below should be ignored. However, if one of the interrupt sources listed below occurs immediately before the end of A/D conversion (<1> in the figure below; 2 internal system clocks), it is mistakenly judged as the A/D conversion start trigger. As a result, A/D conversion is started again after the A/D conversion end interrupt (INTAD) is issued. The first A/D conversion ends correctly and the result is stored in the ADCRn register (this value can be read during the second conversion).

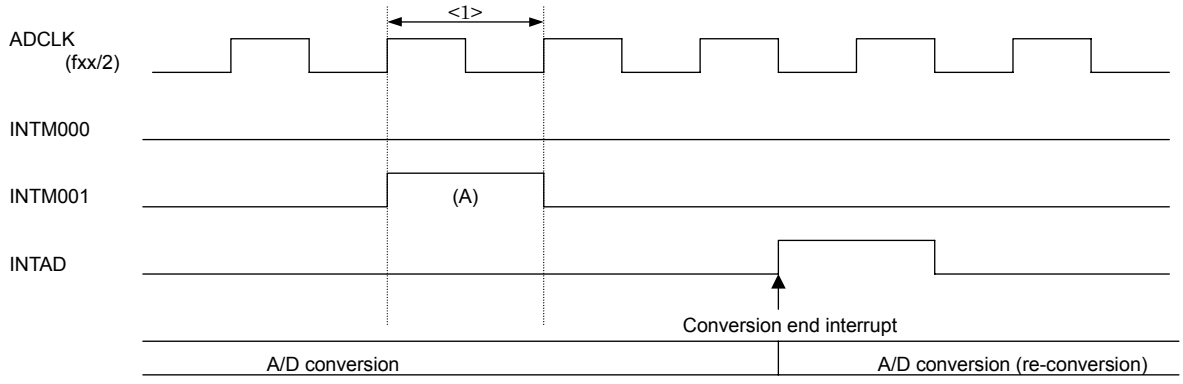
The restarted A/D converter performs the conversion operation correctly, issues the A/D conversion end interrupt (INTAD) and stops. The result is overwritten to the ADCRn register.

[Interrupt source that can trigger A/D conversion]

Timer match interrupt	INTM001
	INTM010
	INTM011
External pin interrupt **Note**	INTP001
	INTP010
	INTP011

Note The external interrupt signal that functions alternately as the external capture trigger input of timer C (channels 0 and 1) can also be a trigger for re-conversion. In the case of an external interrupt input, this bug occurs when a valid edge is input before the timing of (A) in the figure below by the noise eliminator (analog delay (60 to 220 ns)).

[Example of timing at which this bug occurs]



fxx: Internal system clock

[Condition under which this bug does not occur]

This bug does not occur when the A/D trigger mode or timer 4 trigger mode is used.

The Condition under which this bug does not occur in the timer 1 trigger mode or external trigger mode is shown below.

- The compare match interrupt (INTM001/010/011) of timer C (channels 0 and 1) does not occur during A/D conversion, and the external interrupt signal (INTP001/010/011) is not input during A/D conversion.

[Workaround]

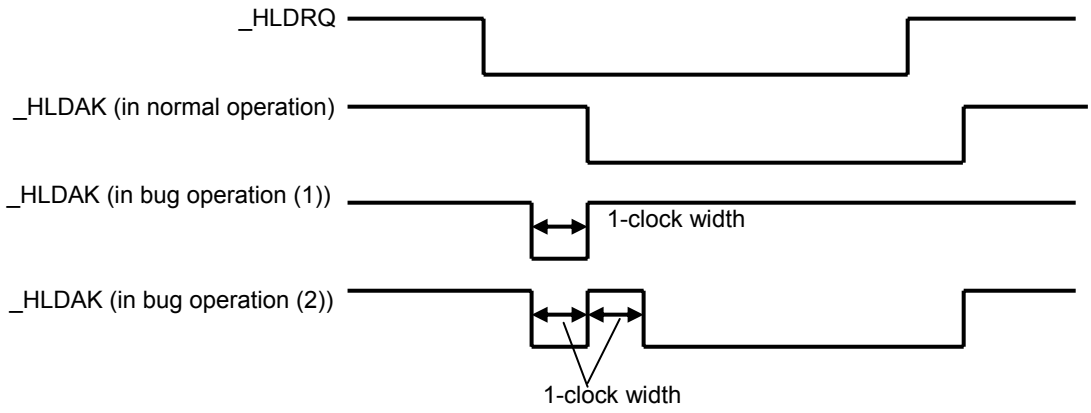
Since the conversion result is correct even when this bug occurs, the affect of this bug is small when obtaining the latest conversion value. If the re-conversion causes any problems, start A/D conversion in the A/D trigger mode by setting the ADCE bit of the ADM0 register to 1 in the interrupt service routine of the timer match interrupt.

No.14 Bug in _HLDAK signal output

[Description]

The _HLDAK signal output from the emulator in response to the _HLDRQ signal from the target system may be illegal (there are two cases).

This bug occurs only when output of the _HLDAK signal and refresh conflict.



[Workaround]

There is no workaround.

This restriction has been corrected in the IE-703107-MC-EM1 with control code E or later.

The function of JP4 that is provided in control code E (V1.33) is described below.

♦ Description of JP4 function

2-3 shorted: Setting to prevent _HLDAK illegal output

1-2 shorted: Setting functions other than above (factory setting)

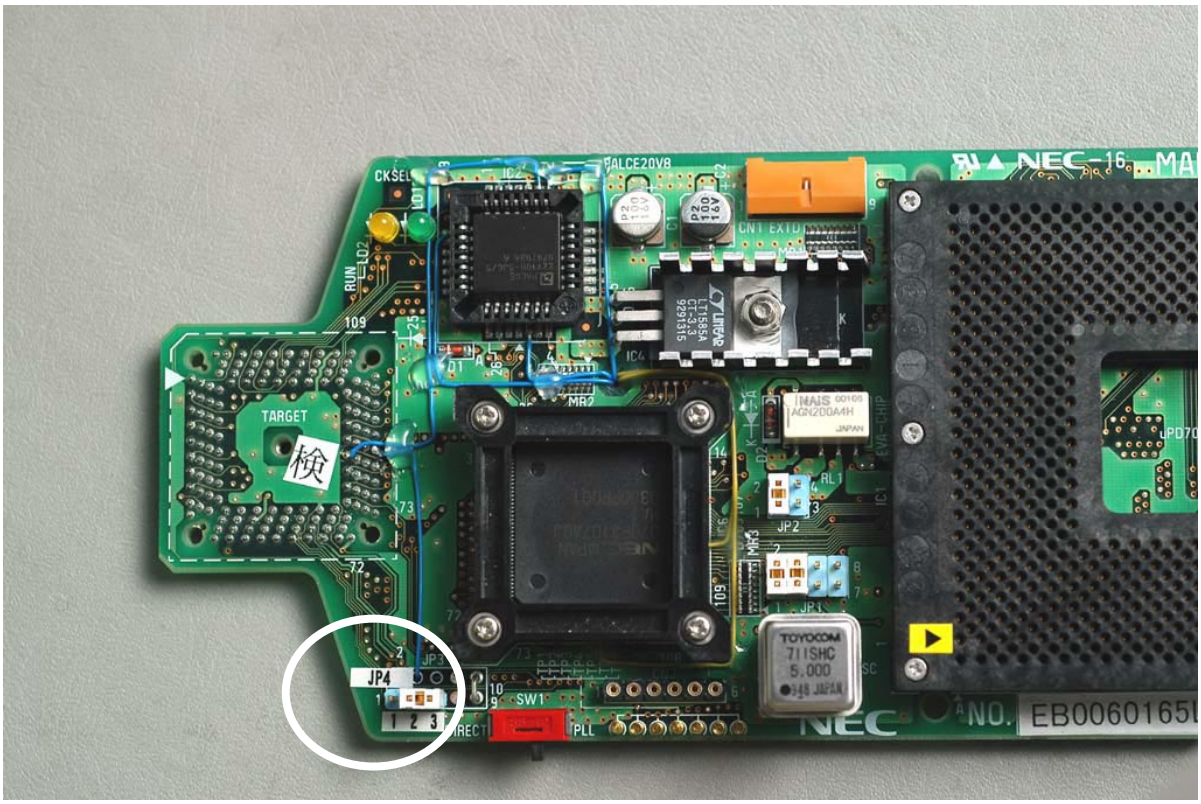
(1) Set 2-3 shorted only for the following system.

- A system in which DRAM or SDRAM is connected to the external bus and the bus hold function is used.

(2) Set 1-2 shorted for systems other than above.

- A system in which DRAM or SDRAM is connected to the external bus and the bus hold function is not used.
- A system in which a device other than DRAM or SDRAM is connected to the external bus.
- A system which is used by the port function.

♦ JP4 position



5. Cautions

No.1 Caution regarding continuous UART transfer

[Description]

The UART in this product has a two-stage buffer configuration consisting of a transmit buffer (TXBn) and a transmit shift register, each of which includes a status flag that indicates the status of the buffer (the TXBFn and TXSFn bits of the ASIFn register). If these two bits are read simultaneously, although "10" changes to "01", depending on the timing, "11" or "00" may be inadvertently read out because the timing at which "10" changes to "01" is in the period in which data is transferred from the transmit buffer to the transmit shift register. As a result, illegal operation may occur in a program that reads data from the TXBFn and TXSFn bits simultaneously.

[Workaround]

When performing continuous transmission, be sure to read only the ASIFn register's TXBFn bit.

No.2 Caution regarding SDRAM controller

[Description]

A refresh cycle may be executed for the SDRAM immediately after the RFNn bit of the SDRAM refresh control register (RFSn) is set (1: refresh operation enabled). However, operations during or immediately after the refresh cycle generated at that time are not affected and that subsequent refresh cycles are executed normally at the set interval. (n = 1, 3, 4, 6)

[Workaround]

Operations during or immediately after the refresh cycle generated by the RFSn register's setting are not affected, and subsequent refresh cycles are executed normally at the set interval. However, in applications in which this bug causes problems, take workarounds by setting the RFSn register using the following procedure.

(1) Set the BTn1 and BTn0 bits of the BCTn register to 01 (page ROM connected) while the MEn bit is set (1). (n = 0 to 7)
(2) Set the RENn bit of the RFSn register (1) to enable refresh. (n = 1, 3, 4, 6)
(3) Set the BTn1 and BTn0 bits of the BCTn register to 11 (SDRAM connected) while the MEn bit is set (1). (n = 0 to 7)
(4) Set the SCRn register to initialize the SDRAM. (n = 1, 3, 4, 6)

6. IE-V850E-MC-A Dependent Restrictions

The table below lists the restrictions that apply to the IE-V850E-MC-A. The table shows whether these restrictions are applicable when used for the V850E/MA1. See the document **IE-V850E-MC, IE-V850E-MC-A Usage Restrictions**.

	No.	Restrictions	IE-V850E-MC-A Control Code					
			B	C	D	E	F	G
Restrictions dependent on CPU functions	a-1	Interrupt aborts LD instruction immediately before JMP	×	×	√	√	√	√
	a-2	Restrictions on IRAM read access after start of interrupt servicing	×	×	√	√	√	√
	a-3	Fetching is abnormal immediately after writing to SCRn register	×	×	√	√	√	√
	a-4	Single, line, or single-step transfer of 2-cycle DMA	×	×	√	√	√	√
	a-5	Port C is not set in control mode immediately after starting in ROMless mode.	×	×	√	√	√	√
	a-6	Restrictions on ports DH and DL	×	×	√	√	√	√
	a-7	HLDAK output illegal due to conflict of self-refresh cycle and HOLDRQ in STOP mode	×	×	√	√	√	√
	a-8	Fetch/data access fails if hardware STOP is executed after CBR refresh of DRAM/SDRAM	×	×	√	√	√	√
	a-9	Restrictions on data cache	Not relevant					
	a-10	PFCCM register cannot be read.	×	×	√	√	√	√
	a-11	VSB bus and memory controller (NB85E500/501/502) cannot be used together.	Not relevant					
	a-12	Restrictions on VSB bus signal	Not relevant					
	a-13	Restrictions on NPB bus signal	Not relevant					
	a-14	Restrictions on memory controller (NB85E500) signal	×	×	√	√	√	√
	a-15	Restrictions on instruction cache	Not relevant					
	a-16	Restriction on SDRAM access during bus hold	×	×	√	√	√	√
	a-17	Restriction on self-refresh cycle by SELFREF pin	×	×	√	√	√	√
	a-18	Restriction on flyby DMA transfer to EDO DRAM	×	×	√	√	√	√
	a-19	Restriction on EDO DRAM with idle state inserted	×	×	√	√	√	√
	a-20	Restriction on flyby DMA transfer	×	×	√	√	√	√
	a-21	Restriction on pin status in single-step mode 1 and ROMless modes 0 and 1	×	×	√	√	√	√
	a-22	When executing a CALLT/SWITCH instruction, LD/SLD instruction writeback is incorrect.	×	×	×	√	√	√
	a-23	External bus cannot be used when emulator is used for V850E/IA1.	Not relevant					
	a-24	Restriction on output of the _DMAAK signal	×	×	×	√	√	√
	a-25	Restriction on starting DMA by built-in peripheral I/O interrupt	×	×	×	√	√	√
	a-26	Restriction on EDO DRAM bus collision	×	×	×	√	√	√
	a-27	Restriction on the 2-way associative function of the instruction cache	Not relevant					

×: Restriction is applicable √: Restriction has been corrected

	No.	Restrictions	IE-V850E-MC-A Control Code					
			B	C	D	E	F	G
Restrictions dependent on CPU functions	a-28	Forced stop of external DMA transfer in DMA line transfer mode	Not relevant					
	a-29	Restriction on reading the DCHC register when DMA 2-cycle transfer is complete	×	×	×	√	√	√
	a-30	Restriction on conflict between SDRAM initialization and SELFREF input	×	×	×	√	√	√
	a-31	Restriction on halfword writing to BSC, BCC, DWC0, and DWC1 registers	×	×	×	√	√	√
	a-32	Restriction on SDRAM write operation	×	×	×	√	√	√
	a-33	Restriction on DRAM fetch immediately after block DMA transfer from DRAM to internal RAM	×	×	√	√	√	√
	a-34	Restriction on instruction cache (2)	Not relevant					
	a-35	Restriction on SLD instruction	×	×	×	×	√	√
	a-36	I/O that cannot be used when using a VSB bus	Not relevant					
	a-37	Restriction on instruction cache (3)	Not relevant					
	a-38	Restriction on DMAAK signal during DMA line transfer	Not relevant					
	a-39	Restriction caused by interrupt input during execution of bit manipulation instruction	×	×	×	×	√	√
	a-40	Restriction on hardware stop during bit manipulation instruction execution	Not relevant					
	a-41	Restriction related to interruption of DMA transfer by external cause	×	×	×	×	√	√
	a-42	Restriction on SDCKE signal during bus hold	×	×	×	×	×	√
	a-43	Caution regarding SDRAM controller	Permanent restriction					
	a-44	Restriction on mul/mulu instruction	Permanent restriction					
	a-45	Restriction on page ROM access	Permanent restriction					
	a-46	Bug related to DMA transfer forcible termination	Permanent restriction					
	a-47	Bug that DMA transfer is forcibly suspended by NMI	Permanent restriction					
	a-48	Bug in program execution and DMA transfer in internal RAM	Permanent restriction					
	a-49	Bug related to DMA transfer whose transfer count is set to two (1)	Permanent restriction					
	a-50	Bug related to DMA transfer whose transfer count is set to two (2)	Permanent restriction					
	a-51	Bug that TCn bit of DMA is not cleared automatically	Permanent restriction					

×: Restriction is applicable √: Restriction has been corrected

No.		Restrictions	IE-V850E-MC-A Control Code					
			B	C	D	E	F	G
Restrictions on debug functions	b-1	Restriction on operating frequency	×	×	×	√	√	√
	b-2	Restriction on break timing when guarded area is fetched	Permanent restriction					
	b-3	Restriction on trace in case of mis-alignment (during read access only)	×	×	√	√	√	√
	b-4	Restrictions on trace data on execution of HALT or STOP instruction	×	×	√	√	√	√
	b-5	Bit manipulation instruction (set1, clr1, not1, tst1) access data is illegally traced by tracer.	×	×	√	√	√	√
	b-6	Events including data conditions by access of bit manipulation instruction cannot be detected.	×	×	√	√	√	√
	b-7	Restriction on HOLD status	×	×	√	√	√	√
	b-8	ROM contents are rewritten if emulation ROM area is accessed for write.	Permanent restriction					
	b-9	Restriction on SFR illegal break	Not relevant					
	b-10	Restrictions on programmable I/O space	Permanent restriction					
	b-11	Break does not occur even if breakpoint is set.	Avoided by debugger					
	b-12	Restriction related to access address during DMA trace	Permanent restriction					
	b-13	Restriction on DBPC and DBPSW access during a break	Permanent restriction					
	b-14	Restriction on DBTRAP instructions	Permanent restriction					
	b-15	Restriction on illegal guard break when IRAM size is 28 KB	×	×	×	×	√	√
	b-16	Restriction on illegal trace when big endian is used	×	×	×	×	√	√
	b-17	Restriction on access data traced by DMA	Permanent restriction					
	b-18	Restriction on SFR read access during break	Avoided by debugger and device file					

×: Restriction is applicable √: Restriction has been corrected