Microcomputer Technical Information

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IE-703079-MC-EM1 In-Circuit Emulator Option Board for V850/SF1 Usage Restrictions		Document No.	ZBG-CD-04-0003		1/2
		Date issued	May 14, 2004		
		Issued by	Development Tool Group Multipurpose Microcomputer Systems Division 3rd Systems Operations Unit NEC Electronics Corporation		
Related documents	IE-703079-MC-EM1 User's Manual: U15447EJ1V0UM00	Notification classification	√	Usage restriction	
				Upgrade	
				Document modification	
				Other notification	

1. Affected product

IE-703079-MC-EM1 Control code[Note]: A, B, C, D, E, F, G, H

2. Details of restriction

This notification concerns the following restriction. See the attachments for details.

- No.17 Bug in accessing FCAN area

3. Workaround

See the attachments for details.

4. Modification schedule

Products in which No.17 is corrected are scheduled for release as follows.

Newly shipped products: From the shipment from February, 2004 (control code: J)

Upgrade for already shipped products: From June, 2004

* Note that this schedule is subject to change without notice. Contact an NEC Electronics sales representative for the detailed release schedule of modified products.

5. Restriction history

Notes on using the IE-703079-MC-EM1, including the restriction history and detailed information, will be described on the following pages.

Note The "control code" is the second digit from the left in the 10-digit serial in the warranty supplied with the product you purchased. If the product has been upgraded, the version can be checked by the label attached to the option board.

6. Revision history

IE-703079-MC-EM1 In-Circuit Emulator Option Board for V850/SF1 Usage Restrictions

Document Number	Issued on	Description
SBG-T-2173	October 11, 2000	Newly created. (Control code A, B, C)
SBG-T-2252	January 31, 2001	Addition of bug (No.10)
SBG-TT-0115	May 31, 2002	Addition of bugs (No.11 to No.15)
SBG-TT-0159	July 19, 2002	Addition of bug (No.16)
ZBG-CD-04-0003 (latest version)	May 14, 2004	Addition of bug (No.17)

Notes on Using IE-703079-MC-EM1

1. Product Version

Control Code	Board Version	Peripheral Chip	Remark
A	1.00	μPD70F3079Y (DS1.0)	
B	1.01	μPD70F3079Y (DS1.1)	
C	1.02	μPD70F3079Y (ES1.1)	
D	1.03	μPD70F3079Y (ES1.1)	
E	1.04	μPD70F3079Y (DS2.0)	
F	1.24	μPD70F3079AY (DS1.1)	
G	1.34	μPD70F3079AY (DS1.1)	
H	1.44	μPD70F3079AY (DS1.1)	
J	1.55	μPD70F3079AY (DS1.1)	

Employ an IE-703002-MC with a control code of H or later when using this option board.

2. Product History

No.	Bugs and Changes/Additions to Specifications	Control Code								
		A	B	C	D	E	F	G	H	J
1	P0.0 cannot be used	×	√	√	√	√	√	√	√	√
2	POC function cannot be used	Permanent restriction								
3	When FCAN memory is accessed, bus cycle is output from the external expansion pin	Permanent restriction								
4	Restriction on P4, P5, P6, P9, and P11 in input mode	×	√	√	√	√	√	√	√	√
5	Restriction when P11 is set as an alternate function pin	×	×	√	√	√	√	√	√	√
6	The high-level signal output from P0.0 is lower than the PortV_{DD} potential by about 1 V	×	×	×	√	√	√	√	√	√
7	The high-level signal output from P0.0 is fixed at 5 V	Permanent restriction								
8	Restriction on the FCAN function when the WAIT pin is used	×	×	×	√	√	√	√	√	√
9	Caution when FCAN memory is accessed	×	×	×	×	√	√	√	√	√
10	Restriction on external clock	Permanent restriction								
11	ROM correction function cannot be emulated	Permanent restriction								
12	Emulation during oscillation stabilization time after RESET release cannot be performed	Permanent restriction								
13	Restriction on interrupts in STOP/IDLE mode	×	×	×	×	×	×	√	√	√
14	Modification of emulation target CPU	×	×	×	×	×	√	√	√	√
15	Hi-Z output from the CLKOUT pin cannot be emulated	Permanent restriction								
16	Bug in external bus interface	×	×	×	×	×	×	×	√	√
17	Bug in accessing FCAN area	√	√	√	√	√	√	√	×	√

×: Applicable, √: Not applicable or already corrected

The “control code” is the second digit from the left in the 10-digit serial in the warranty supplied with the product you purchased. If the product has been upgraded, the version can be checked by the label attached to the option board.

3. Details of Bugs and Added Specifications

No.1 P0.0 cannot be used

[Description]

P0.0 cannot be used.

[Workaround]

There is no workaround.

This bug has been corrected in control code B.

No.2 POC function cannot be used

[Description]

POC function cannot be used.

[Workaround]

There is no workaround.

This will be designated as a permanent restriction.

No.3 When FCAN memory is accessed, bus cycle is output from the external expansion pin

[Description]

When FCAN memory is accessed, bus cycle is output from the external expansion pin.

[Workaround]

There is no workaround.

This will be designated as a permanent restriction.

No.4 Restriction on P4, P5, P6, P9, and P11 in input mode

[Description]

If P4, P5, P6, P9, and P11 are in input mode, the potential of the pins is lowered even if a pull-up resistor is connected on the target system (approx. 2.5 to 4 V).

[Workaround]

There is no workaround.

This bug has been corrected in control code B.

No.5 Restriction when P11 is set as an alternate function pin

[Description]

If PM11 is set to output mode while P11 is set as a multiplexed pin (CAN control pin), the potential of the low-level output signal is not lowered to less than 2.5 V.

[Workaround]

There is no workaround.

This bug has been corrected in control code C.

No.6 The high-level signal output from P0.0 is lower than the PortV_{DD} potential by about 1 V

[Description]

The high-level signal output from P0.0 is lower than the PortV_{DD} potential by about 1 V.

[Workaround]

There is no workaround.

This bug has been corrected in control code D.

No.7 The high-level signal output from P0.0 is fixed at 5 V

[Description]

The high-level output from P0.0 is fixed at 5 V regardless of PortV_{DD}.

[Workaround]

There is no workaround.

This will be designated as a permanent restriction.

No.8 Restriction on the FCAN function when the WAIT pin is used

[Description]

The FCAN function cannot be used if the WAC flag of the PAC register is set to the WAIT pin.

[Workaround]

There is no workaround.

This bug has been corrected in the control code D.

No.9 Caution when FCAN memory is accessed

[Description]

The in-circuit emulator deadlocks if addresses between 0xnffe00 and 0xnffffff (n = 3, 7, b) of the FCAN address area are accessed (this area is unusable).

[Workaround]

Do not access addresses between 0xnffe00 and 0xnffffff (n = 3, 7, b).

This bug has been corrected in control code E.

No.10 Restriction on external clock

[Description]

Emulation cannot be performed externally with the main clock or the subclock.

[Workaround]

Use the clock in the emulator.

This will be designated as a permanent restriction.

No.11 ROM correction function cannot be emulated

[Description]

The ROM correction function cannot be emulated.

[Workaround]

There is no workaround.

This will be designated as a permanent restriction.

No.12 Emulation during oscillation stabilization time after RESET release cannot be performed

[Description]

Emulation during the oscillation stabilization time after RESET release cannot be performed.

Emulation during the oscillation stabilization time after STOP mode release is possible.

[Workaround]

There is no workaround.

This will be designated as a permanent restriction.

No.13 Restriction on interrupts in STOP/IDLE mode

[Description]

The emulator deadlocks if the device is shifted to the STOP/IDLE mode while the interrupt request flag for an interrupt that is not masked is set.

[Workaround 1]

Be sure to clear the non-masked interrupt request flag before shifting to the STOP/IDLE mode. If the device is inadvertently shifted before clearing the flag, execute "Run" → "Stop" or click the  button on the debugger. The program is forcibly terminated. Then, execute "Run" → "CPU Reset" or click the  button.

[Workaround 2]

Do not allow the device to shift to the STOP/IDLE mode while the interrupt request flag for an interrupt that is not masked is set.

This bug has been corrected in control code G.

No.14 Modification of emulation target CPU

[Description]

The emulation target CPUs have been changed from the μPD70F3079Y and μPD70307xY (non-A versions) to the μPD70F3079AY and μPD70307xAY (A versions).

* Care must be taken because the initial value of the oscillation stabilization time selection register (OSTS) differs between the μPD70F3079Y, μPD70307xY (non-A products) and the μPD70F3079AY, μPD70307xAY (A products).

* The Hi-Z output from the CLKOUT pin cannot be emulated.

[Workaround]

There is no workaround.

This change has been implemented in control code F.

No.15 Hi-Z output from the CLKOUT pin cannot be emulated

[Description]

The Hi-Z output from the CLKOUT pin cannot be emulated. Even if the power save control register (PSC) is set to “Hi-Z output (DCLK1 = 0, DCLK0 = 1)” in the emulator, the same operation as “output enable (DCLK1 = 0, DCLK0 = 0)” is performed.

[Workaround]

There is no workaround.

This will be designated as a permanent restriction.

No.16 Bug in external bus interface

[Description]

The data cannot be read correctly when using the external bus interface.

[Workaround]

There is no workaround.

This bug has been corrected in control code H.

No.17 Bug in accessing FCAN area

[Description]

When an instruction to access the FCAN address area (xxnFF800H to xxnFFFFFH (n = 3, 7, or B)) is allocated to the emulation memory or target memory mapped to the external area and the instruction is executed, the FCAN register may not be able to be read (but it can be written).

[Workaround]

Allocate the instructions to access the FCAN address area to the internal ROM area.

This bug only applies to control code H products.

This bug has been corrected in control code J.

4. Cautions

When using the FCAN function, implement the following procedure on startup of the debugger.

a) Before startup of the debugger, supply power to pin V_{DD0} (GC package: pin 8, GF package: pin 11) on the target board.

b) Set the memory mapping on the debugger as shown below.

Attribute: Target memory

Mapping address: nFF800H to nFFFFFH (n = 3, 7, B)

c) Do not mask WAIT and HLDRQ when accessing the FCAN memory.