CUSTOMER NOTIFICATION

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CP(K), O

IE-703037-MC-EM1
(Control Code: A, B, C, D)

Restrictions

Be sure to read this document before using the product.

1. PRODUCT VERSION

Part number: IE-703037-MC-EM1

Control Code	Version of Board	Peripheral Chip	Remark
A	V1.32	μPD70F3033 ES1.1	
B	V1.33	μPD70F3033 ES1.1a	
C	V1.34	μPD70F3035 ES2.0	
D	V1.35	μPD70F3035 ES2.0	

Note The control code is the second digit from the left of the 10-digit control code (serial number) that starts from E.

If you have any questions concerning the product, consult the Development Tool Support Center.

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2. LIST OF RESTRICTIONS

No.	Restrictions	Applicable Control Code			
		A	B	C	D
1	Restriction related to CLKOUT	×	×	×	×
2	Restriction when INTWDT interrupt occurs	×	×	√	√
3	Restriction on IIC bus function	×	×	√	√
4	Interrupt processing is not performed if P113 is set in the output port mode.	×	×	√	√
5	P31 does not operate as an output port if P33 is used as SO4.	×	×	√	√
6	If the timing of setting the STOP mode and the timing of releasing the STOP mode conflict, the ICE becomes dead-locked.	×	×	√	√
7	If the compare register is written when TM2 to TM7 match the compare register, the match signal is not generated.	×	×	√	√
8	SB2 cannot be emulated.	×	√	√	√
9	Restriction on IEBus	×	×	√	√
10	Restriction on INTC (interrupt controller)	×	×	√	√
11	Restriction on I/O register illegal access break	–	×	×	×
12	Restriction on the initial values of PM6 and PM9	×	×	×	×
13	Restriction on P11 when set as output port	×	×	×	×
14	Restriction on interrupts in STOP/IDLE mode	×	×	×	×
15	Bug in initial value of pull-up resistor option register 10 (PU10)	×	×	×	√

√: Bug has been corrected.
×: Bug occurs.
–: Bug does not occur.

3. DETAILS OF RESTRICTIONS

(1) Restriction related to CLKOUT

[Description]

Output of CLKOUT is not disabled even if the reset signal is input.

[Workaround]

There is no workaround. Please regard this as permanent restriction.

(2) Restriction when INTWDT interrupt occurs

[Description]

If the INTWDT interrupt (non-maskable) occurs, execution branches to 0x30h (handler address not used by the device) instead of the correct interrupt handler address (0x20h).

[Workaround]

Place the same processing as that at 0020h at handler address 0030h.

(3) Restriction on IIC bus function

[Description]

The IIC bus function is not supported at present.

[Workaround]

There is no workaround.

(4) Interrupt processing is not performed if P113 is set in the output port mode.

[Description]

Interrupt processing is not performed if P113 is set as an output port.

[Workaround]

Use P113 as an input port.

(5) P31 does not operate as an output port if P33 is used as SO4.

[Description]

P31 does not operate as an output port if P33 is used as SO4.

[Workaround]

Use P31 as an input port when P33 is used as SO4.

(6) If the timing of setting the STOP mode and the timing of releasing the STOP mode conflict, the ICE becomes dead-locked.

[Description]

If the timing of setting the STOP mode and the timing of releasing the STOP mode conflict, the ICE is dead-locked. For details, refer to “V850/SB1 and SB2 Bug Information (SBG-T-1508)”.

[Workaround]

Use the IDLE mode or sub-IDLE mode instead of the STOP mode.

(7) If the compare register is written when TM2 to TM7 match the compare register, the match signal is not generated.

[Description and workaround]

For details, refer to “V850/SB1 and SB2 Bug Information (SBG-T-1508)”.

(8) SB2 cannot be emulated.

[Description]

SB2 cannot be emulated.

[Workaround]

There is no workaround.

(9) Restriction on IEBus

[Description & Workaround]

For details, refer to “Simplified IEBus Macro (SBG-T-1556)” and “Trouble of IEBus Macro (SBG-T-0843)”.

(10) Restriction on INTC (interrupt controller)

The same restriction applies to the target device.

[Description]

The bit manipulation instructions (set1, clr1, not1, tst1) perform a read-modify-write (RMW) operation that reads out the value of a register that is to be changed to an internal buffer, changes the value, and writes the new value to the register.

If a cycle in which the hardware of a register on which RMW operation is performed is set/reset[*1] and a DMA cycle conflict, setting/resetting the hardware of the register is canceled.

Example: If the DMA cycle started by a DMA start request (such as INTCSIn) coincides with the DMA transfer count end interrupt (INTDMAn) in a bit manipulation instruction cycle to an interrupt control register (DMAICn)

*1: Interrupt control register (xxIC), in-service priority register (ISPR)

[Workaround]

The interrupt control register (xxIC) and in-service priority register (ISPR) are registers that are set and reset by hardware. Do not use the bit manipulation instructions to manipulate these registers.

[Restriction]

Do not specify the xxIC register or ISPR register as the DIOAn register (DMA peripheral address register).
(Do not access the xxIC and ISPR register by using DMA.)

(11) Restriction on I/O register illegal access break

[Description]

There are some addresses that are reserved areas but for which an I/O register illegal access break cannot be detected.

These addresses are as follows:

Access Address	Emulation of SB1 (Except -Y Model)	Emulation of SB1 (-Y Model)	Emulation of SB2 (Except -Y Model)	Emulation of SB2 (-Y Model)
0xFFF138	×	√	×	√
0xFFF340	×	√	×	√
0xFFF342	×	√	×	√
0xFFF344	×	√	×	√
0xFFF346	×	√	×	√
0xFFF348	×	√	×	√
0xFFF34A	×	√	×	√
0xFFF34C	×	√	×	√
0xFFF350	×	√	×	√
0xFFF352	×	√	×	√
0xFFF354	×	√	×	√
0xFFF356	×	√	×	√
0xFFF358	×	√	×	√
0xFFF35A	×	√	×	√
0xFFF35C	×	√	×	√
0xFFF142	×	×	√	√
0xFFF144	×	×	√	√
0xFFF3E0	×	×	√	√
0xFFF3E2	×	×	√	√
0xFFF3E4	×	×	√	√
0xFFF3E6	×	×	√	√
0xFFF3E8	×	×	√	√
0xFFF3EA	×	×	√	√
0xFFF3EC	×	×	√	√
0xFFF3EE	×	×	√	√
0xFFF3F0	×	×	√	√
0xFFF3F2	×	×	√	√
0xFFF3F4	×	×	√	√
0xFFF3F6	×	×	√	√
0xFFF3F8	×	×	√	√

√: I/O register illegal break is detected.

×: I/O register illegal break is not detected.

[Workaround]

Take sufficient care when accessing an I/O register.

Please regard this as permanent restriction.

(12) Restriction on the initial values of PM6 and PM9

[Description]

The read values of PM6 and PM9 at reset are different from those of the real chip.

I/O Register Name	Address	Emulator Read Value	Real Chip Read Value
PM6	0xFFF02C	FF	3F
PM9	0xFFF032	FF	7F

[Workaround]

There is no workaround. Please regard this as permanent restriction.

(13) Restriction on P11 when set as output port

[Description]

If P11 is read when it is set as output port, the pin status is read instead of the port register value.

[Workaround]

There are no workaround. Please regard this as permanent restriction.

(14) Restriction on interrupts in STOP/IDLE mode

[Description]

The emulator is dead-locked under the following conditions.

If the device is shifted to the STOP/IDLE mode while the interrupt request flag is set by an interrupt that is not masked.

[Workaround]

Be sure to clear the non-masked interrupt request flag before shifting to the STOP/IDLE mode. If the device is inadvertently shifted before clearing the flag, execute “Run” → “Stop” or click the  button on the debugger. The program is forcibly terminated. Then, execute “Run” → “CPU Reset” or click the  button.

(15) Bug in initial value of pull-up resistor option register 10 (PU10)

[Description]

On-chip pull-up resistors are connected to ports 100 to 107 following debugger startup or after a reset (including the time from immediately after emulator power-on to debugger startup), even though the value of pull-up resistor option register 10 (PU10) is displayed as 00h (on-chip pull-up resistors not connected) on the debugger at that time.

[Workaround]

Write 00h to pull-up resistor option register 10 (PU10) during initialization immediately after a reset or in the I/O register window.

This workaround has been implemented in products with control code D and later.