CUSTOMER NOTIFICATION

SUD-T-4147-5-E

March 27, 2001

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IE-703017-MC-EM1
(Control Code: A, B, C, D, E, F)

Restrictions

Be sure to read this document before using the product.

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1. PRODUCT VERSION

Part number: IE-703017-MC-EM1

Control Code	Version of Board	Peripheral Chip	Remark
A	1.10	μPD70F3017Y ES1.1	IC32: V1.0 IC12: 105801210
B	2.21	μPD70F3017Y ES1.2	IC32: V1.0 IC12: 105801220
C	2.22	μPD70F3017Y ES1.2	IC32: V1.0 IC12: 105801230
D	2.23	μPD70F3017AY ES1.1	IC32: V2.0 IC12: 105801230
E	2.24	μPD70F3017AY ES1.1 or rank P or M	IC32: V2.0 IC12: 105801230
F	2.25	μPD70F3017AY ES1.1 or rank P or M	IC32: V2.0 IC12: 105801240

Note The control code is the second digit from the left of the 10-digit control code (serial number) that starts from E.

If you have any questions concerning the product, consult the Development Tool Support Center.

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2. LIST OF RESTRICTIONS

No.	Restrictions	Applicable Control Code					
		A	B	C	D	E	F
1	Incorrect operation when supply voltage (Vdd, BVdd) is less than 3 V.	×	×	×	×	×	×
2	I2C bus function cannot be used.	×	×	×	√	√	√
3	Values of fixed bits P11, PM11, P12, PM12, PMC12 becomes undefined.	×	√	√	√	√	√
4	Analog noise eliminator not present on external interrupt pin. (Same as μPD70F3017 ver1.1)	×	√	√	√	√	√
5	Incorrect overrun error occurs in UART (Same as μPD70F3017 ver1.1, ver1.2)	×	×	×	√	√	√
6	Jump to incorrect handler address when INTWDT interrupt occurs.	×	×	×	√	√	√
7	If the timing of setting the STOP mode and the timing of releasing the STOP mode conflict, the ICE is dead-locked.	×	×	×	√	√	√
8	Restriction related to CLKOUT	×	×	×	×	×	×
9	If a compare register is written when TM2 to TM7 match the compare register, the match signal is not generated.	×	×	×	√	√	√
10	Restriction on INTC (interrupt controller)	×	×	×	√	√	√
11	Restriction on the initial values of PM6 and PM9	×	×	×	×	×	×
12	Restriction related to P11 and P12	×	×	×	√	√	√
13	Restriction on I/O register illegal access break	×	×	×	×	×	×
14	Restriction on maximum operation frequency	×	×	×	×	√	√
15	Restriction on P11 when set as output port	×	×	×	×	×	×
16	Restriction on interrupts in STOP/IDLE mode	×	×	×	×	×	×
17	Bug in initial value of pull-up resistor option register 10 (PU10)	×	×	×	×	×	√

√: Restriction does not apply
×: Restriction applies

3. DETAILS OF RESTRICTIONS

(1) Incorrect operation when supply voltage (Vdd, BVdd) is less than 3 V.

[Description]

When the supply voltage (Vdd, BVdd) is less than 3V, access to the I/O register and the interrupt function fail to operate correctly.

[Workaround]

There is no workaround. Make sure the supply voltage is 3 V or more.

(2) I2C bus function cannot be used.

[Description]

The I2C bus function is not currently supported.

[Workaround]

This workaround has been implemented in products with control code D and later.

(3) Values of fixed bits P11, PM11, P12, PM12, PMC12 becomes undefined.

[Description]

The value of the following fixed bits of the I/O registers becomes undefined.

I/O Register Name	Undefined Bit (Undefined Value)	Read Value of Applicable Device	Read Value Of ICE	Remark
P11	Bits 7 to 5	000xxxxx	ZZZxxxxx	Z is undefined
PM11	Bits 7 to 4	0001xxxx	ZZZZxxxx	Z is undefined
P12	Bits 7 to 1	0000000x	ZZZZZZZx	Z is undefined
PM12	Bits 7 to 1	0000000x	ZZZZZZZx	Z is undefined
PMC12	Bits 7 to 1	0000000x	ZZZZZZZx	Z is undefined

[Workaround]

There is no workaround. Mask the undefined bits in software.

This workaround has been implemented in products with control code B and later.

(4) Analog noise eliminator not present on external interrupt pin.

(Same as μPD70F3017 ver. 1.1)

[Description]

The analog noise eliminator is not present on NMI, INTP0 to INTP3. Consequently an interrupt can occur with several ns of noise.

[Workaround]

There is no workaround.

This workaround has been implemented in products with control code B and later.

(5) Incorrect overrun error occurs in UART (Same as μPD70F3017 ver.1.1, ver.1.2)

[Description]

When the receive buffer register (RXBn) is read, an overrun error occurs even though the buffer is not in an overrun error state.

[Workaround]

Please refer to the bug notification for the device μPD703017.

This workaround has been implemented in products with control code D and later.

(6) Jump to incorrect handler address when INTWDT interrupt occurs.

[Description]

When the INTWDT (non-maskable) interrupt occurs, process jumps to an incorrect handler address 0x30h (in an area not used in this device) rather than the correct handler address 0x20h.

[Workaround]

Place the handler program found at 0020h at the address 0030h.

This workaround has been implemented in products with control code D and later.

(7) If the timing of setting the STOP mode and the timing of releasing the STOP mode conflict, the ICE is dead-locked.

[Description]

If the timing to set the STOP mode and the timing to release the STOP mode conflict, the ICE is dead-locked. For details, refer to “V850/SB1 and SB2 Bug Information (SBG-T-1508)”.

[Workaround]

Use the IDLE mode or sub-IDLE mode instead of the STOP mode.

This workaround has been implemented in products with control code D and later.

(8) Restriction related to CLKOUT

[Description]

Output of CLKOUT is not disabled even if the reset signal is input.

[Workaround]

There is no workaround. Please regard this as permanent restriction.

(9) If a compare register is written when TM2 to TM7 match the compare register, the match signal is not generated.

[Description]

For details, refer to “V850/SB1 and SB2 Bug Information (SBG-T-1508)”.

[Workaround]

For details, refer to “V850/SB1 and SB2 Bug Information (SBG-T-1508)”.

(10) Restriction on INTC (interrupt controller)

The same restriction applies to the target device.

[Description]

The bit manipulation instructions (set1, clr1, not1, tst1) perform a read-modify-write (RMW) operation that reads out the value of a register that is to be changed to an internal buffer, changes the value, and writes the new value to the register.

If a cycle in which the hardware of the register on which RMW operation is performed is set/reset[*1] and a DMA cycle conflict, setting/resetting the hardware of the register is canceled.

Example: If the DMA cycle started by a DMA start request (such as INTCSIn) coincides with the DMA transfer count end interrupt in a bit manipulation instruction cycle to an interrupt control register (DMAICn)

*1: Interrupt control register (xxIC), in-service priority register (ISPR)

[Workaround]

The interrupt control register (xxIC) and in-service priority register (ISPR) are set and reset by hardware. Do not use bit manipulation instructions to manipulate these registers.

[Restriction]

Do not specify the xxIC register or ISPR register as the DIOAn register (DMA peripheral address register).

(Do not access the xxIC and ISPR register by using DMA.)

This workaround has been implemented in products with control code D and later.

(11) Restriction on the initial values of PM6 and PM9

[Description]

The read values of PM6 and PM9 at reset are different from those of the real chip.

I/O Register Name	Address	Emulator Read Value	Real Chip Read Value
PM6	0xFFF02C	FF	3F
PM9	0xFFF032	FF	7F

[Workaround]

There is no workaround. Please regard this as permanent restriction.

(12) Restriction related to P11 and P12

[Description]

a) If the following SFR registers related to P11 and P12 are accessed, illegal data may be written or read.

P11, PM11, PU11, P12, PM12, PMC12

b) With PMC12, the WAIT pin that is multiplexed with P120 may not be able to be selected.

[Workaround]

There is no workaround.

This workaround has been implemented in products with control code D and later.

(13) Restriction on I/O register illegal access break

[Description]

There are same addresses as reserved areas but for which an I/O register illegal access break cannot be deleted.

Access Address	During Emulation of Y Model	During Emulation of Model Other Than Y
0xFFF340	o	X
0xFFF342	o	X
0xFFF344	o	X
0xFFF346	o	X
0xFFF348	o	X
0xFFF34A	o	X

[Workaround]

There is no workaround. Please regard this as permanent restriction.

(14) Restriction on maximum operation frequency

[Description]

The maximum operation frequency is as follows.

Products with control codes A to D: 17 MHz

Products with control code E or later: 20 MHz

[Workaround]

There is no workaround.

This workaround has been implemented in products with control code E and later.

(15) Restriction on P11 when set as output port

[Description]

If P11 is read when it is set as output port, the pin status is read instead of the port register value.

[Workaround]

There is no workaround. Please regard this as permanent restriction.

(16) Restriction on interrupts in STOP/IDLE mode

[Description]

The emulator is dead-locked under the following conditions.

If the device is shifted to the STOP/IDLE mode while the interrupt request flag is set by an interrupt that is not masked.

[Workaround]

Be sure to clear the non-masked interrupt request flag before shifting to the STOP/IDLE mode. If the device is inadvertently shifted before clearing the flag, execute “Run” → “Stop” or click the  button on the debugger. The program is forcibly terminated. Then, execute “Run” → “CPU Reset” or click the  button.

(17) Bug in initial value of pull-up resistor option register 10 (PU10)

[Description]

On-chip pull-up resistors are connected to ports 100 to 107 following debugger startup or after a reset (including the time from immediately after emulator power-on to debugger startup), even though the value of pull-up resistor option register 10 (PU10) is displayed as 00h (on-chip pull-up resistors not connected) on the debugger at that time.

[Workaround]

Write 00h to pull-up resistor option register 10 (PU10) during initialization immediately after a reset or in the I/O register window.

This workaround has been implemented in products with control code F and later.