Microcomputer Technical Information

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1. Affected product

   IE-703017-MC-EM1 Control code[Note]: A, B, C, D, E, F, G

2. Details of restriction

   This notification concerns the following restriction. See the attachment for details.

   - No.18 Bug that relay continues to switch the power on/off

3. Workaround

   See the attachment for details of the workaround for this restriction.

4. Modification schedule

   Modified products are scheduled for release as follows.

Newly shipped products:	From the shipment of March 2003 (control code: H)
Upgrade for already shipped products:	Available from mid-March, 2003

   * Note that this schedule is subject to change without notice. For the detailed release schedule of modified products, contact an NEC Electronics sales representative.

5. Restriction history

   Notes on using the IE-703017-MC-EM1, including the restriction history and detailed information, will be described on the following pages.

Note The "control code" is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If the product has been upgraded, the version can be checked by the label attached to the product.

Notes on Using IE-703017-MC-EM1

1. Product Version

Part number: IE-703017-MC-EM1

Control Code	Version of Board	Peripheral Chip	Remark
A	1.10	μPD70F3017Y ES1.1	IC32: V1.0 IC12: 105801210
B	1.21	μPD70F3017Y ES1.2	IC32: V1.0 IC12: 105801220
C	1.22	μPD70F3017Y ES1.2	IC32: V1.0 IC12: 105801230
D	1.23	μPD70F3017AY ES1.1	IC32: V2.0 IC12: 105801230
E	1.24	μPD70F3017AY ES1.1 or rank P or M	IC32: V2.0 IC12: 105801230
F	1.25	μPD70F3017AY ES1.1 or rank P or M	IC32: V2.0 IC12: 105801240
G	2.36	μPD70F3017A rank M	IC32: V2.0 IC12: 105801240

Note The “control code” is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If the product has been upgraded, the version can be checked by the label attached to the product.

Employ an IE-703002-MC with a control code of H or later when using this option board.

2. Product History

No.	Restrictions	Control Code					
		A	B	C	D	E	F, G
1	Incorrect operation when supply voltage (Vdd, BVdd) is less than 3 V.	Permanent restriction					
2	I^2C bus function cannot be used.	×	×	×	√	√	√
3	Values of fixed bits of P11, PM11, P12, PM12, and PMC12 are undefined.	×	√	√	√	√	√
4	Analog noise eliminator not present on external interrupt pin. (Same bug as μPD70F3017 Ver.1.1)	×	√	√	√	√	√
5	Incorrect overrun error occurs in UART (Same bug as μPD70F3017 Ver.1.1, 1.2)	×	×	×	√	√	√
6	Jump to incorrect handler address when INTWDT interrupt occurs.	×	×	×	√	√	√
7	The emulator deadlocks if the timing of setting the STOP mode and the timing of releasing the STOP mode conflict	×	×	×	√	√	√
8	Restriction related to CLKOUT	Permanent restriction					
9	The match signal is not generated if a compare register is written when TM2 to TM7 match the compare register.	×	×	×	√	√	√
10	Restriction on INTC (interrupt controller)	×	×	×	√	√	√
11	Restriction on initial values of PM6 and PM9	Permanent restriction					
12	Restriction related to P11 and P12	×	×	×	√	√	√
13	Restriction on I/O register illegal access break	Permanent restriction					
14	Restriction on maximum operating frequency	×	×	×	×	√	√
15	Restriction on P11 when set as output port	Permanent restriction					
16	Restriction on interrupts in STOP/IDLE mode	Permanent restriction					
17	Bug in initial value of pull-up resistor option register 10 (PU10)	×	×	×	×	×	√
18	Bug that relay continues to switch the power on/off	×	×	×	×	×	×

√: Restriction does not apply

×: Restriction applies

3. Details of Usage Restrictions

No.1 Incorrect operation when supply voltage (Vdd, BVdd) is less than 3 V.

[Description]

When the supply voltage (Vdd, BVdd) is less than 3V, access to the I/O register and the interrupt function fail to operate correctly.

[Workaround]

There is no workaround. Make sure the supply voltage is 3 V or more.

No.2 I^2C bus function cannot be used.

[Description]

The I^2C bus function is not currently supported.

[Workaround]

This restriction has been corrected in products with control code D and later.

No.3 Values of fixed bits of P11, PM11, P12, PM12, and PMC12 are undefined.

[Description]

The value of the following fixed bits of the I/O registers becomes undefined.

I/O Register Name	Undefined Bit (Undefined Value)	Read Value of Target Device	Read Value of Emulator	Remark
P11	Bits 7 to 5	000xxxxx	ZZZxxxxx	Z is undefined
PM11	Bits 7 to 4	0001xxxx	ZZZZxxxx	Z is undefined
P12	Bits 7 to 1	0000000x	ZZZZZZZx	Z is undefined
PM12	Bits 7 to 1	0000000x	ZZZZZZZx	Z is undefined
PMC12	Bits 7 to 1	0000000x	ZZZZZZZx	Z is undefined

[Workaround]

There is no workaround. Mask the undefined bits in software.

This restriction has been corrected in products with control code B and later.

No.4 Analog noise eliminator not present on external interrupt pin.

(Same bug as μPD70F3017 Ver.1.1)

[Description]

The analog noise eliminator is not present on NMI, INTP0 to INTP3. Consequently an interrupt is acknowledged with several ns of noise.

[Workaround]

There is no workaround.

This restriction has been corrected in products with control code B and later.

No.5 Incorrect overrun error occurs in UART (Same bug as μPD70F3017 Ver.1.1, 1.2)

[Description]

When the receive buffer register (RXBn) is read, an overrun error occurs even though the buffer is not in an overrun error state.

[Workaround]

Please refer to the bug notification for the μPD703017.

This restriction has been corrected in products with control code D and later.

No.6 Jump to incorrect handler address when INTWDT interrupt occurs.

[Description]

When the INTWDT (non-maskable) interrupt occurs, process jumps to an incorrect handler address 0x30h (in an area not used in this device) rather than the correct handler address 0x20h.

[Workaround]

Describe the same handler program as the handler program described at 0020h at address 0030h.

This restriction has been corrected in products with control code D and later.

No.7 The emulator deadlocks if the timing of setting the STOP mode and the timing of releasing the STOP mode conflict.

[Description]

The emulator deadlocks if the timing to set the STOP mode and the timing to release the STOP mode conflict. Refer to “V850/SB1 and SB2 Bug Information (SBG-T-1508-E)” for details.

[Workaround]

Use the IDLE mode or sub-IDLE mode instead of the STOP mode.

This restriction has been corrected in products with control code D and later.

No.8 Restriction related to CLKOUT

[Description]

Output of CLKOUT is not disabled even if the reset signal is input.

[Workaround]

There is no workaround. Please regard this as permanent restriction.

No.9 The match signal is not generated if a compare register is written when TM2 to TM7 match the compare register.

[Description]

Refer to “V850/SB1 and SB2 Bug Information (SBG-T-1508-E)” for details.

[Workaround]

Refer to “V850/SB1 and SB2 Bug Information (SBG-T-1508-E)” for details.

This restriction has been corrected in products with control code D and later.

No.10 Restriction on INTC (interrupt controller)

The same restriction applies to the target device.

[Description]

The bit manipulation instructions (set1, clr1, not1, tst1) perform a read-modify-write (RMW) operation that reads out the value of a register that is to be changed to an internal buffer, changes the value, and writes the new value to the register.

If a cycle in which the hardware of the register on which RMW operation is performed is set/reset[*1] and a DMA cycle conflict, setting/resetting the hardware of the register is canceled.

Example If the DMA cycle started by a DMA start request (such as INTCSIn) conflicts with the DMA transfer count end interrupt in a bit manipulation instruction cycle to an interrupt control register (DMAICn)

*1: Interrupt control register (xxIC), in-service priority register (ISPR)

[Workaround]

The interrupt control register (xxIC) and in-service priority register (ISPR) are set and reset by hardware. Do not use bit manipulation instructions to manipulate these registers.

[Restriction]

Do not specify the xxIC register or ISPR register as the DIOAn register (DMA peripheral address register). (Do not access the xxIC and ISPR register by using DMA.)

This restriction has been corrected in products with control code D and later.

No.11 Restriction on initial values of PM6 and PM9

[Description]

The read values of PM6 and PM9 at reset are different from those of the real chip.

I/O Register Name	Address	Emulator Read Value	Real Chip Read Value
PM6	0xFFF02C	FF	3F
PM9	0xFFF032	FF	7F

[Workaround]

There is no workaround. Please regard this as permanent restriction.

No.12 Restriction related to P11 and P12

[Description]

a) If the following registers related to P11 and P12 are accessed, illegal data may be written or read.
P11, PM11, PU11, P12, PM12, PMC12

b) With PMC12, the WAIT pin that is multiplexed with P120 may not be able to be selected.

[Workaround]

There is no workaround.

This restriction has been corrected in products with control code D and later.

No.13 Restriction on I/O register illegal access break

[Description]

There are same addresses as reserved areas but for which an I/O register illegal access break cannot be detected.

Access Address	During Emulation of Y Version	During Emulation of Non-Y Versions
0xFFF340	Detected	Cannot be detected
0xFFF342	Detected	Cannot be detected
0xFFF344	Detected	Cannot be detected
0xFFF346	Detected	Cannot be detected
0xFFF348	Detected	Cannot be detected
0xFFF34A	Detected	Cannot be detected

[Workaround]

There is no workaround. Please regard this as permanent restriction.

No.14 Restriction on maximum operating frequency

[Description]

The maximum operating frequency is as follows.

Products with control codes A to D: 17 MHz

Products with control code E or later: 20 MHz

[Workaround]

There is no workaround.

This restriction has been corrected in products with control code E and later.

No.15 Restriction on P11 when set as output port

[Description]

If P11 is read when it is set as output port, the pin status is read instead of the port register value.

[Workaround]

There is no workaround. Please regard this as permanent restriction.

No.16 Restriction on interrupts in STOP/IDLE mode

[Description]

The emulator deadlocks under the following conditions.

If the device is shifted to STOP/IDLE mode while the interrupt request flag for an interrupt that is not masked is set.

[Workaround 1]

Be sure to clear the non-masked interrupt request flag before shifting to STOP/IDLE mode. If the device is inadvertently shifted before clearing the flag, execute “Run” → “Stop” or click the  button on the debugger. The program is forcibly terminated. Then, execute “Run” → “CPU Reset” or click the  button.

[Workaround 2]

Do not shift to the STOP/IDLE mode while the interrupt request flag is set by an interrupt that is not masked.

No.17 Bug in initial value of pull-up resistor option register 10 (PU10)

[Description]

On-chip pull-up resistors are connected to ports 100 to 107 following debugger startup or after a reset (including the time from immediately after emulator power-on to debugger startup), even though the value of pull-up resistor option register 10 (PU10) is displayed as 00h (on-chip pull-up resistors not connected) on the debugger at that time.

[Workaround]

Write 00h to pull-up resistor option register 10 (PU10) during initialization immediately after a reset or in the I/O register window.

This restriction has been corrected in products with control code F and later.

No.18 Bug that relay continues to switch the power on/off

[Description]

When BVDD and VDD are shorted on the target board, if the power to the emulator is turned on while the target power is off, the relay in the IE-703017-MC-EM1 continues to switch the power on/off.

[Workaround]

Turn the target power on when the power to the emulator is on. At this time, turn the target power on as soon as the power to the emulator is turned on.

4. Cautions

None.