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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A012A/E	Rev.	1.00
Title	I^2C bus interface (RIIC) Precautions when using timeout detection function		Information Category	Technical Notification		
Applicable Product	RX610 group RX62N, RX621 group RX62T group RX630 group RX63N, RX631 group	Lot No. All lots	Reference Document	RX610 group RX62N, RX621 group RX62T group RX630 group RX63N, RX631 group User's Manual, Hardware section		

While timeout detection function of I^2C bus interface (RIIC) is set to CMR1.CKS [2:0] ≠ 000, timeout is detected even when communications are proceeding correctly. To avoid this, use registered disclosed in this document and follow the avoidance flow. In this avoidance flow, every time data is accessed, write 0000h to the timeout internal counter and clear counter. Thus, it is applicable only to data transfer using CPU or one using DTC. When you use DMAC for data transfer of RIIC, you need to set ICMR1.CKS [2:0] ＝ 000b or change it to transfer using CPU or one using DTC.

1. Condition

When using timeout detection function of I^2C bus interface (RIIC) under setting of CMR1.CKS [2:0] ≠ 000.

2. Phenomenon

Even when communications are proceeding correctly, timeout is detected from a set of ICFER.TMOE bit after a certain period of time for detection has elapsed.

3. Disclosed register

・ (1) ICMR2.TMWE bit (b3) of I^2C bus mode register (ICMR2) will be disclosed.

	b7	b6	b5	b4	b3	b2	b1	b0
	DLCS	SDDL [2:0]			TMWE	TMOH	TMOL	TMOS
Value after reset	0	0	0	0	0	1	1	0

Bit	Symbol	Bit name	Description	R/W
b3	TMWE	Timeout internal counter write enable bit	0: Writing to internal counter of timeout detection function is disabled 1: Writing to internal counter of timeout detection function is enabled When this bit is set to "1", the address of timeout internal counter (TMOCNT_L/U) is allocated to the address of SARL0/SARU0.	R/W

(2)Disclose the timeout internal counter register (TMOCNT).

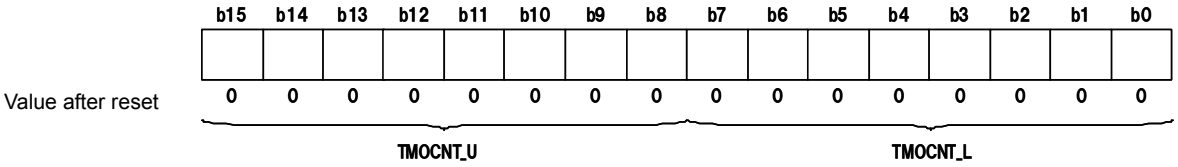
Timeout internal counter (TMOCNT)

Address RIIC0.TMOCNT_L 0008 830Ah*, RIIC1.TMOCNT_L 0008 832Ah*,

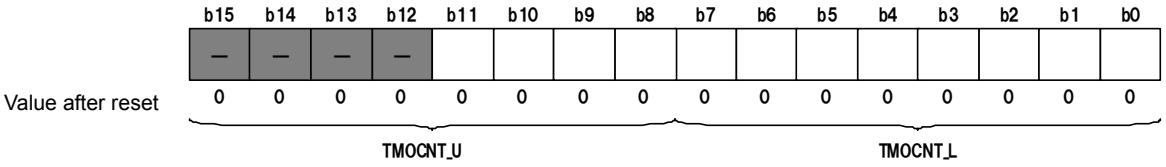
RIIC0.TMOCNT_U 0008 830Bh*, RIIC1.TMOCNT_U 0008 832Bh*

*Same addresses with ones of the slave address registers, SARL0, SARU0. Care should be taken.

・TMOS=0 (Long mode)



・TMOS=1 (Short mode)



Bit	Symbol	Bit name	Description	R/W
b15-8	TMOCNT_U	Timeout internal counter	Timeout internal counter high-order *1	W *2
b7-0	TMOCNT_L		Timeout internal counter low-order	

*1: With TMOS=1 (Short mode), b15-b12 are reserved bits. They are writable, however value written is disabled.

*2: Value in timeout internal counter cannot be read. When value is read, the read value is FFFFh.

Timeout internal counter (TMOCNT_L/TMOCNT_U) is initialized (0000h) after a reset, while ICCR1.IICRST=1 or ICFER.TMOE=1 and PCLK/1 is selected with ICMR1.CKS[2:0]=000b setting, and when counter clear conditions specified by TMOH/TMOL of ICMR2 (SCL rising edge/falling edge detection) are satisfied.

4. Avoidance Flow

To avoid this, add the procedures marked in red indicated below to the flowchart in the user's manual.

"xx" as in Figure xx.5 indicates the chapter of I^2C of the user's manual respectively. Please refer to the "Target products and Reference" for details.

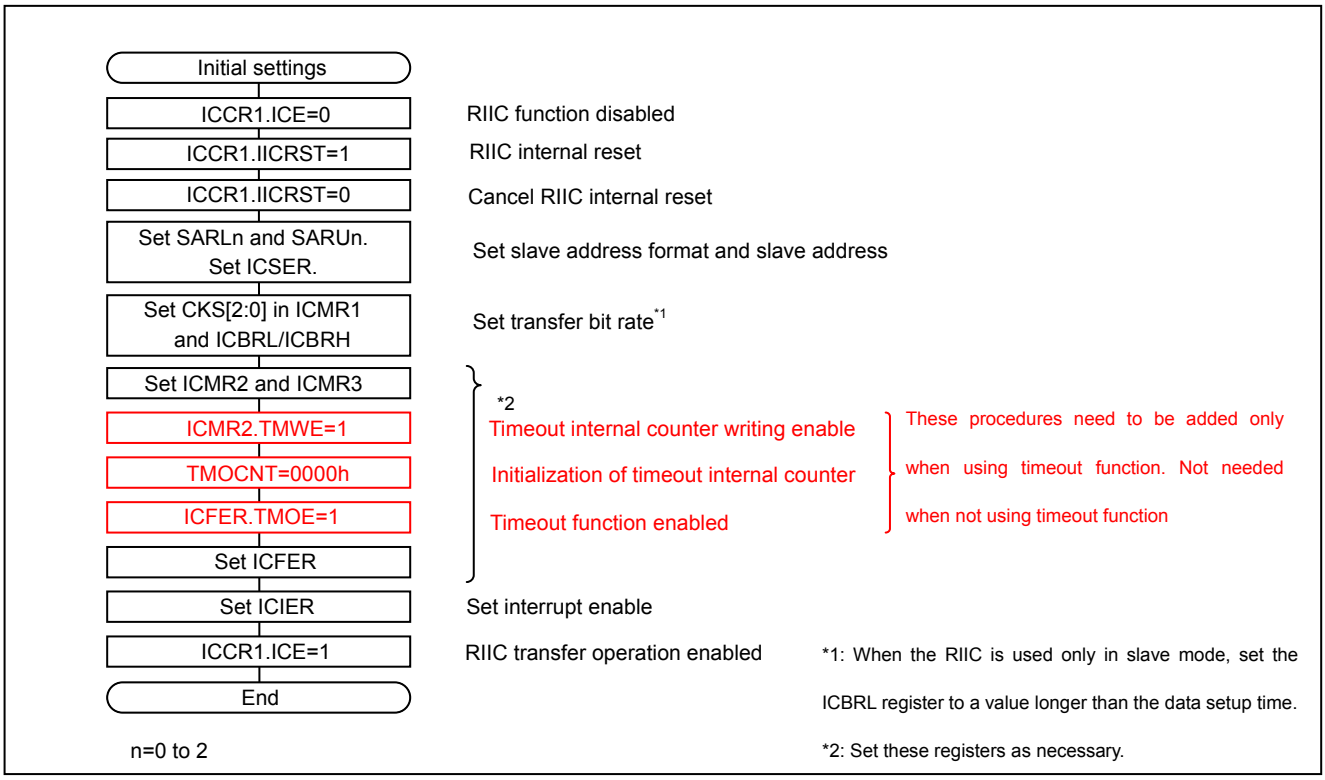


Figure xx.5 Example of RIIC Initialization Flow

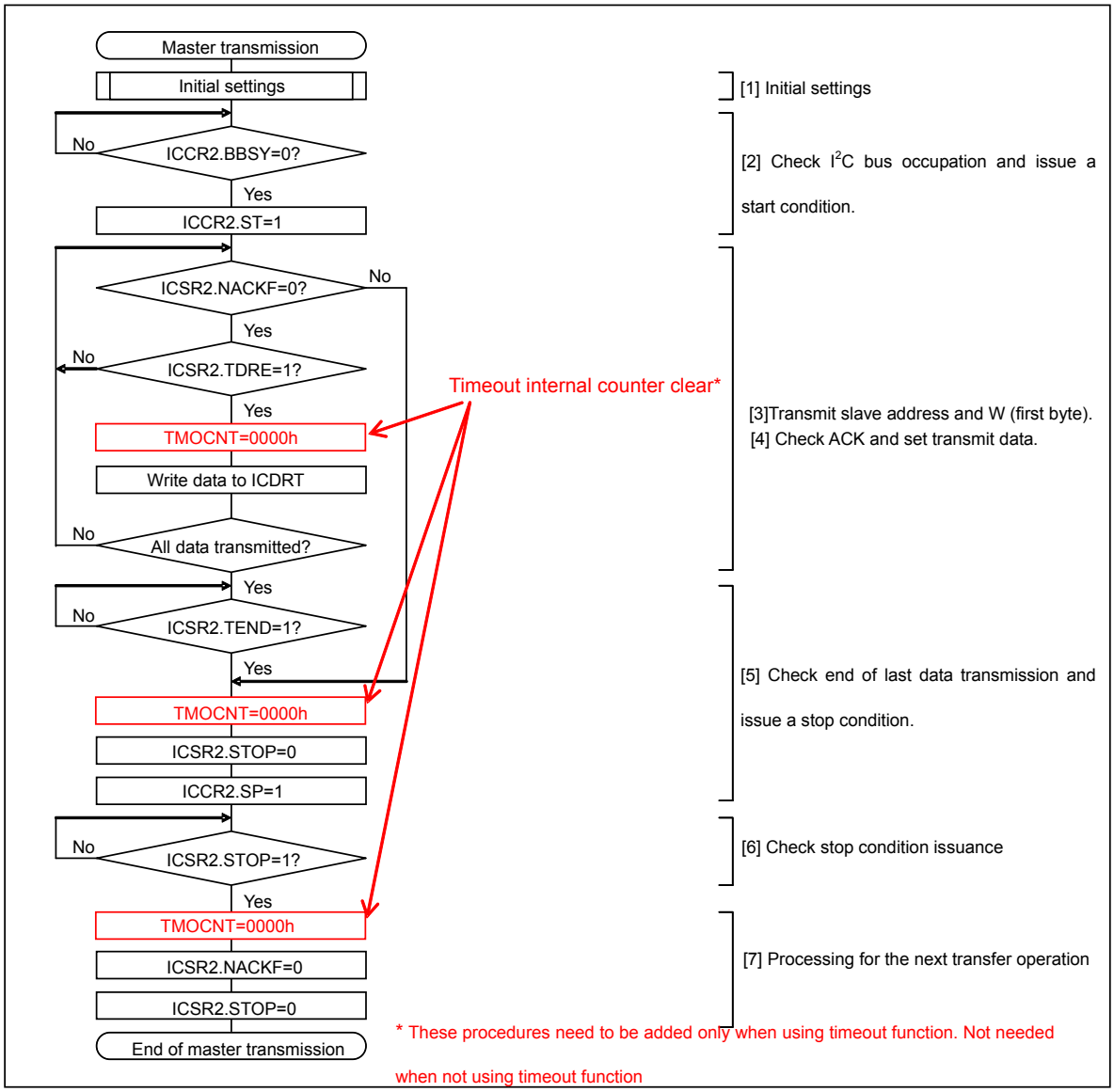


Figure xx.6 Example of Master Transmission Flowchart

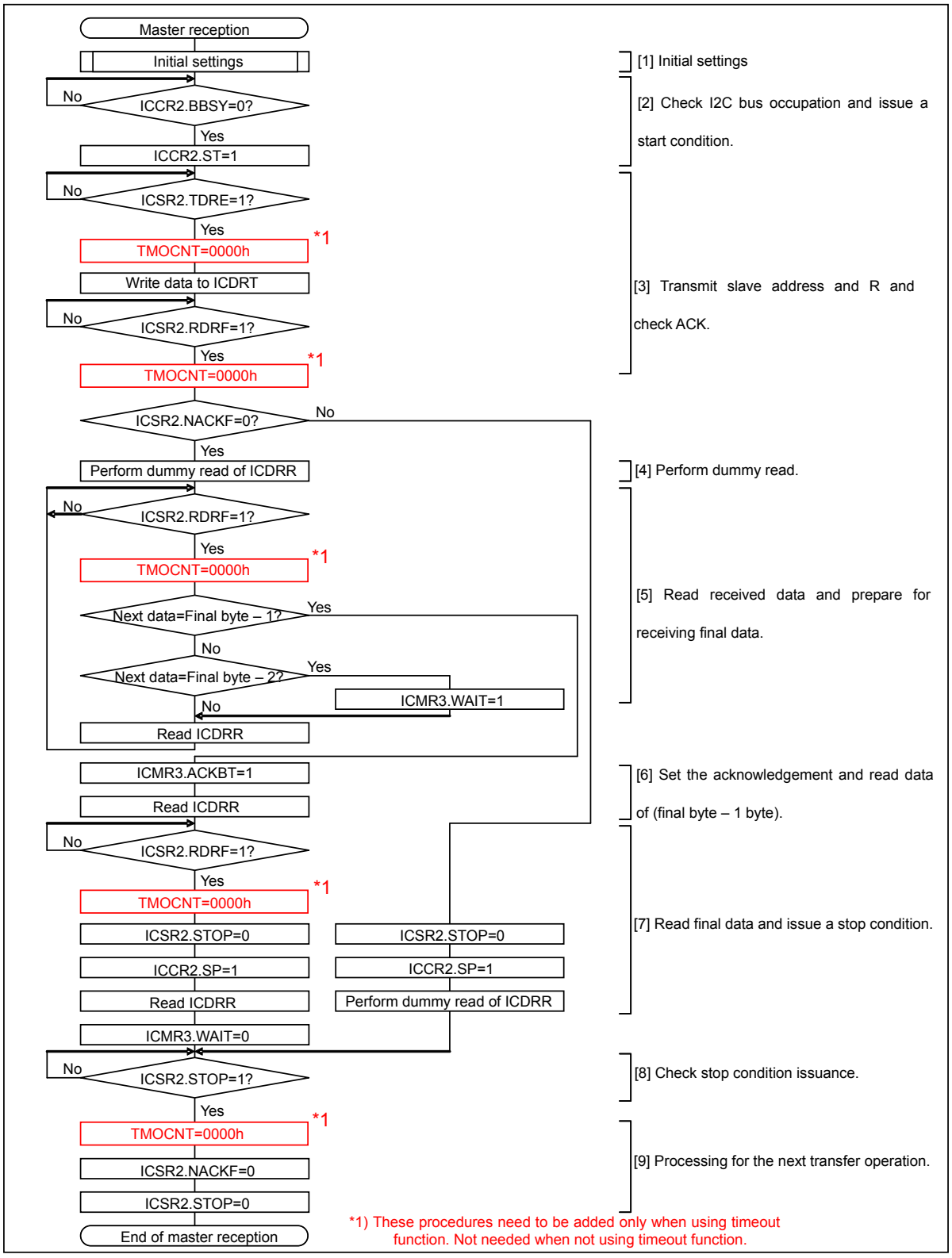


Figure xx.10 Example of Master Reception Flowchart (7-Bit Address Format)

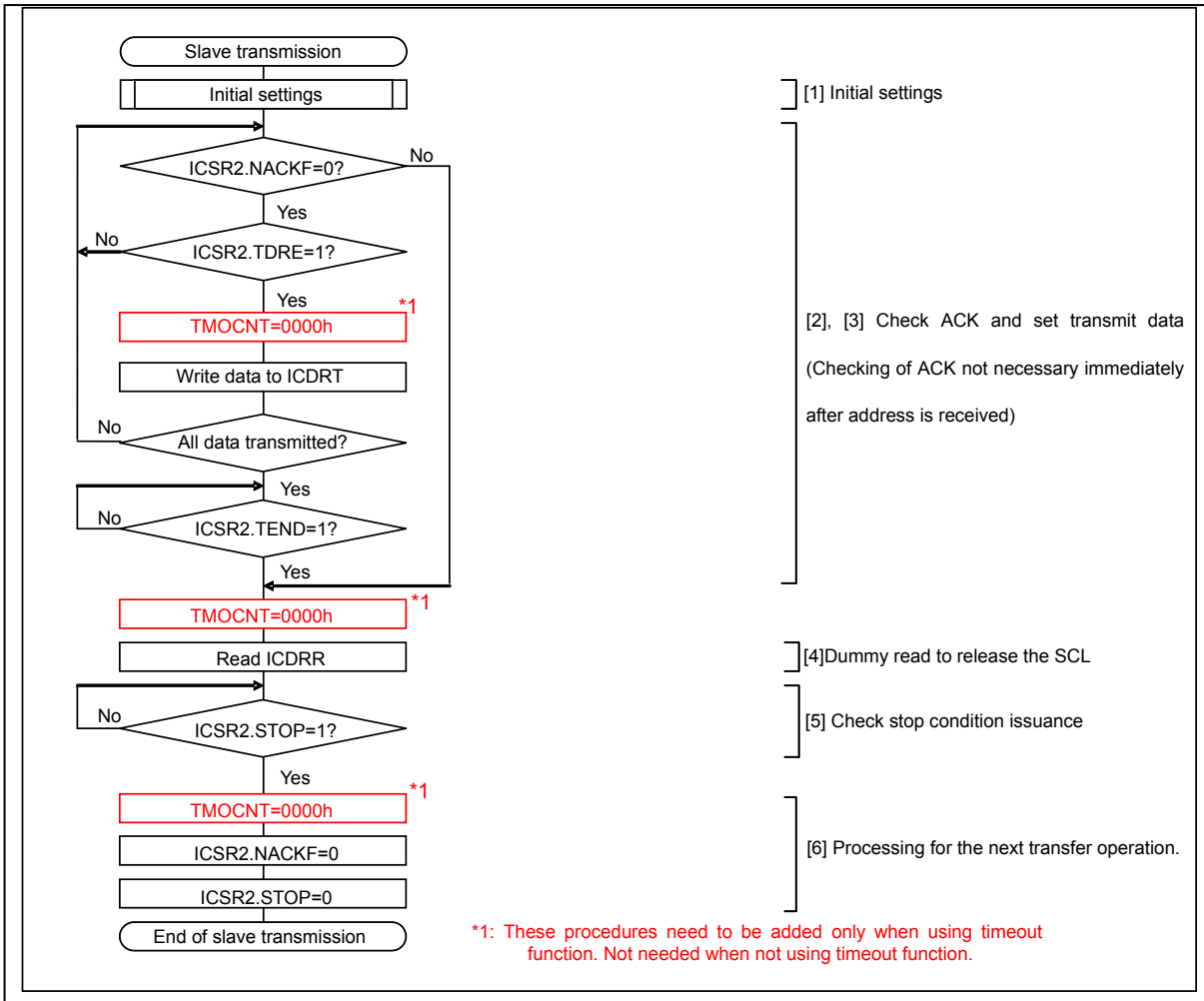


Figure xx.14 Example of Slave Transmission Flowchart

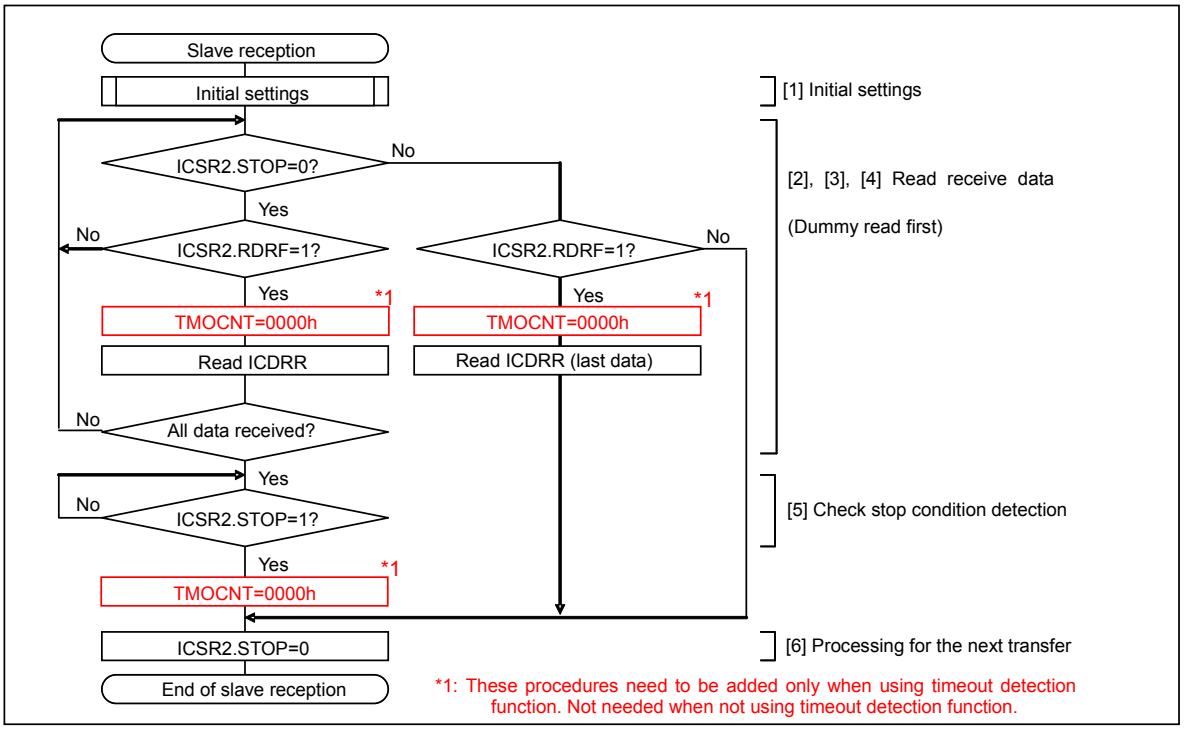


Figure xx.17 Example of Slave Reception Flowchart

5. Avoidance when using DTC

When writing transmit data to ICDRT or reading receive data from ICDRR by the DTC during master transmission/reception, use the following flow to avoid the phenomenon. Set the DTC to chain transfer, and clear internal counter every time transmit data or receive data is transferred.

Master reception flowchart is indicated below.

This flowchart shows only flow involved with DTC transfer. For the rest of the flow, refer to the flowcharts indicated on page 3 to 6.

(1) Initial settings flow: What is indicated on page 3 + DTC setting

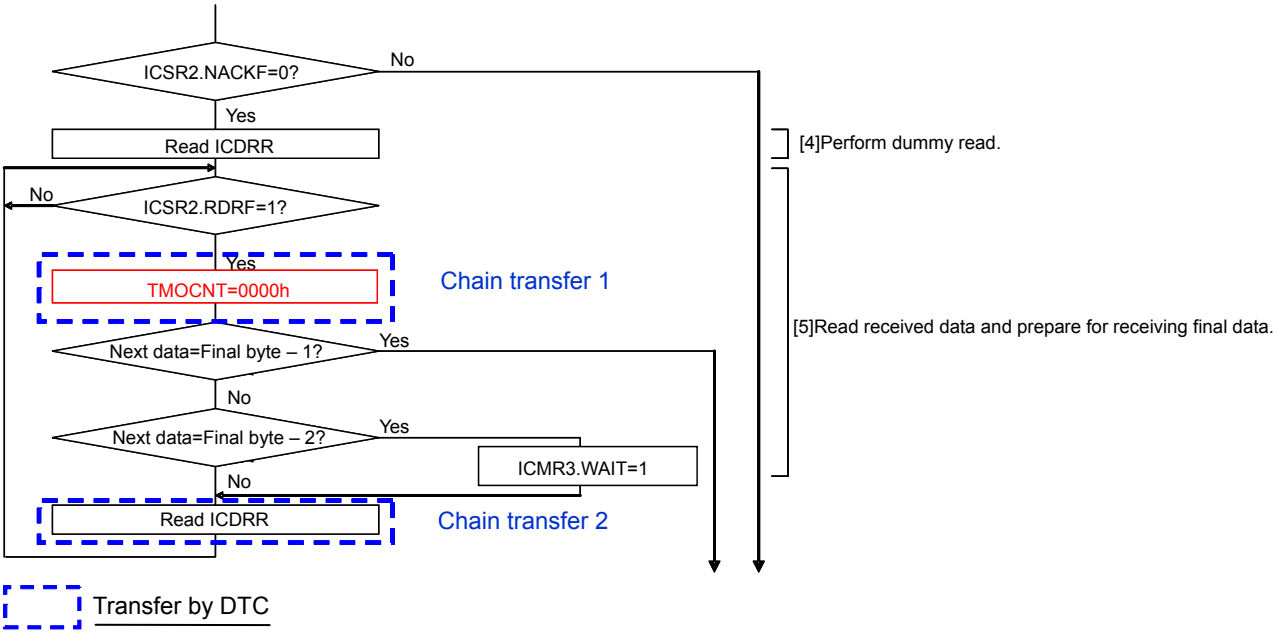
The DTC needs to be set to enable the following operation.

Set the DTC to chain transfer.

・First chain transfer (Chain transfer 1): Write 0000h to TMOCNT

・Subsequent chain transfer (Chain transfer 2): Transfer specified by user (Read ICDRR, etc)

(2) Example of flowchart during N-2 times transfer by DTC (excerpt comments from the flowchart on page 5)



■Target Products and Reference

Group	Title	Rev.	Document No.	Chapter of I^2C
RX610 group	RX610 group User's Manual, Hardware section	Rev.1.10	R01UH0032EJ0110	22
RX62N, RX621 group	RX62N group, RX621 group User's Manual, Hardware section	Rev.1.30	R01UH0033EJ0130	31
RX62T group	RX62T group User's Manual, Hardware section	Rev.1.10	R01UH0034EJ0110	23
RX630 group	RX630 group User's Manual, Hardware section	Rev.1.12	R01UH0040EJ0112	32
RX63N, RX631group	RX63N group, RX631 group User's Manual, Hardware section	Rev.0.9	R01UH0041EJ0090	35