To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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RenesasTechnology Corp.

Product Category	MPU&MCU	Document No.	TN-H8*-283A/EA	Rev.	1.0
Title	H8S/2215 Group, Smart card interface functional public presentation		Information Category	Specification Change	
Applicable Product	H8S/2215 Group	Lot No. All	Reference Document	H8S/2215 Series Hardware Manual REJ09B0140-0400O Rev.4.00	

Into H8S/2215 group, it has the independent serial communication interface (SCI) of 3 channels. Although the smart card (IC card) interface function based on ISO/IEC 7816-3 (Identification Card) was added to such SCI, it was considering as secret until now. Lately, connection of smart card interface extension functional public presentation of these SCI is carried out.

In order to use SCI as a smart card interface, the 0bit of SCI/SCMR is set as 1. (Refer to Table 1)

Table 1 Open bit (SCI/SCMR/SMIF)

Bit	Bit Name	Initial Value	R/W	Description
0	SMIF	0	R/W	Smart Card Interface Mode Select When this bit is set to 1, smart card interface mode is selected. 0: Normal asynchronous or clocked synchronous mode 1: Smart card interface mode

In addition, if a SMIF bit is set as 1, the function of each register of SMR, SCR, and SSR will change.
It following-paper-refers to for details.

The main features of this smart card interface

- An error signal can be automatically transmitted on detection of a parity error during reception
- Data can be automatically re-transmitted on detection of a error signal during transmission
- Both direct convention and inverse convention are supported

< Hardware manual change part >

- Section 9 I/O ports
- Section 13 Serial Communication Interface (SCI)

Hereafter, hardware manual change part details are described.

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>Section 9 I/O Ports</td><td>237

247</td><td>

Table 9.13 P33 Pin Function

SMIF in SCMR_1	0			1			
TE in SCR_1	0		1	0		1	
P33DDR	0	1	—	0	1	0	1
Pin function	P33 input	P33 output	TXD1 output	P33 input	Prohibition of a setup	TXD1 output	Prohibition of a setup

Table 9.16 P30 Pin Function

SMIF in SCMR_0	0			1			
TE in SCR_0	0		1	0		1	
P30DDR	0	1	—	0	1	0	1
Pin function	P30 input	P30 output	TXD0 output	P30 input	Prohibition of a setup	TXD0 output	Prohibition of a setup

Table 9.24 PA1 Pin Function

Operating mode	Modes 4 to 6							
AE3 to AE0	101x or 11xx	Other than 101x or 11xx						
SMIF in SCMR_2	—	0			1			
TE in SCR_2	—	0		1	0		1	
PA1DDR	—	0	1	—	0	1	0	1
Pin function	A17 output	PA1 input	PA1 output	TXD2 output	PA1 input	Prohibition of a setup	TXD2 output	Prohibition of a setup

Operating mode	Mode 7						
SMIF in SCMR_2	0			1			
TE in SCR_2	0		1	0		1	
PA1DDR	0	1	—	0	1	0	1
Pin function	PA1 input	PA1 output	TXD2 output	PA1 input	Prohibition of a setup	TXD2 output	Prohibition of a setup

</td></tr>
</table>

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>Section 13 Serial Communication Interface (SCI)</td><td>375</td><td>This LSI has three independent serial communication interface (SCI) channels. The SCI can handle both asynchronous and clocked synchronous serial communication. Asynchronous serial data communication can be carried out using standard asynchronous communication chips such as a Universal Asynchronous Receiver/Transmitter (UART) or an Asynchronous Communication Interface Adapter (ACIA). The SCI also supports the smart card (IC card) interface based on ISO/IEC 7816-3 (Identification Card) as an enhanced asynchronous communication function.</td></tr>
<tr><td>13.1 Features</td><td>376</td><td>Smart Card Interface
• An error signal can be automatically transmitted on detection of a parity error during reception
• Data can be automatically re-transmitted on detection of a error signal during transmission
• Both direct convention and inverse convention are supported</td></tr>
<tr><td>13.3 Register Descriptions</td><td>379</td><td>The SCI has the following registers for each channel. Some bits in the serial mode register (SMR), serial status register (SSR), and serial control register (SCR) have different functions in different modes .normal serial communication interface mode and smart card interface mode; therefore, the bits are described separately for each mode in the corresponding register sections.</td></tr>
<tr><td>13.3.5 Serial Mode Register (SMR)</td><td>381</td><td>SMR is used to set the SCI's serial transfer format and select the baud rate generator clock source. Some bits in SMR have different functions in normal mode and smart card interface mode.
Table title added
• Normal Serial Communication Interface Mode (When SMIF in SCMR is 0)
Added
• Smart Card Interface Mode (When SMIF in SCMR is 1)
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Initial Value</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td>GM</td><td>0</td><td>R/W</td><td>GS Mode
Setting this bit to 1 allows GSM mode operation. In GSM mode, the TEND set timing is put forward to 11.0 etu from the start and the clock output control function is appended. For details, see section 13.7.9, Clock Output Control.
0: Normal smart card interface mode operation (initial value)
(1) The TEND flag is generated 12.5 etu (11.5 etu in the block transfer mode) after the beginning of the start bit.
(2) Clock output on/off control only.
1: GSM mode operation in smart card interface mode
(1) The TEND flag is generated 11.0 etu after the beginning of the start bit.
(2) In addition to clock output on/off control, high/how fixed control is supported (set using SCR).</td></tr>
<tr><td>6</td><td>BLK</td><td>0</td><td>R/W</td><td>Setting this bit to 1 allows block transfer mode operation.
For details, see section 13.7.4, Block Transfer Mode.
0: Normal smart card interface mode operation (initial value)
(1) Error signal transmission, detection, and automatic data retransmission are performed.
(2) The TXI interrupt is generated by the TEND flag.
(3) The TEND flag is set 12.5 etu (11.0 etu in the GSM mode) after transmission starts.
1: Operation in block transfer mode
(1) Error signal transmission, detection, and automatic data retransmission are not performed.
(2) The TXI interrupt is generated by the TDRE flag.
(3) The TEND flag is set 11.5 etu (11.0 etu in the GSM mode) after transmission starts.</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>13.3.5 Serial Mode Register (SMR)</td><td></td><td>
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Initial Value</th><th>R/W</th><th>Description</th></tr>
<tr><td>5</td><td>PE</td><td>0</td><td>R/W</td><td>Parity Enable
When this bit is set to 1, the parity bit is added to transmit data before transmission, and the parity bit is checked in reception. Set this bit to 1 in smart card interface mode.</td></tr>
<tr><td>4</td><td>O/E</td><td>0</td><td>R/W</td><td>Parity Mode (valid only when the PE bit is 1)
0: Selects even parity
1: Selects odd parity
For details on the usage of this bit in smart card interface mode, see section 13.7.2, Data Format (Except in Block Transfer Mode).</td></tr>
<tr><td>3</td><td>BCP1</td><td>0</td><td>R/W</td><td>Basic Clock Pulse 1,0</td></tr>
<tr><td>2</td><td>BCP0</td><td>0</td><td>R/W</td><td>These bits select the number of basic clock cycles in a 1-bit data transfer time in smart card interface mode.
00: 32 clock cycles (S = 32)
01: 64 clock cycles (S = 64)
10: 372 clock cycles (S = 372)
11: 256 clock cycles (S = 256)
For details, see section 13.7.5, Receive Data Sampling Timing and Reception Margin. S is described in section 13.3.10, Bit Rate Register (BRR).</td></tr>
<tr><td>1</td><td>CKS1</td><td>0</td><td>R/W</td><td>Clock Select 1,0</td></tr>
<tr><td>0</td><td>CKS0</td><td>0</td><td>R/W</td><td>These bits select the clock source for the baud rate generator.
00: φ clock (n = 0)
01: φ /4 clock (n = 1)
10: φ /16 clock (n = 2)
11: φ/64 clock (n = 3)
For the relation between the bit rate register setting and the baud rate, see section 13.3.10, Bit Rate Register (BRR). n is the decimal display of the value of n in BRR (see section 13.3.10, Bit Rate Register (BRR)).</td></tr>
</table>
</td></tr>
<tr><td>13.3.6 Serial Control Register (SCR)</td><td>383</td><td>SCR is a register that enables or disables SCI transfer operations and interrupt requests, and is also used to selection of the transfer clock source. For details on interrupt requests, refer to section 13.9, Interrupts. Some bits in SCR have different functions in normal mode and smart card interface mode.
Table title added
• Normal Serial Communication Interface Mode (When SMIF in SCMR is 0)</td></tr>
</table>

Item	Page	Revision (See Manual for Details)
13.3.6 Serial Control Register (SCR)		Added • Smart Card Interface Mode (When SMIF in SCMR is 1)

Bit	Bit Name	Initial Value	R/W	Description
7	TIE	0	R/W	Transmit Interrupt Enable When this bit is set to 1, TXI interrupt request is enabled. TXI interrupt request cancellation can be performed by reading 1 from the TDRE flag in SSR, then clearing it to 0, or clearing the TIE bit to 0.
6	RIE	0	R/W	Receive Interrupt Enable When this bit is set to 1, RXI and ERI interrupt requests are enabled. RXI and ERI interrupt request cancellation can be performed by reading 1 from the RDRF, FER, PER, or ORER flag in SSR, then clearing the flag to 0, or clearing the RIE bit to 0.
5	TE	0	R/W	Transmit Enable When this bit s set to 1, transmission is enabled. In this state, serial transmission is started when transmit data is written to TDR and the TDRE flag in SSR is cleared to 0. SMR setting must be performed to decide the transfer format before setting the TE bit to 1. When this bit is cleared to 0, the transmission operation is disabled, and the TDRE flag is fixed at 1.
4	RE	0	R/W	Receive Enable When this bit is set to 1, reception is enabled. Serial reception is started in this state when a start bit is detected in asynchronous mode or serial clock input is detected in clocked synchronous mode. SMR setting must be performed to decide the reception format before setting the RE bit to 1. Clearing the RE bit to 0 does not affect the RDRF, FER, PER, and ORER flags, which retain their states.
3	MPIE	0	R/W	Multiprocessor Interrupt Enable (enabled only when the MP bit in SMR is 1 in asynchronous mode) Write 0 to this bit in Smart Card interface mode. When receive data including MPB = 0 is received, receive data transfer from RSR to RDR, receive error detection, and setting of the RERF, FER, and ORER flags in SSR, are not performed. When receive data including MPB = 1 is received, the MPB bit in SSR is set to 1, the MPIE bit is cleared to 0 automatically, and generation of RXI and ERI interrupts (when the TIE and RIE bits in SCR are set to 1) and FER and ORER flag setting are enabled.
2	TEIE	0	R/W	Transmit End Interrupt Enable Write 0 to this bit in Smart Card interface mode. TEI cancellation can be performed by reading 1 from the TDRE flag in SSR, then clearing it to 0 and clearing the TEND flag to 0, or clearing the TEIE bit to 0.

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>13.3.6 Serial Control Register (SCR)</td><td></td><td>
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Initial Value</th><th>R/W</th><th>Description</th></tr>
<tr><td>1</td><td>CKE1</td><td>0</td><td>R/W</td><td>Clock Enable 0 and 1
Enables or disables clock output from the SCK pin. The clock output can be dynamically switched in GSM mode. For details, refer to section 13.7.9, Clock Output Control.
When the GM bit in SMR is 0:
00: Output disabled (SCK pin can be used as an I/O port pin)
01: Clock output
1X: Reserved
When the GM bit in SMR is 1:
00: Output fixed low
01: Clock output
10: Output fixed high
11: Clock output</td></tr>
<tr><td>0</td><td>CKE0</td><td>0</td><td></td><td></td></tr>
</table>
[Legend]
X: Don't care
</td></tr>
<tr><td>13.3.7 Serial Status Register (SSR)</td><td>385</td><td>SSR is a register containing status flags of the SCI and multiprocessor bits for transfer. 1 cannot be written to flags TDRE, RDRF, ORER, PER, and FER; they can only be cleared. Some bits in SSR have different functions in normal mode and smart card interface mode.

Table title added
• Normal Serial Communication Interface Mode (When SMIF in SCMR is 0)

Added
• Smart Card Interface Mode (When SMIF in SCMR is 1)
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Initial Value</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td>TDRE</td><td>1</td><td>R/(W)*1</td><td>Transmit Data Register Empty
Indicates whether TDR contains transmit data.
[Setting conditions]
• When the TE bit in SCR is 0
• When data is transferred from TDR to TSR and data can be written to TDR
[Clearing conditions]
• When 0 is written to TDRE after reading TDRE = 1
• When the DMAC or the DTC*2 is activated by a TXI interrupt request and writes data to TDR</td></tr>
<tr><td>6</td><td>RDRE</td><td>0</td><td>R/(W)*1</td><td>Receive Data Register Full
Indicates that the received data is stored in RDR.
[Setting condition]
• When serial reception ends normally and receive data is transferred from RSR to RDR
[Clearing conditions]
• When 0 is written to RDRF after reading RDRF = 1
• When the DMAC or the DTC*2 is activated by an RXI interrupt and transferred data from RDR
The RDRF flag is not affected and retains their previous values when the RE bit in SCR is cleared to 0. If reception of the next data is completed while the RDRF flag is still set to 1, an overrun error will occur and the receive data will be lost.</td></tr>
</table>
</td></tr>
</table>

Item	Page	Revision (See Manual for Details)
13.3.7 Serial Status Register (SSR)		

Bit	Bit Name	Initial Value	R/W	Description
5	ORER	0	R/(W)*1	Overrun Error Indicates that an overrun error occurred during reception, causing abnormal termination. [Setting condition] When the next serial reception is completed while RDRF = 1 The receive data prior to the overrun error is retained in RDR, and the data received subsequently is lost. Also, subsequent serial cannot be continued while the ORER flag is set to 1. In clocked synchronous mode, serial transmission cannot be continued, either. [Clearing condition] When 0 is written to ORER after reading ORER = 1 The ORER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0.
4	ERS	0	R/(W)*1	Error Signal Status Indicates that the status of an error, signal 1 returned from the reception side at reception [Setting condition] When the low level of the error signal is sampled [Clearing condition] When 0 is written to ERS after reading ERS = 1 The ERS flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0.
3	PER	0	R/(W)*1	Parity Error Indicates that a parity error occurred during reception using parity addition in asynchronous mode, causing abnormal termination. [Setting condition] When a parity error is detected during reception If a parity error occurs, the receive data is transferred to RDR but the RDRF flag is not set. Also, subsequent serial reception cannot be continued while the PER flag is set to 1. In clocked synchronous mode, serial transmission cannot be continued, either. [Clearing condition] When 0 is written to PER after reading PER = 1 The PER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0.

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>13.3.7 Serial Status Register (SSR)</td><td></td><td>
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Initial Value</th><th>R/W</th><th>Description</th></tr>
<tr><td>2</td><td>TEND</td><td>1</td><td>R</td><td>Transmit End
This bit is set to 1 when no error signal has been sent back from the receiving end and the next transmit data is ready to be transferred to TDR.
[Setting conditions]
When the TE bit in SCR is 0 and the ERS bit is also 0
When the ESR bit is 0 and the TDRE bit is 1 after the specified interval following transmission of 1-byte data.
The timing of bit setting differs according to the register setting as follows:
When GM = 0 and BLK = 0, 2.5 etu after transmission starts
When GM = 0 and BLK = 1, 1.0 etu after transmission starts
When GM = 1 and BLK = 0, 1.5 etu after transmission starts
When GM = 1 and BLK = 1, 1.0 etu after transmission starts
[Clearing conditions]
When 0 is written to TDRE after reading TDRE = 1
When the DMAC or the DTC is activated by a TXI interrupt and transfers transmission data to TDR</td></tr>
<tr><td>1</td><td>MPB</td><td>0</td><td>R</td><td>Multiprocessor Bit
This bit is not used in Smart Card interface mode.</td></tr>
<tr><td>0</td><td>MPBT</td><td>0</td><td>R/W</td><td>Multiprocessor Bit Transfer
Write 0 to this bit in Smart Card interface mode.</td></tr>
</table>
Notes: 1. The write value should always be 0 to clear the flag.
2. The clearing conditions using the DTC are that DISEL bit be cleared to 0 and the transfer counter value be other than 0.
</td></tr>
<tr><td>13.3.8 Smart Card Mode Register (SCMR)</td><td>388</td><td>SCMR is a register that selects the transfer format. In this LSI, Smart Card interface mode cannot be specified.
↓
SCMR selects the operation in smart card interface or the data Transfer formats.
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Initial Value</th><th>R/W</th><th>Description</th></tr>
<tr><td>0</td><td>SMIF</td><td>0</td><td>R/W</td><td>Smart Card Interface Mode Select
When this bit is set to 1, smart card interface mode is selected.
0: Normal asynchronous or clocked synchronous mode
1: Smart card interface mode</td></tr>
</table>
</td></tr>
</table>

Item	Page	Revision (See Manual for Details)
13.3.10 Bit Rate Register (BRR)	393	BRR is an 8-bit register that adjusts the bit rate. As the SCI performs baud rate generator control independently for each channel, different bit rates can be set for each channel. Table 13.2 shows the relationships between the N setting in BRR and bit rate B for normal asynchronous mode, clocked synchronous mode, and Smart Card interface mode. The initial value of BRR is H'FF, and it can be read from or written to by the CPU at all times.

Table 13.2 Relationships between the N Setting in BRR and Bit Rate B

Mode	ABCS	Bit Rate	Error
Added			
Smart Card interface mode	x	$B = \frac{\phi \times 10^6}{S \times 2^{2n+1} \times (N + 1)}$	$Error (\%) = \left\| \frac{\phi \times 10^6}{B \times S \times 2^{2n+1} \times (N + 1)} - 1 \right\| \times 100$

[Legend]

B: Bit rate (bps)

N: BRR setting for baud rate generator ($0 \leq N \leq 255$)

ϕ: Operating frequency (MHz)

n, S: Determined by the SMR settings shown in the following tables.

x: Don't care

SMR Setting			
CKS1	CKS0	Clock Source	n
0	0	ϕ	0
0	1	ϕ/4	1
1	0	ϕ/16	2
1	0	ϕ/64	3

Added

SMR Setting		
BCP1	BCP0	S
0	0	32
0	1	64
1	0	372
1	1	256

Table 13.3 shows sample N settings in BRR in normal asynchronous mode. Table 13.4 shows the maximum bit rate for each frequency in normal asynchronous mode. Table 13.6 shows sample N settings in BRR in clocked synchronous mode. Table 13.8 shows sample N settings in BRR in Smart Card interface mode. In Smart Card interface mode, S (the number of basic clock periods in a 1-bit transfer interval) can be selected. For details, see section 13.7.5, Receive Data Sampling and Reception Margin. Tables 13.5 and 13.7 show the maximum bit rates with external clock input.

Item	Page	Revision (See Manual for Details)
13.3.10 Bit Rate Register (BRR)		Added

Table 13.8 BRR Settings for Various Bit Rates (Smart Card Interface Mode, when n = 0 and S = 372)

	Operating Frequency ϕ (MHz)							
Bit Rate	5.00		7.00		7.1424		10.00	
(bps)	N	Error (%)	N	Error (%)	N	Error (%)	N	Error (%)
6720	0	0.01	1	30.00	1	28.57	1	0.01
9600	0	30.00	0	1.99	0	0.00	1	30.00

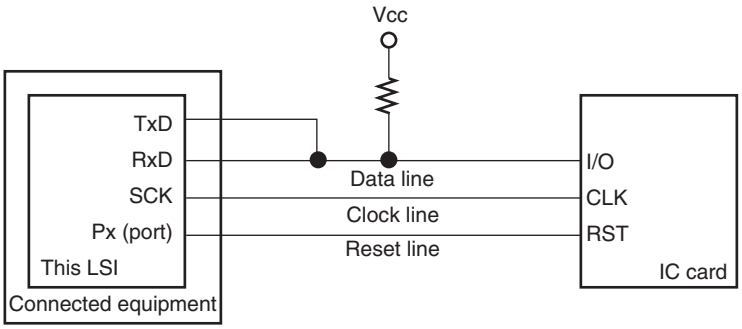
	Operating Frequency ϕ (MHz)							
Bit Rate	10.7136		13.00		14.2848		16.00	
(bps)	N	Error (%)	N	Error (%)	N	Error (%)	N	Error (%)
6720	1	7.14	2	13.33	2	4.76	2	6.67
9600	1	25.00	1	8.99	1	0.00	1	12.01

Added

Table 13.9 Maximum Bit Rate at Various Frequencies (Smart Card Interface Mode)

ϕ (MHz)	Maximum Bit Rate (bps)				n	N
	S = 32	S =64	S = 256	S = 372		
5.00	78125	39063	9766	6720	0	0
6.00	93750	46875	11719	8065	0	0
7.00	109375	54688	13672	9409	0	0
7.1424	111600	55800	13950	9600	0	0
10.00	156250	78125	19531	13441	0	0
10.7136	167400	83700	20925	14400	0	0
13.00	203125	101563	25391	17473	0	0
14.2848	223200	111600	27900	19200		
16.00	250000	125000	31250	21505	0	0

Note: In this LSI, operating frequency ϕ must be 13 MHz or greater.

Item	Page	Revision (See Manual for Details)
Added 13.7 Operation in Smart Card Interface	423	Added **13.7 Operation in Smart Card Interface** The SCI supports an IC card (Smart Card) interface that conforms to ISO/IEC 7816-3 (Identification Card) as a serial communication interface extension function. Switching between the normal serial communication interface and the Smart Card interface mode is carried out by means of a register setting. **13.7.1 Pin Connection Example** Figure 13.24 shows an example of connection with the Smart Card. In communication with an IC card, as both transmission and reception are carried out on a single data transmission line, the TxD pin and RxD pin should be connected to the LSI pin. The data transmission line should be pulled up to the VCC power supply with a resistor. If an IC card is not connected, and the TE and RE bits are both set to 1, closed transmission/reception is possible, enabling self-diagnosis to be carried out. When the clock generated on the Smart Card interface is used by an IC card, the SCK pin output is input to the CLK pin of the IC card. This LSI port output is used as the reset signal.  **Figure 13.24 Schematic Diagram of Smart Card Interface Pin Connections** **13.7.2 Data Format (Except for Block Transfer Mode)** Figure 13.25 shows the transfer data format in Smart Card interface mode. • One frame consists of 8-bit data plus a parity bit in asynchronous mode. • In transmission, a guard time of at least 2 etu (Elementary Time Unit: the time for transfer of one bit) is left between the end of the parity bit and the start of the next frame. • If a parity error is detected during reception, a low error signal level is output for one etu period, 10.5 etu after the start bit. If an error signal is sampled during transmission, the same data is retransmitted automatically after a delay of 2 etu or longer.

Item	Page	Revision (See Manual for Details)
13.7 Operation in Smart Card Interface		

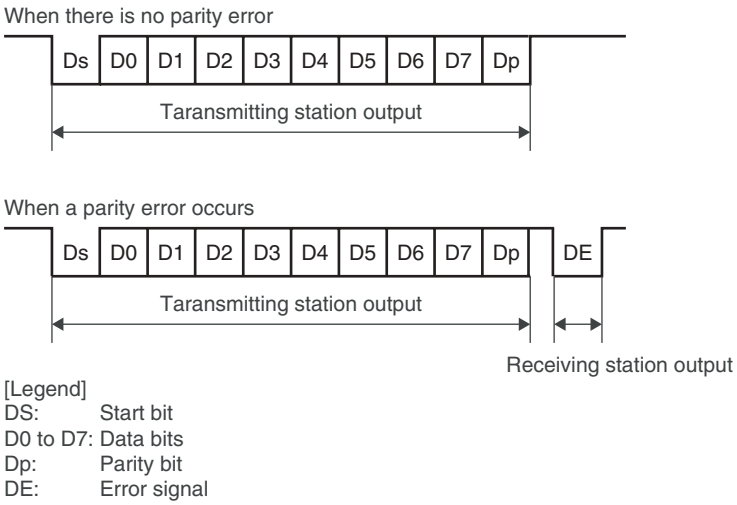


Figure 13.25 Normal Smart Card Interface Data Format

Data transfer with other types of IC cards (direct convention and inverse convention) are performed as described in the following.

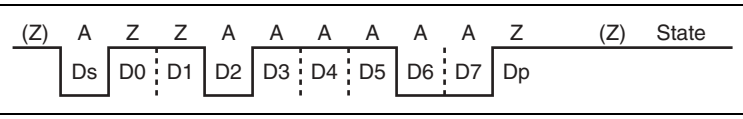


Figure 13.26 Direct Convention (SDIR = SINV = O/E = 0)

With the direction convention type IC and the above sample start character, the logic 1 level corresponds to state Z and the logic 0 level to state A, and transfer is performed in LSB-first order.

The start character data above is H'3B. For the direct convention type, clear the SDIR and SINV bits in SCMR to 0. According to Smart Card regulations, clear the O/E bit in SMR to 0 to select even parity mode.

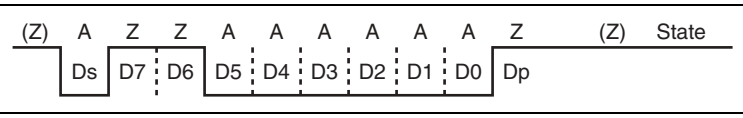


Figure 13.27 Inverse Convention (SDIR = SINV = O/E = 1)

With the inverse convention type, the logic 1 level corresponds to state A and the logic 0 level to state Z, and transfer is performed in MSB-first order. The start character data for the above is H'3F. For the inverse convention type, set the SDIR and SINV bits in SCMR to 1. According to Smart Card regulations, even parity mode is the logic 0 level of the parity bit, and corresponds to state Z. In this LSI, the SINV bit inverts only data bits D0 to D7. Therefore, set the O/E bit in SMR to 1 to invert the parity bit for both transmission and reception.

Item	Page	Revision (See Manual for Details)
13.7 Operation in Smart Card Interface		**13.7.3 Clock** Only an internal clock which is generated by the on-chip baud rate generator is used as a transmit/receive clock. When an output clock is selected by setting CKE0 to 1, a clock with a frequency S* times the bit rate is output from the SCK pin. Note: * S is the value shown in section 13.3.10, Bit Rate Register (BRR). **13.7.4 Block Transfer Mode** Operation in block transfer mode is the same as that in the normal Smart Card interface mode, except for the following points. • In reception, though the parity check is performed, no error signal is output even if an error is • detected. However, the PER bit in SSR is set to 1 and must be cleared before receiving the parity bit of the next frame. • In transmission, a guard time of at least 1 etu is left between the end of the parity bit and the start of the next frame. • In transmission, because retransmission is not performed, the TEND flag is set to 1, 11.5 etu after transmission start. • As with the normal Smart Card interface, the ERS flag indicates the error signal status, but since error signal transfer is not performed, this flag is always cleared to 0. **13.7.5 Receive Data Sampling Timing and Reception Margin** In Smart Card interface mode an internal clock generated by the on-chip baud rate generator can only be used as a transmission/reception clock. In this mode, the SCI operates on a basic clock with a frequency of 32, 64, 372, or 256 times the transfer rate (fixed to 16 times in normal asynchronous mode) as determined by bits BCP1 and BCP0. In reception, the SCI samples the falling edge of the start bit using the basic clock, and performs internal synchronization. As shown in figure 13.28, by sampling receive data at the rising-edge of the 16th, 32nd, 186th, or 128th pulse of the basic clock, data can be latched at the middle of the bit. The reception margin is given by the following formula. $$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5) F - \frac{|D - 0.5|}{N} (1 + F) \right| \times 100 \ [\%]$$ Where M: Reception margin (%) N: Ratio of bit rate to clock (N = 32, 64, 372, and 256) D: Clock duty (D = 0 to 1.0) L: Frame length (L = 10) F: Absolute value of clock frequency deviation

Item	Page	Revision (See Manual for Details)
13.7 Operation in Smart Card Interface		Assuming values of F = 0, D = 0.5 and N = 372 in the above formula, the reception margin formula is as follows. M = (0.5 – 1/2 × 372) × 100% = 49.866%

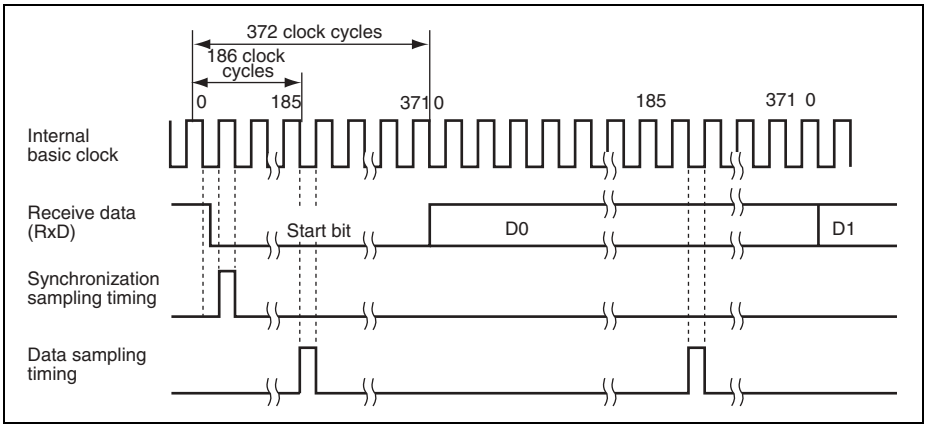


Figure 13.28 Receive Data Sampling Timing in Smart Card Mode (Using Clock of 372 Times the Transfer Rate)

13.7.6 Initialization

Before transmitting and receiving data, initialize the SCI as described below. Initialization is also necessary when switching from transmit mode to receive mode, or vice versa.

1. Clear the TE and RE bits in SCR to 0.
2. Clear the error flags ERS, PER, and ORER in SSR to 0.
3. Set the GM, BLK, O/E, BCP0, BCP1, CKS0, CKS1 bits in SMR. Set the PE bit to 1.
4. Set the SMIF, SDIR, and SINV bits in SCMR.
   When the SMIF bit is set to 1, the TxD and RxD pins are both switched from ports to SCI pins, and are placed in the high-impedance state.
5. Set the value corresponding to the bit rate in BRR.
6. Set the CKE0 and CKE1 bits in SCR. Clear the TIE, RIE, TE, RE, MPIE, and TEIE bits to 0.
   If the CKE0 bit is set to 1, the clock is output from the SCK pin.
7. Wait at least one bit interval, then set the TIE, RIE, TE, and RE bits in SCR. Do not set the TE bit and RE bit at the same time, except for self-diagnosis.

To switch from receive mode to transmit mode, after checking that the SCI has finished reception, initialize the SCI, and set RE to 0 and TE to 1. Whether SCI has finished reception or not can be checked with the RDRF, PER, or ORER flags. To switch from transmit mode to receive mode,

after checking that the SCI has finished transmission, initialize the SCI, and set TE to 0 and RE to 1. Whether SCI has finished transmission or not can be checked with the TEND flag.

Item	Page	Revision (See Manual for Details)
13.7 Operation in Smart Card Interface		**13.7.7 Serial Data Transmission (Except for Block Transfer Mode)** As data transmission in Smart Card interface mode involves error signal sampling and retransmission processing, the operations are different from those in normal serial communication interface mode (except for block transfer mode). Figure 13.29 illustrates the retransfer operation when the SCI is in transmit mode. 1. If an error signal is sent back from the receiving end after transmission of one frame is complete, the ERS bit in SSR is set to 1. If the RIE bit in SCR is enabled at this time, an ERI interrupt request is generated. The ERS bit in SSR should be cleared to 0 by the time the next parity bit is sampled. 2. The TEND bit in SSR is not set for a frame in which an error signal indicating an abnormality is received. Data is retransferred from TDR to TSR, and retransmitted automatically. 3. If an error signal is not sent back from the receiving end, the ERS bit in SSR is not set. Transmission of one frame, including a retransfer, is judged to have been completed, and the TEND bit in SSR is set to 1. If the TIE bit in SCR is enabled at this time, a TXI interrupt request is generated. Writing transmit data to TDR transfers the next transmit data. Figure 13.31 shows a flowchart for transmission. A sequence of transmit operations can be performed automatically by specifying the DTC or the DMAC to be activated with a TXI interrupt source. In a transmit operation, the TDRE flag is set to 1 at the same time as the TEND flag in SSR is set, and a TXI interrupt will be generated if the TIE bit in SCR has been set to 1. If the TXI request is designated beforehand as a DTC* or the DMAC activation source, the DTC* or the DMAC will be activated by the TXI request, and transfer of the transmit data will be carried out. The TDRE and TEND flags are automatically cleared to 0 when data is transferred by the DTC* or the DMAC. In the event of an error, the SCI retransmits the same data automatically. During this period, the TEND flag remains cleared to 0 and the DTC* or the DMAC is not activated. Therefore, the SCI and DTC* or the DMAC will automatically transmit the specified number of bytes in the event of an error, including retransmission. However, the ERS flag is not cleared automatically when an error occurs, and so the RIE bit should be set to 1 beforehand so that an ERI request will be generated in the event of an error, and the ERS flag will be cleared. When performing transfer using the DMAC or the DTC, it is essential to set and enable the DMAC or the DTC* before carrying out SCI setting. For details of the DMAC or the DTC* setting procedures, refer to section 8, Data Transfer Controller (DTC) or section 7, DMA controller (DMAC). Note: * The Flags are automatically cleared by the DTC when the DTC's DISEL bit is cleared to 0 and the transfer counter value is not 0.

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13.7 Operation in Smart Card Interface		

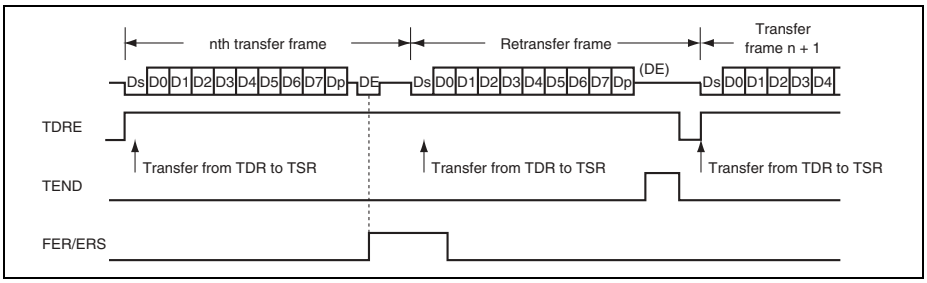

Figure 13.29 Retransfer Operation in SCI Transmit Mode

The timing for setting the TEND flag depends on the value of the GM bit in SMR. The TEND flag set timing is shown in figure 13.30.

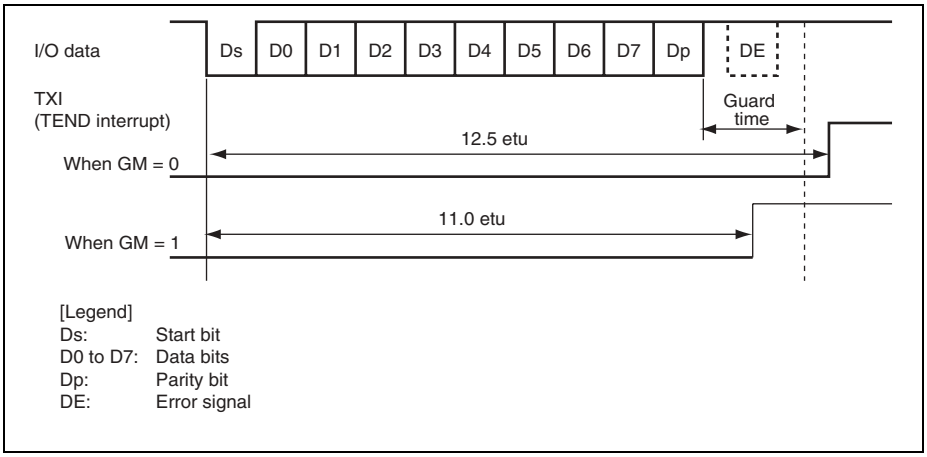

Figure 13.30 TEND Flag Generation Timing in Transmission Operation

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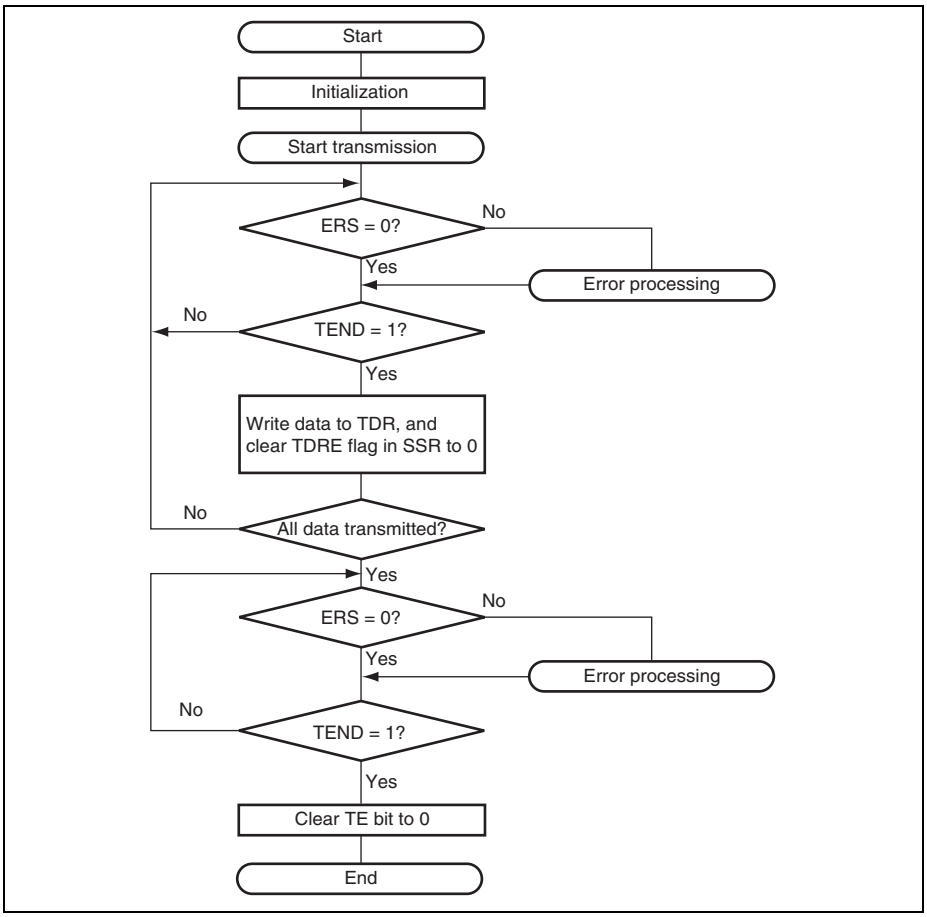
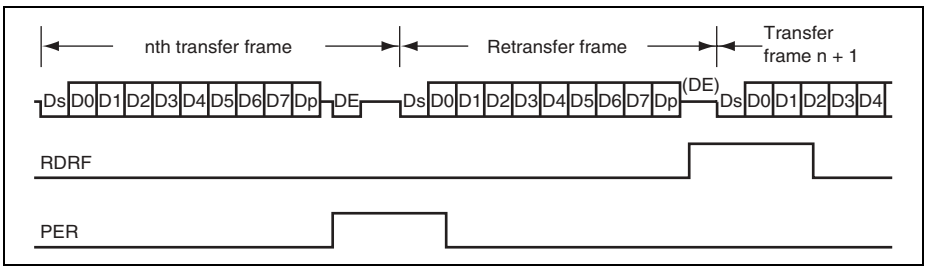
13.7 Operation in Smart Card Interface		

Figure 13.31 Example of Transmission Processing Flow

Item	Page	Revision (See Manual for Details)
13.7 Operation in Smart Card Interface		**13.7.8 Serial Data Reception (Except for Block Transfer Mode)** Data reception in Smart Card interface mode uses the same operation procedure as for normal serial communication interface mode. Figure 13.32 illustrates the retransfer operation when the SCI is in receive mode. 1. If an error is found when the received parity bit is checked, the PER bit in SSR is automatically set to 1. If the RIE bit in SCR is set at this time, an ERI interrupt request is generated. The PER bit in SSR should be kept cleared to 0 until the next parity bit is sampled. 2. The RDRF bit in SSR is not set for a frame in which an error has occurred. 3. If no error is found when the received parity bit is checked, the PER bit in SSR is not set to 1, the receive operation is judged to have been completed normally, and the RDRF flag in SSR is automatically set to 1. If the RIE bit in SCR is enabled at this time, an RXI interrupt request is generated. Figure 13.33 shows a flowchart for reception. A sequence of receive operations can be performed automatically by specifying the DTC* or the DMAC to be activated using an RXI interrupt source. In a receive operation, an RXI interrupt request is generated when the RDRF flag in SSR is set to 1. If the RXI request is designated beforehand as a DTC* or the DMAC activation source, the DTC* or the DMAC will be activated by the RXI request, and the receive data will be transferred. The RDRF flag is cleared to 0 automatically when data is transferred by the DTC* or the DMAC. If an error occurs in receive mode and the ORER or PER flag is set to 1, a transfer error interrupt (ERI) request will be generated. Hence, so the error flag must be cleared to 0. In the event of an error, the DTC* or the DMAC is not activated and receive data is skipped. Therefore, receive data is transferred for only the specified number of bytes in the event of an error. Even when a parity error occurs in receive mode and the PER flag is set to 1, the data that has been received is transferred to RDR and can be read from there. Note: For details on receive operations in block transfer mode, refer to section 13.4, Operation in Asynchronous Mode. * The Flags are automatically cleared by the DTC when the DTC's DISEL bit is cleared to 0 and the transfer counter value is not 0.  **Figure 13.32 Retransfer Operation in SCI Receive Mode**

Item	Page	Revision (See Manual for Details)
13.7 Operation in Smart Card Interface		

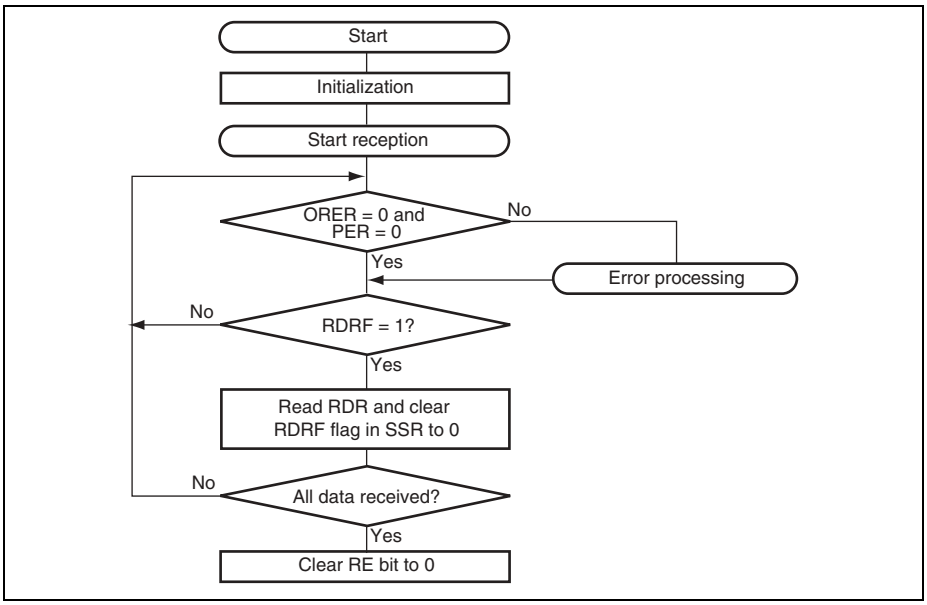


Figure 13.33 Example of Reception Processing Flow

13.7.9 Clock Output Control

When the GM bit in SMR is set to 1, the clock output level can be fixed with bits CKE0 and CKE1 in SCR. At this time, the minimum clock pulse width can be made the specified width. Figure 13.34 shows the timing for fixing the clock output level. In this example, GM is set to 1, CKE1 is cleared to 0, and the CKE0 bit is controlled.

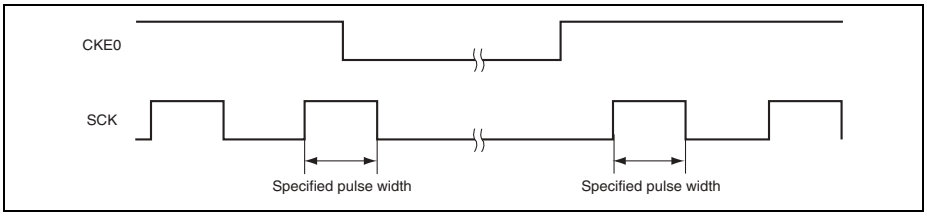
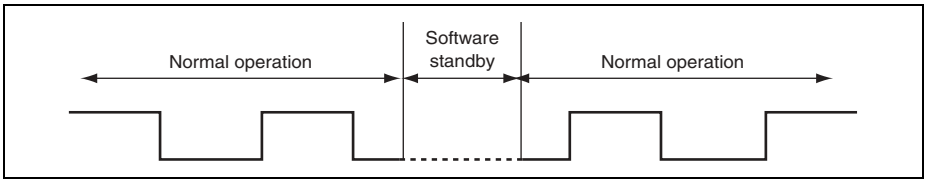


Figure 13.34 Timing for Fixing Clock Output Level

Item	Page	Revision (See Manual for Details)
13.7 Operation in Smart Card Interface		When turning on the power or switching between Smart Card interface mode and software standby mode, the following procedures should be followed in order to maintain the clock duty. **Powering On:** To secure clock duty from power-on, the following switching procedure should be followed. 1. The initial state is port input and high impedance. Use a pull-up resistor or pull-down resistor to fix the potential. 2. Fix the SCK pin to the specified output level with the CKE1 bit in SCR. 3. Set SMR and SCMR, and switch to smart card mode operation. 4. Set the CKE0 bit in SCR to 1 to start clock output. **When changing from smart card interface mode to software standby mode:** 1. Set the data register (DR) and data direction register (DDR) corresponding to the SCK pin to the value for the fixed output state in software standby mode. 2. Write 0 to the TE bit and RE bit in the serial control register (SCR) to halt transmit/receive operation. At the same time, set the CKE1 bit to the value for the fixed output state in software standby mode. 3. Write 0 to the CKE0 bit in SCR to halt the clock. 4. Wait for one serial clock period. During this interval, clock output is fixed at the specified level, with the duty preserved. 5. Make the transition to the software standby state. When returning to smart card interface mode from software standby mode: 1. Exit the software standby state. 2. Write 1 to the CKE0 bit in SCR and output the clock. Signal generation is started with the normal duty.  **Figure 13.35 Clock Halt and Restart Procedure**

Item	Page	Revision (See Manual for Details)
13.8 Interrupts	427	Added

13.9.2 Interrupts in Smart Card Interface Mode

Table 13.13 shows the interrupt sources in Smart Card interface mode. The transmit end interrupt (TEI) request cannot be used in this mode.

Note: In case of block transfer mode, see section 13.9.1, Interrupts in Normal Serial Communication Interface Mode.

Table 13.13 Interrupt Sources in Smart Card Interface Mode

Channel	Name	Interrupt Source	Interrupt Flag	DTC Activation	DMAC Activation	Priority*
0	ERI0	Receive Error, Detection	ORER, PER, ERS	Not possible	Not possible	High
	RXI0	Receive Data Full	RDRF	Possible	Possible	
	TXI0	Transmit Data Empty	TEND	Possible	Possible	
1	ERI1	Receive Error, Detection	ORER, PER, ERS	Not possible	Not possible	
	RXI1	Receive Data Full	RDRF	Possible	Possible	
	TXI1	Transmit Data Empty	TEND	Possible	Possible	
2	ERI2	Receive Error, Detection	ORER, PER, ERS	Not possible	Not possible	
	RXI2	Receive Data Full	RDRF	Possible	Not possible	
	TXI2	Transmit Data Empty	TEND	Possible	Not possible	Low

Note: * Indicates the initial state immediately after a reset. Priorities in channels can be changed by the interrupt controller.