

# RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan  
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RZ*-A0150A/E	Rev.	1.00
Title	External interrupt input detection failure and DREQ input setting correction		Information Category	Technical Notification		
Applicable Product	RZ/T2M Group, RZ/T2ME Group, RZ/T2L Group, RZ/N2L Group, RZ/T2H and RZ/N2H Groups	Lot No.	Reference Document	RZ/T2M Group User's Manual: Hardware Rev.1.20 (R01UH0916EJ0120), RZ/T2ME Group User's Manual: Hardware Rev.1.00 (R01UH1062EJ0100), RZ/T2L Group User's Manual: Hardware Rev.1.20 (R01UH0985EJ0120), RZ/N2L Group User's Manual: Hardware Rev.1.30 (R01UH0955EJ0130), RZ/T2H and RZ/N2H Groups User's Manual: Hardware Rev.1.10 (R01UH1039EJ0110)		
		All lots				

This document describes an issue and workaround with the external interrupt input detection, and a correction about DREQ input setting.

## 1. Issue

If the timing of an external interrupt input signal change coincides with the rising edge of the clock used in the edge detection circuit, the edge of the interrupt/request signal may occasionally be missed.

### - Affected items

#### • Input signal:

NMI, IRQ0 – IRQ15 (RZ/T2M, T2ME, T2L, and N2L)

SEI, IRQ0 – IRQ15 (RZ/T2H and N2H)

#### • Detection mode: Falling edge, Rising edge, and Falling and rising edge

### - Occurrence conditions

When the detection mode for external interrupt input is set to falling edge, rising edge or both falling and rising edge, and the noise filter for the interrupt/request input is disabled.

Note: When detection mode is set to low level, this issue is NOT applicable.

## 2. Workaround

When the detection mode for the external interrupt input is set to the edge detection, the noise filter for the input must be enabled. Noise filter settings are configured using Interrupt Noise Filter Enable Register for Safety Register (S\_PORTNF\_FLTSEL) and Interrupt Noise Filter Enable Register (NS\_PORTNF\_FLTSEL).

There is no restrictions on the sampling clock settings for the noise filter.

3. Correction about DREQ input setting

The DREQ input detection mode is performed in the Channel Configuration Register (CHCFG\_n) in DMAC, NOT in the Interrupt Edge Detection Setting Register (NS\_PORTNF\_MD). Therefore, The correct description of the MDDRQ[1:0] bits in the NS\_PORTNF\_MD is as below.

When DREQ input is used, the MDDRQ bits in the NS\_PORTNF\_MD register must be set to 00b.

Bit	Symbol	Function	R/W
29:28	MDDRQ[1:0]	Select input mode for DREQ of DMAC 0 0: Invert Others: Prohibited	R/W

4. AC timing correction

Enabling the noise filter will change the AC timing for the interrupt/request input as below. Please note that.

1) RZ/T2M, T2ME, T2L, and N2L

**Table 1 Interrupt Timing**

Parameter		Symbol	Min	Typ	Max	Unit
NMI pulse width	Level detection	t <sub>NMIW</sub>	t <sub>l<sub>cyc</sub></sub> × 2 <sup>*1</sup>	—	—	ns
	Edge detection		t <sub>PMcyc</sub> × 3.5 <sup>*2,*3</sup>	—	—	ns
IRQ pulse width	Level detection	t <sub>IRQW</sub>	t <sub>l<sub>cyc</sub></sub> × 2 <sup>*1</sup>	—	—	ns
	Edge detection		t <sub>PMcyc</sub> × 3.5 <sup>*2,*3</sup>	—	—	ns

Note 1. t<sub>l<sub>cyc</sub></sub>: ICLK cycle

Note 2. t<sub>PMcyc</sub>: PCLKM cycle

Note 3. This value is when noise filter sampling frequency divided rate is 1. In other cases, it is [clock division rate] × t<sub>PMcyc</sub> × 3.5.

**Table 2 DMAC Timing**

Parameter	Symbol	Min <sup>*1</sup>	Typ	Max	Unit
DREQ pulse width	t <sub>DRQW</sub>	t <sub>l<sub>cyc</sub></sub> × 2	—	—	ns

Note 1. t<sub>l<sub>cyc</sub></sub>: ICLK cycle

2) RZ/T2H and N2H

**Table 1 Interrupt Timing**

Parameter		Symbol	Min	Typ	Max	Unit
NMI pulse width	Level detection	t <sub>NMIW</sub>	t <sub>PHcyc</sub> × 2 <sup>*1</sup>	—	—	ns
	Edge detection		t <sub>PMcyc</sub> × 3.5 <sup>*2,*3</sup>	—	—	ns
IRQ pulse width	Level detection	t <sub>IRQW</sub>	t <sub>PHcyc</sub> × 2 <sup>*1</sup>	—	—	ns
	Edge detection		t <sub>PMcyc</sub> × 3.5 <sup>*2,*3</sup>	—	—	ns

Note 1. t<sub>PHcyc</sub>: PCLKH cycle

Note 2. t<sub>PMcyc</sub>: PCLKM cycle

Note 3. This value is when noise filter sampling frequency divided rate is 1. In other cases, it is [clock division rate] × t<sub>PMcyc</sub> × 3.5.

**Table 2 DMAC Timing**

Parameter	Symbol	Min <sup>*1</sup>	Typ	Max	Unit
DREQ pulse width	t <sub>DRQW</sub>	t <sub>PHcyc</sub> × 2	—	—	ns

Note 1. t<sub>PHcyc</sub>: PCLKH cycle