Date: Jun. 30, 2023

# RENESAS TECHNICAL UPDATE

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| Product Category | MPU/MCU | | Document No. | TN-RZ*-A0111A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | Ethernet Switch (ETHSW) function issue | | Information Category | Technical Notification | | |
| Applicable Product | RZ/T2M Group<br>RZ/N2L Group | Lot No.<br>All | Reference Document | RZ/T2M Group User's Manual: Hardware Rev.1.10 (R01UH0916EJ0110)<br>RZ/N2L Group User's Manual: Hardware Rev.1.20 (R01UH0955EJ0120) | | |

We would like to inform about issues regarding Ethernet Switch (ETHSW) function as described below.

| No. | Issues | Workaround |
|---|---|---|
| 1 | TX_RESPONSE_OK_CNT and TX_VERIFY_OK_CNT registers may be incremented count incorrectly. | No workaround. Do not use TX_RESPONSE_OK_CNT and TX_VERIFY_OK_CNT registers. Count the frame by software if needed. |
| 2 | When FRM_LENGTH register in port 3 (Management port) is set to very small value, the frame may be discarded since the frame length may be incorrectly detected as oversize. | Set FRM_LENGTH register in port 3 to more than or equal to the initial value. When you want to limit the frame length of the received frame, use FRM_LENGTH registers in port 0 to port2. |
| 3 | When setting 0 to the INT_VALUE bit in TDMA_CTR1 register, the interrupt is not generated. | When using the interrupt by TDMA_CTR1, set the value other than 0 to the INT_VALUE bit. |
| 4 | When Transmit Timestamp Capture Overflow occurs, Transmit Timestamp Capture Overflow interrupt may not be generated. | Do not use Transmit Timestamp Capture Overflow interrupt. Instead, use Transmit Timestamp Capture interrupt and obtain the captured timestamp before overflow occurs. |
| 5 | The IRQ_STAT bit in TSM_IRQ_STAT_ACK register does not show the TSM interrupt pending status correctly. | When checking TSM interrupt pending status, do not use the IRQ_STAT bit in TSM_IRQ_STAT_ACK register but the TSM_INT bit in the INT_STAT_ACK register. |
| 6 | When reading MDIO related registers (MDIO_CFG_STATUS, MDIO_COMMAND and MDIO_DATA) after reading statistic counter registers from 0x8102_0300 to 0x8102_033C, the read value from MDIO related registers may be incorrect. | When reading statistic counter registers between 0x8102_0300 to 0x8102_033C, perform dummy read to the 0x8102_0310 after the reading. |