To our customers,

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On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Renesas Technology Corp.

Product Category	MPU&MCU		Document No.	TN-SH7-A600A/E	Rev.	1.00
Title	Error corrections and addition of usage notes to the SH7261 Group and SH7201 Group Hardware Manuals		Information Category	Technical Notification		
Applicable Product	SH7261 Group SH7201 Group	Lot No. All lots	Reference Document	SH7261 Group Hardware Manual Rev.1.00 REJ09B0320-0100 SH7201 Group Hardware Manual Rev.1.00 REJ09B0321-0100		

Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of error corrections and addition of usage note to the SH7261 Group and SH7201 Group Hardware Manuals (Rev.1.00). Please take this information into consideration when using these products.

Section 1 Overview

[On page 10 in the SH7261 Group Hardware Manual]

1.2 Product Lineup

Table 1.2 Product Lineup

[Before change]

Abbreviation	Product Code	RCAN-ET	IEB	Operating Temperature
R5S72611	R5S72611B120FP	Supported	Not supported	–20 to +70°C (Regular specifications)
	R5S72611P100FP			–40 to +85°C (Wide-range specifications)
	R5S72611P80FP			–40 to +85°C (Wide-range specifications)
R5S72612	R5S72612B120FP	Not supported	Supported	–20 to +70°C (Regular specifications)
	R5S72612P100FP			–40 to +85°C (Wide-range specifications)
	R5S72612P80FP			–40 to +85°C (Wide-range specifications)
R5S72613	R5S72613B120FP	Supported	Supported	–20 to +70°C (Regular specifications)
	R5S72613P100FP			–40 to +85°C (Wide-range specifications)
	R5S72613P80FP			–40 to +85°C (Wide-range specifications)

[After change]

Abbreviation	Product Code	RCAN-ET	IEB	Operating Temperature
R5S72611	R5S72611RB120FP	Supported	Not supported	–20 to +70°C (Regular specifications)
	R5S72611RP100FP			–40 to +85°C (Wide-range specifications)
	R5S72611RP80FP			–40 to +85°C (Wide-range specifications)
R5S72612	R5S72612RB120FP	Not supported	Supported	–20 to +70°C (Regular specifications)
	R5S72612RP100FP			–40 to +85°C (Wide-range specifications)
	R5S72612RP80FP			–40 to +85°C (Wide-range specifications)
R5S72613	R5S72613RB120FP	Supported	Supported	–20 to +70°C (Regular specifications)
	R5S72613RP100FP			–40 to +85°C (Wide-range specifications)
	R5S72613RP80FP			–40 to +85°C (Wide-range specifications)

[On page 8 in the SH7201 Group Hardware Manual]

1.2 Product Lineup

Table 1.2 Product Lineup

[Before change]

Abbreviation	Product Code	Operating Temperature
R5S72011	R5S72011B120FP	–20 to +70°C (Regular specifications)
	R5S72011W100FP	–20 to +85°C (Wide-range specifications)

[After change]

Abbreviation	Product Code	Operating Temperature
R5S72011	R5S72011RB120FP	–20 to +70°C (Regular specifications)
	R5S72011RW100FP	–20 to +85°C (Wide-range specifications)

Section 4 Clock Pulse Generator (CPG)

[On page 90 in the SH7261 Group Hardware Manual, on page 86 in the SH7201 Group Hardware Manual]

4.4.2 CKIO Control Register (CKIOCR)

[Before change]

When this LSI is started in clock operating mode 3, CKIOCR is initialized to H'00 by a power-on reset or in deep standby mode. When this LSI is started in clock operating mode 0 or 2, CKIOCR is initialized to H'01 by a power-on reset or in deep standby mode. This register is not initialized by a manual reset, in sleep mode, or in software standby mode.

[After change]

When this LSI is started in clock operating mode 3, CKIOCR is initialized to H'00 by a power-on reset caused by the $\overline{\text{RES}}$ pin or in deep standby mode. When this LSI is started in clock operating mode 0 or 2, CKIOCR is initialized to H'01 by a power-on reset caused by the $\overline{\text{RES}}$ pin or in deep standby mode. This register is not initialized by an internal reset triggered by an overflow of the WDT, manual reset, in sleep mode, or in software standby mode.

Section 9 Bus State Controller (BSC)

[On page 263 in the SH7261 Group Hardware Manual, on page 259 in the SH7201 Group Hardware Manual]

The description on (c), Byte Access Control by DQM, and two figures (figures 9.21 and 9.22) are newly added. The number of following figures will be modified accordingly.

(c) Byte Access Control by DQM

Figure 9.21 shows a timing example for byte writing to the SDRAM with a 16-bit bus width, and figure 19.22 for byte reading from the SDRAM with a 16-bit bus width. In the SDRAM access, the DQM signal is asserted when data is masked.

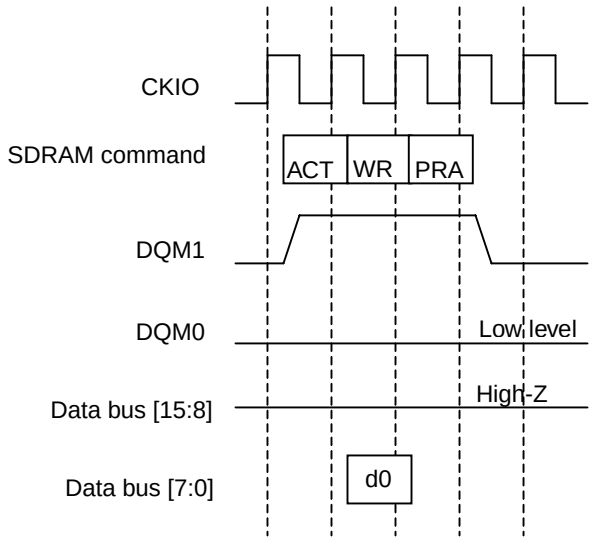

Figure 9.21 Byte Write Timing to SDRAM with 16-Bit Bus Width (Example)

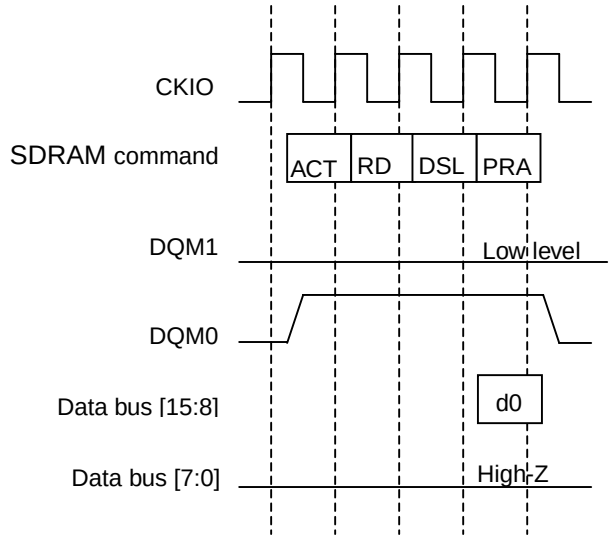

Figure 9.22 Byte Read Timing from SDRAM with 16-Bit Bus Width (Example)

Section 11 Direct Memory Access Controller (DMAC)

[On page 302 in the SH7261 Group Hardware Manual, on page 298 in the SH7201 Group Hardware Manual]

[Modified as follows]

Notes: Terminologies in this section are as follows:

1. Single data transfer: Transfer in one read cycle and one write cycle by the DMAC (in the case of dual address transfer)~~, and one read cycle or one write cycle transfer by the DMAC (at single address transfer)~~

   :

6. BIU: Bus Interface Unit (peripheral module). One of the following four kinds according to the source or destination of transfer.

   BIU_E: External space (normal space and SDRAM space)

   BIU_P: Peripheral bus (1) (see figure 1.1)

   BIU_SH: Peripheral bus (2) (see figure 1.1), on-chip RAM space

   BIU_C: Peripheral bus (3) (see figure 1.1)

Section 18 Serial Sound Interface (SSI)

[On page 772 in the SH7261 Group Hardware Manual, on page 768 in the SH7201 Group Hardware Manual]

The following note is added to the description on bit 11 (SPDP) of the control register (SSICR).

Bit	Bit Name	Initial Value	R/W	Description
11	SPDP	0	R/W	Serial Padding Polarity 0: Padding bits are low. 1: Padding bits are high. Note: When MUEN = 1, padding bits are low. (The MUTE function is given a priority.)

[On page 777 in the SH7261 Group Hardware Manual, on page 773 in the SH7201 Group Hardware Manual]

The location of the note in bit 26 (OIRQ) of the status register (SSISR) is changed as follows.

Bit	Bit Name	Initial Value	R/W	Description
26	OIRQ	0	R/W*[1]	Overflow Error Interrupt Status Flag : • TRMD = 0 (Receive mode) If OIRQ = 1, SSIRDR was not read before there was new unread data written to it. This will lead to the loss of a sample and a potential corruption of multi-channel data. Note: When overflow error occurs, the current data in the data buffer of this module is overwritten by the next incoming data from the SSI interface. • TRMD = 1 (Transmit mode) If OIRQ = 1, SSITDR had data written to it before it was transferred to the shift register. This will lead to the loss of a sample and a potential corruption of multi-channel data.

[On page 779 in the SH7261 Group Hardware Manual, on page 775 in the SH7201 Group Hardware Manual]

The description on bit 0 (IDST) of the status register (SSISR) is changed as follows.

[Before change]

Bit	Bit Name	Initial Value	R/W	Description
0	IDST	1*2	R	Idle Mode Status Flag : • SSI = Master transmitter (SWSD = 1 and TRMD = 1) This bit is set to 1 if all the data in the system word to be transmitted has been written to SSITDR and if the EN bit is cleared to end the system word currently being output. :

[After change]

Bit	Bit Name	Initial Value	R/W	Description
0	IDST	1*2	R	Idle Mode Status Flag : • SSI = Master transmitter (SWSD = 1 and TRMD = 1) This bit is set to 1 if the EN bit is cleared and the data written to SSITDR is completely output from the serial data input/output pin (SSIDATA), that is, the output of the system word length is completed. :

[On page 781 in the SH7261 Group Hardware Manual, on page 777 in the SH7201 Group Hardware Manual]

[Modified as follows]

18.4.1 Bus Format

:

The bus format can be selected from one of the four major modes shown in table 18.3.

[On page 785 in the SH7261 Group Hardware Manual, on page 781 in the SH7201 Group Hardware Manual]

[Modified as follows]

(6) Multi-channel Formats

:

The SSI module supports the transfer of 2, 3, and 4 channels by using the CHNL, SWL and DWL bits only when the system word length (SWL) is greater than or equal to the data word length (DWL) multiplied by channels (CHNL).

[On page 787 in the SH7261 Group Hardware Manual, on page 783 in the SH7201 Group Hardware Manual]

[Modified as follows]

Figures 18.7 to 18.9 show how 2, 3 and 4 channels are transferred to the serial audio bus. Note that there are no padding bits in the first example, the second example is left-aligned and the third is right-aligned. This selection is arbitrary and is just for demonstration purposes only.

[On page 787 in the SH7261 Group Hardware Manual, on page 783 in the SH7201 Group Hardware Manual]

The contents and title of figure 18.7 are modified as follows.

SCKP = 0, SWSP = 0, DEL = 1, CHNL = 01, SPDP = don't care, SDTA = don't care
System word length = data word length × 2

Figure 18.7 Multichannel Format (2 Channels Without Padding)

[On page 787 in the SH7261 Group Hardware Manual, on page 783 in the SH7201 Group Hardware Manual]

The contents and title of figure 18.8 are modified as follows.

SCKP = 0, SWSP = 0, DEL = 1, CHNL = 10, SPDP = 1, SDTA = 0
System word length = data word length × 3

Figure 18.8 Multichannel Format (3 Channels with High Padding)

[On page 788 in the SH7261 Group Hardware Manual, on page 784 in the SH7201 Group Hardware Manual]

The contents and title of figure 18.9 are modified as follows.

SCKP = 0, SWSP = 0, DEL = 1, CHNL = 11, SPDP = 0, SDTA = 1
System word length = data word length × 4

Figure 18.9 Multichannel Format (4 Channels; Transmitting and Receiving in the order of Padding Bits and Serial Data; with Padding)

Section 19 Controller Area Network (RCAN-ET)

[On page 854 in the SH7261 Group Hardware Manual, on page 850 in the SH7201 Group Hardware Manual]

[Modified as follows]

Figure 19.8 - Halt Mode/Sleep Mode shows allowed state transition.

- Do not set MCR5 (Sleep Mode) without entering Halt Mode.
- After setting MCR1, make sure that GSR4 is set and the RCAN-ET has entered Halt Mode before clearing MCR1.

Section 20 IEBus™ Controller (IEB)

[On page 934 in the SH7261 Group Hardware Manual]

The description on section 20.8, Usage Notes, is added.

20.8 Usage Notes

20.8.1 Notes when the Communications have not been completed within the Maximum Number of Transmit Bytes

(1) Data Transmission

During the data transmission, when the maximum number of bytes defined by the communications mode have been transmitted because a NAK has been received from the receive unit, or when transmission has not been completed within the maximum number of transmit bytes because the message length value exceeds it, the IEB sets the error flag of IETSR and enters the wait state. In this case, the IEB transmits data for the maximum number of transmit bytes + one byte. Then, if a NAK has been received in an acknowledge bit of data for the maximum number of transmit bytes + one byte, the TXERO flag is set. If an ACK is received, the TXF flag is set.

Figure 20.18 shows the operation timing when the transmission has not been completed within the maximum number of transmit bytes.

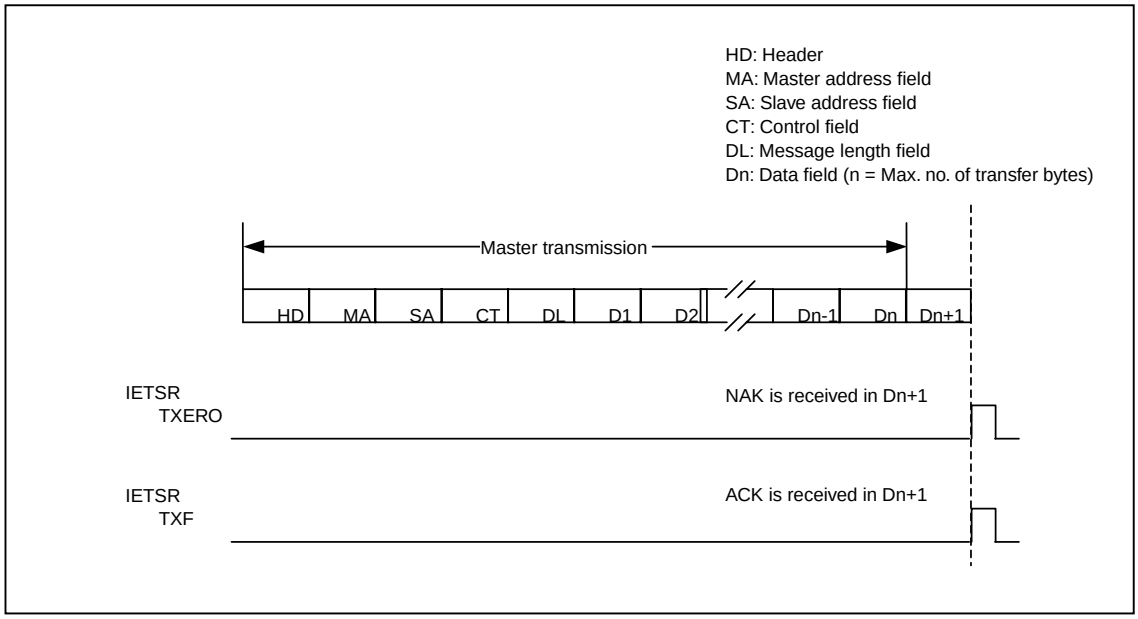

Figure 20.18 Operation Timing when Transmission has not been Completed within Maximum Number of Transmit Bytes

(2) Data Reception

During the data reception, when reception has not been completed within the maximum number of bytes defined by the communications mode because of a parity error or overrun error causing the retransfer of data, or when reception has not been completed because the message length value exceeds the maximum number of receive bytes, the IEB sets the error flag of IERSR and enters the wait state. In this case, the IEB waits for data for the maximum number of receive bytes + one byte. Then, if data for the maximum number of receive bytes + one byte is not received, a receive timing error is detected and the RXERTME flag is set. In this case, the RXEDLE flag is not set. The RXEDLE flag is set when data for the maximum number of receive bytes + one byte is received.

The IEB also waits for data for the maximum number of receive bytes + one byte, when the maximum number of receive bytes have been received but the parity error is not cleared. If data for the maximum number of receive bytes + one byte is not received, the RXERTME flag is set. In this case, the RXEPE flag is not set. The RXEPE flag is set when data for the maximum number of receive bytes + one byte is received.

Figure 20.19 shows the operation timing when the reception has not been completed within the maximum number of receive bytes.

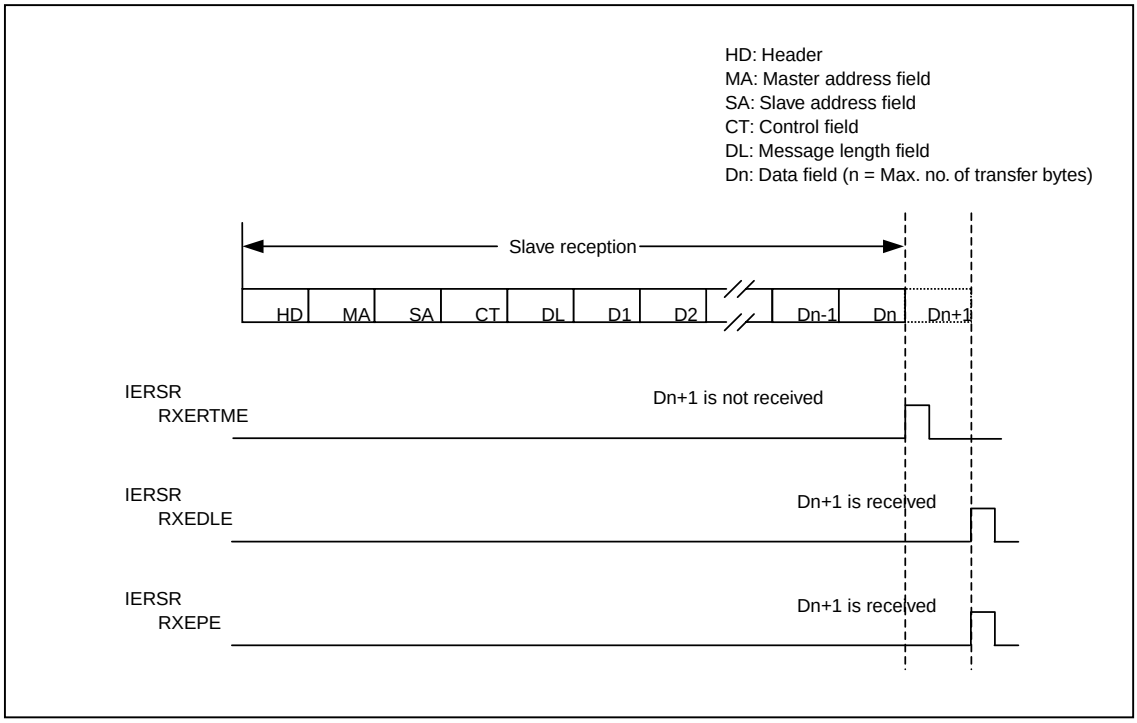

Figure 20.19 Operation Timing when Reception has not been Completed within Maximum Number of Receive Bytes

Section 22 A/D Converter (ADC)

[On page 1028 in the SH7261 Group Hardware Manual, on page 890 in the SH7201 Group Hardware Manual]

The description on section 22.7.7, Usage Note when Shifting to Single Mode during A/D Conversion, is added.

22.7.7 Usage Note when Shifting to Single Mode during A/D Conversion

During the A/D conversion in scan mode or multi mode, if the A/D conversion is stopped by clearing the A/D start bit (ASDT) in ADCSR to 0 and restarted after a transition to single mode, make sure to set ASDT to 1 after the time required for one-channel A/D conversion has elapsed.

Section 27 Power-Down Modes

[On page 1131 in the SH7261 Group Hardware Manual, on page 993 in the SH7201 Group Hardware Manual]

27.2.9 Deep Standby Oscillation Settling Clock Select Register (DSCNT)

[Before change]

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	CKS[2:0]	000	R/W	Clock Select Selects the clock used to count the oscillation settling time from among eight types clocks derived by dividing the peripheral clock (Pϕ). The oscillation settling time is calculated as follows: Oscillation settling time = 1/Pϕ × Division ratio specified by CKS[2:0] × 255 [µs] The following are the oscillation settling times when the peripheral clock (Pϕ) is running at 5, 10, and 15 MHz.

Setting value	Clock select	Oscillation settling time (ms) 5 MHz	10 MHz	15 MHz
000:	1 x Pϕ	0.05	0.03	0.02
001:	1/64 x Pϕ	3.26	1.63	1.09
010:	1/128 x Pϕ	6.53	3.26	2.18
011:	1/256 x Pϕ	13.06	6.53	4.35
100:	1/512 x Pϕ	26.11	13.06	8.70
101:	1/1024 x Pϕ	52.22	26.11	17.41
110:	1/4096 x Pϕ	208.90	104.45	69.63
111:	1/16384 x Pϕ	835.58	417.79	278.53

[After change]

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	CKS[2:0]	000	R/W	Clock Select Selects the clock used to count the oscillation settling time from among eight types clocks derived by dividing the peripheral clock (Pϕ). The oscillation settling time is calculated as follows: Oscillation settling time = 1/Pϕ × Division ratio specified by CKS[2:0] × 255 [µs] The following are the oscillation settling times when the peripheral clock (Pϕ) is running at 5, 10, and 15 MHz.

Setting value	Clock select	Oscillation settling time (ms) 5 MHz	10 MHz	15 MHz
000:	1 x Pϕ*1	0.05	0.03	0.02
001:	1/64 x Pϕ*1	3.26	1.63	1.09
010:	1/128 x Pϕ*1	6.53	3.26	2.18
011:	1/256 x Pϕ*2	13.06	6.53	4.35
100:	1/512 x Pϕ*2	26.11	13.06	8.70
101:	1/1024 x Pϕ	52.22	26.11	17.41
110:	1/4096 x Pϕ	208.90	104.45	69.63
111:	1/16384 x Pϕ	835.58	417.79	278.53

Notes: 1. Setting prohibited.

2. Set the clock so that it is equal to or longer than the oscillation settling time 2 on return from standby (t_{OSC3}).

[On page 1143 in the SH7261 Group Hardware Manual, on page 1005 in the SH7201 Group Hardware Manual]

The description on section 27.4.2, Note on Canceling Standby Mode when External Clock is Input, is added.

27.4.1 Note on Setting Registers

When writing to the registers related to power-down modes, note the following.

When writing to the register related to power-down modes, the CPU, after executing a write instruction, executes the next instruction without waiting for the write operation to complete. Therefore, to reflect the change specified by writing to the register while the next instruction is executed, insert a dummy read of the same register between the register write instruction and the next instruction.

27.4.2 Note on Canceling Standby Mode when External Clock is Input

When standby mode is canceled by NMI interrupt or IRQ interrupt and an external clock from the EXTAL pin or CKIO pin is used, make sure that the external clock is input before the interrupt is input. If not so, the oscillation settling time could not be counted correctly.

Appendix

[On page 1286 in the SH7261 Group Hardware Manual, on page 1140 in the SH7201 Group Hardware Manual]

A. Pin States

Table A.1 Pin States

[Before change]

Pin Function		Pin State						
		Reset State				Power-Down State		
		Power-On						
		Area 0 Data Bus Width						
Type	Pin Name	8 Bits	16 Bits	32 Bits	Manual	Sleep	Software Standby	Deep Standby
Bus control	$\overline{\text{WAIT}}$	—			I	I	Z	Z
	$\overline{\text{CSO}}$	H			O	O	H	K
	$\overline{\text{CS6}}$ to $\overline{\text{CS1}}$	—			O	O	H	K
	$\overline{\text{RD}}$	H			O	O	H	K
	$\overline{\text{WR3}}$	—	—	H	O	O	H	K
	$\overline{\text{WR2}}$	—	—	H	O	O	H	K
	$\overline{\text{WR1}}$	—	H	H	O	O	H	K
	$\overline{\text{WR0}}$	H	H	H	O	O	H	K
	BC3 to BC0	—			O	O	H	K
	$\overline{\text{SDCS1}}$, $\overline{\text{SDCS0}}$	—			O	O	H	K
	$\overline{\text{SDRAS}}$	—			O	O	H	K
	$\overline{\text{SDCAS}}$	—			O	O	H	K
	$\overline{\text{SDWE}}$	—			O	O	H	K
	DQM3 to DQM0	—			O	O	H	K
	SDCKE	—			O	O	K	K

[After change]

Pin Function		Pin State						
		Reset State				Power-Down State		
		Power-On						
		Area 0 Data Bus Width						
Type	Pin Name	8 Bits	16 Bits	32 Bits	Manual	Sleep	Software Standby	Deep Standby
Bus control	$\overline{\text{WAIT}}$	—			I	I	Z	Z
	$\overline{\text{CSO}}$	H			O	O	K	K
	$\overline{\text{CS6}}$ to $\overline{\text{CS1}}$	—			O	O	K	K
	$\overline{\text{RD}}$	H			O	O	K	K
	$\overline{\text{WR3}}$	—	—	H	O	O	K	K
	$\overline{\text{WR2}}$	—	—	H	O	O	K	K
	$\overline{\text{WR1}}$	—	H	H	O	O	K	K
	$\overline{\text{WR0}}$	H	H	H	O	O	K	K
	BC3 to BC0	—			O	O	K	K
	$\overline{\text{SDCS1}}$, $\overline{\text{SDCS0}}$	—			O	O	K	K
	$\overline{\text{SDRAS}}$	—			O	O	K	K
	$\overline{\text{SDCAS}}$	—			O	O	K	K
	$\overline{\text{SDWE}}$	—			O	O	K	K
	DQM3 to DQM0	—			O	O	K	K
	SDCKE	—			O	O	K	K