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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A0226A/E	Rev.	1.00
Title	Errata to User's Manual: Hardware Regarding the I^2C-bus Interface (RIIC)		Information Category	Technical Notification		
Applicable Product	RX630 Group, RX63N Group, RX631 Group, RX63T Group	Lot No. All	Reference Document	RX630 Group User's Manual: Hardware Rev.1.60 (R01UH0040EJ0160) RX63N Group, RX631 Group User's Manual: Hardware Rev.1.80 (R01UH0041EJ0180) RX63T Group User's Manual: Hardware Rev.2.20 (R01UH0238EJ0220)		

This document describes corrections to the "I^2C Bus Interface (RIIC)" chapter in User's Manual: Hardware for the applicable products.
Page and section numbers are based on those of the manual for the RX630 Group. Refer to the table on the last page for the corresponding page and section numbers in the other groups.

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The first paragraph of the description for the NACKE bit in section 33.2.6, I^2C Bus Function Enable Register (ICFER) is corrected as follows.

Before correction

This bit is used to specify whether to continue or discontinue the transfer operation when NACK is received from the slave device in transmit mode. Normally, set this bit to 1.

After correction

This bit is used to specify whether to continue or discontinue the data transfer when NACK is received in transmit mode. Normally, set this bit to 1.

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The second paragraph of the description for the AL flag in section 33.2.10, I^2C Bus Status Register 2 (ICSR2) is corrected as follows.

Before correction

The RIIC can also set the flag to indicate the detection of loss of arbitration during NACK transmission in master mode or during data transmission in slave mode.

After correction

The RIIC can also detect loss of arbitration during NACK transmission in receive mode or during data transmission in slave mode.

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The note for the TDRE flag in section 33.2.10, I²C Bus Status Register 2 (ICSR2) is corrected as follows.

Before correction

Note: When the NACKF flag is set to 1 while the NACKE bit in ICFER is 1, the RIIC suspends data transmission/ reception. Here, if the TDRE flag is 0 (next transmit data has been written), data is transferred to the ICDRS register and the ICDRT register becomes empty at the rising edge of the ninth clock cycle, but the TDRE flag is not set to 1.

After correction

Note: The NACKF flag becoming 1 while the ICFER.NACKE bit is 1 suspends data transmission and reception by the RIIC. Even if the next data for transmission has already been written to the ICDRT register (the TDRE flag is 0), the data in the ICDRT register is retained but not transferred to the ICDRS register. At this point, the TDRE flag does not become 1.

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The first paragraph of section 33.7.3, Device-ID Address Detection is corrected as follows.

Before correction

The RIIC module has a facility for detecting device-ID addresses conformant with the I²C bus specification (Rev. 03). When the RIIC receives 1111 100b as the first byte after a start condition or restart condition was issued with the DIDE bit in ICSER set to 1, the RIIC recognizes the address as a device ID, sets the DID flag in ICSR1 to 1 on the rising edge of the eighth SCL clock cycle when the following R/W# bit is 0, and then compares the second and subsequent bytes with its own slave address. If the address matches the value in the slave address register, the RIIC sets the corresponding AASy flag (y = 0 to 2) in ICSR1 to 1.

After correction

The RIIC module has a function to detect device-ID addresses complying with the I²C-bus specification. When the RIIC receives 1111 100b as the first seven bits of the first byte following a start condition or a restart condition while the ICSER.DIDE bit is set to 1, the RIIC recognizes the address as a device-ID address, sets the ICSR1.DID flag to 1 on the rising edge of the ninth SCL when the following R/W# bit is 0, and then compares the second and following bytes with its own slave address. If the received address matches the value in the slave address register, the RIIC sets the corresponding ICSR1.AASy flag (y = 0 to 2) to 1.

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Figure 33.28 in section 33.7.3, Device-ID Address Detection is corrected as follows.

Before correction

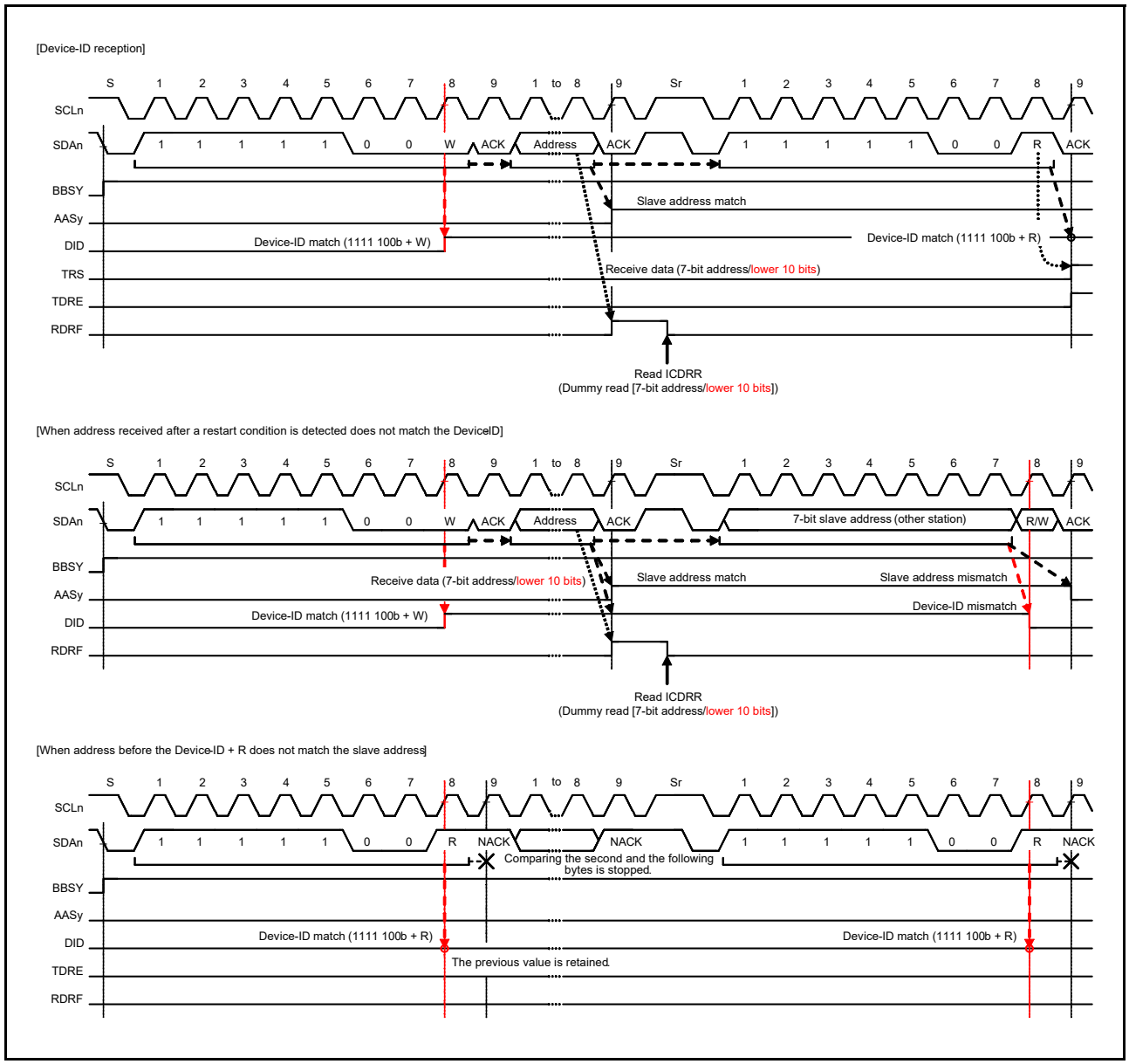
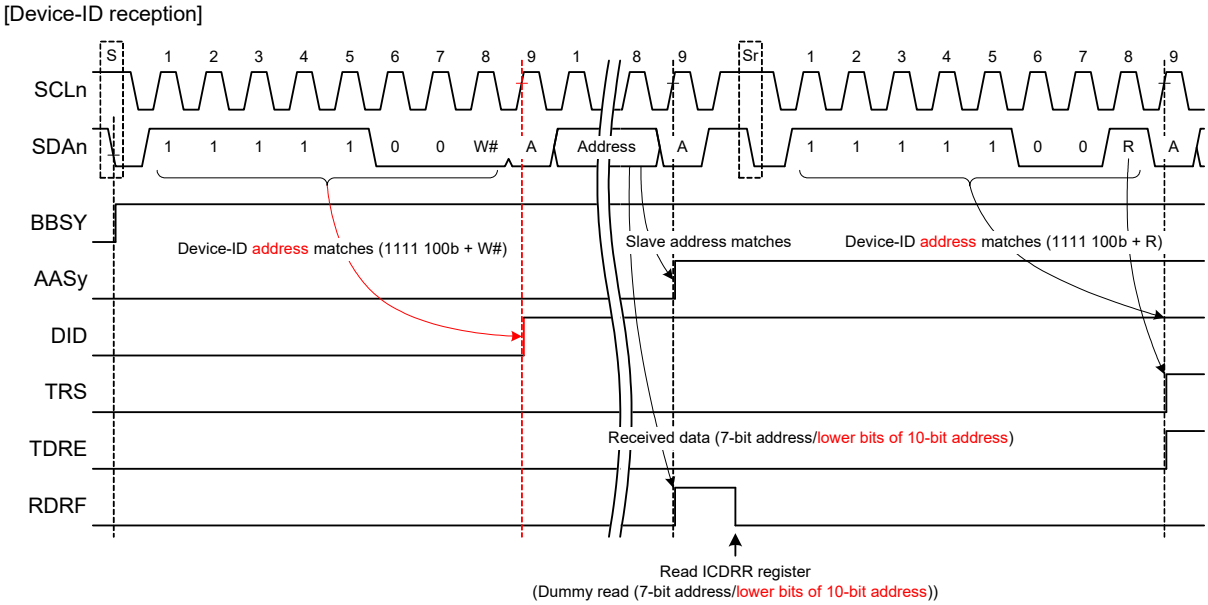
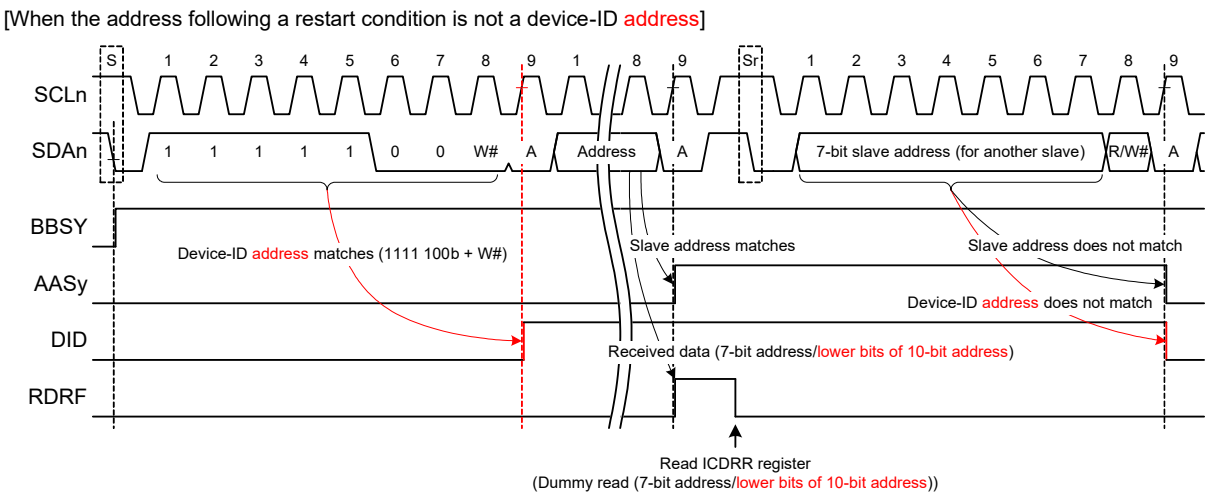


Figure 33.28 AASy/DID Flag Set/Clear Timing during Reception of Device-ID

After correction





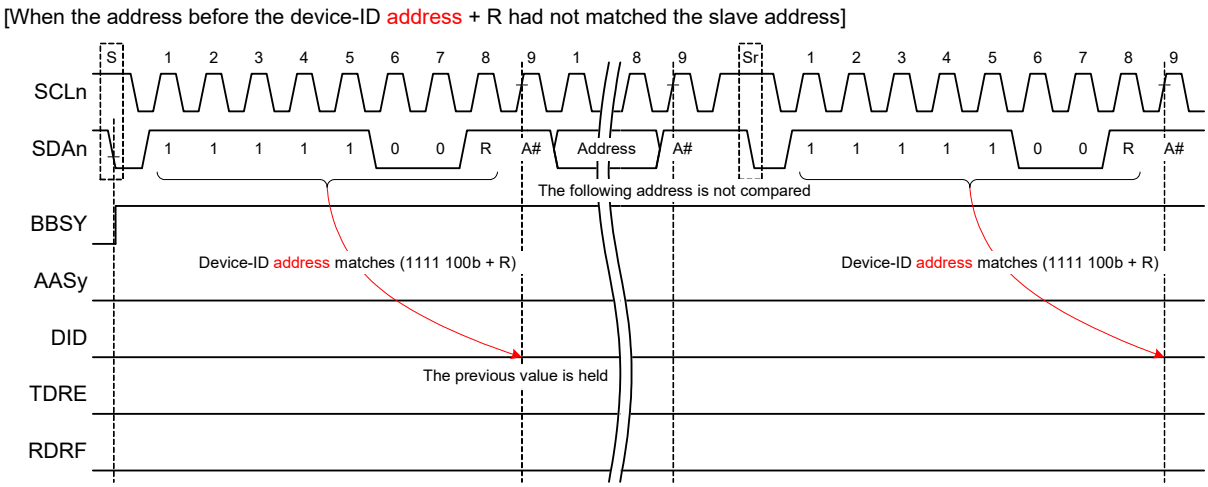


Figure 33.28 Set/Clear Timing of the AASy and DID Flags during Reception of Device-ID Address

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The second paragraph in section 33.8.2, NACK Reception Transfer Suspension Function is corrected as follows.

Before correction

If the transfer operation is suspended by this function (NACKF flag = 1 in ICSR2), transmit operation and receive operation are discontinued. To restore transmit/receive operation, be sure to clear the NACKF flag to 0. In master transmit mode, clear the NACKF flag to 0, issue a restart or stop condition, and then issue a start condition again.

After correction

If the data transmission is suspended (ICSR2.NACKF flag is 1) by this function, the following data transmission and data reception are not started. To resume data transfer, set the NACKF flag to 0. In master transmit mode, restart data transfer by setting the NACKF flag to 0 after generating a restart condition, or restart data transfer from a start condition after generating a stop condition then setting the NACKF flag to 0.

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Figure 33.31 in section 33.8.2, NACK Reception Transfer Suspension Function is corrected as follows.

Before correction

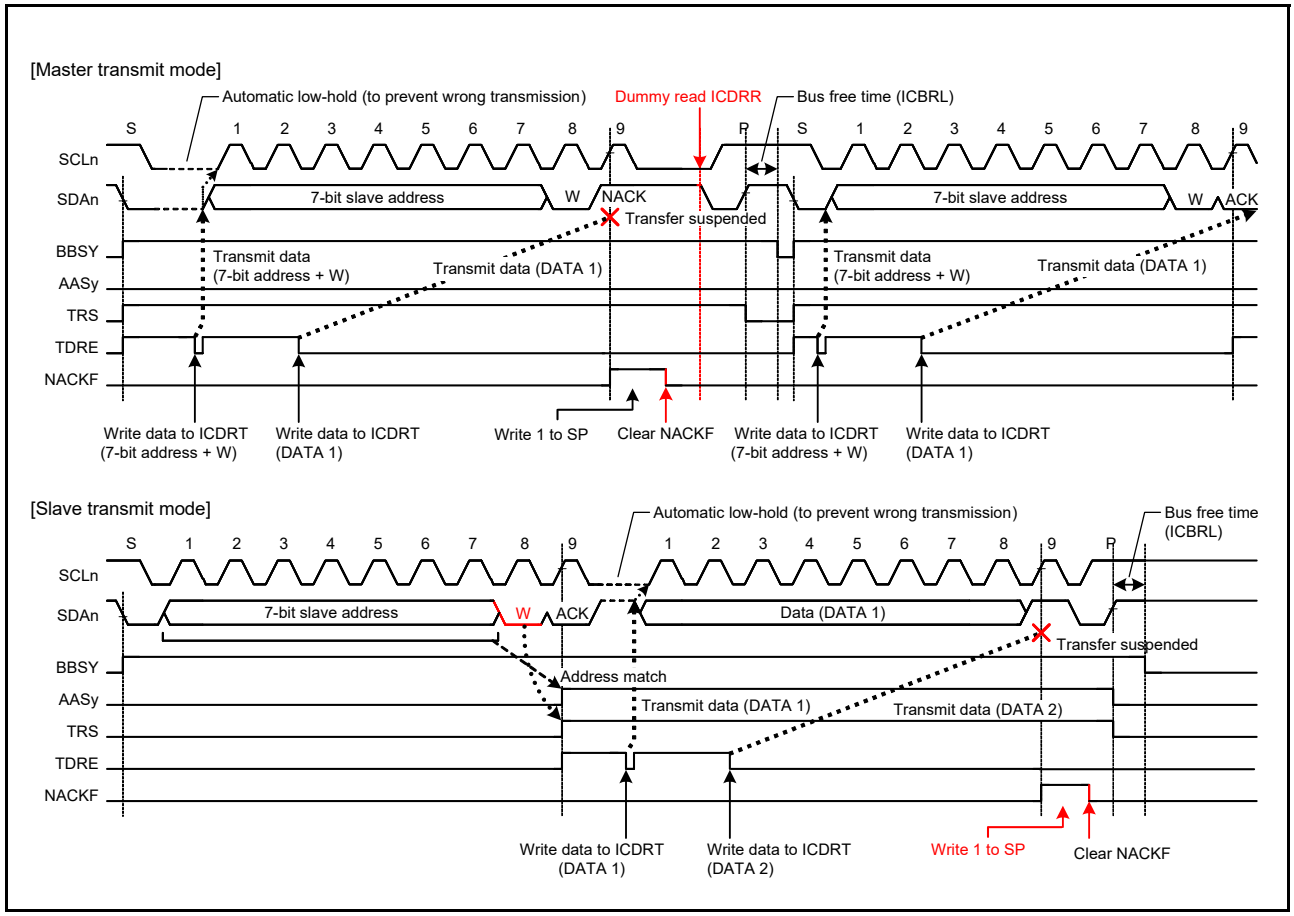

Figure 33.31 Suspension of Data Transfer when NACK is Received (NACKE = 1)

After correction

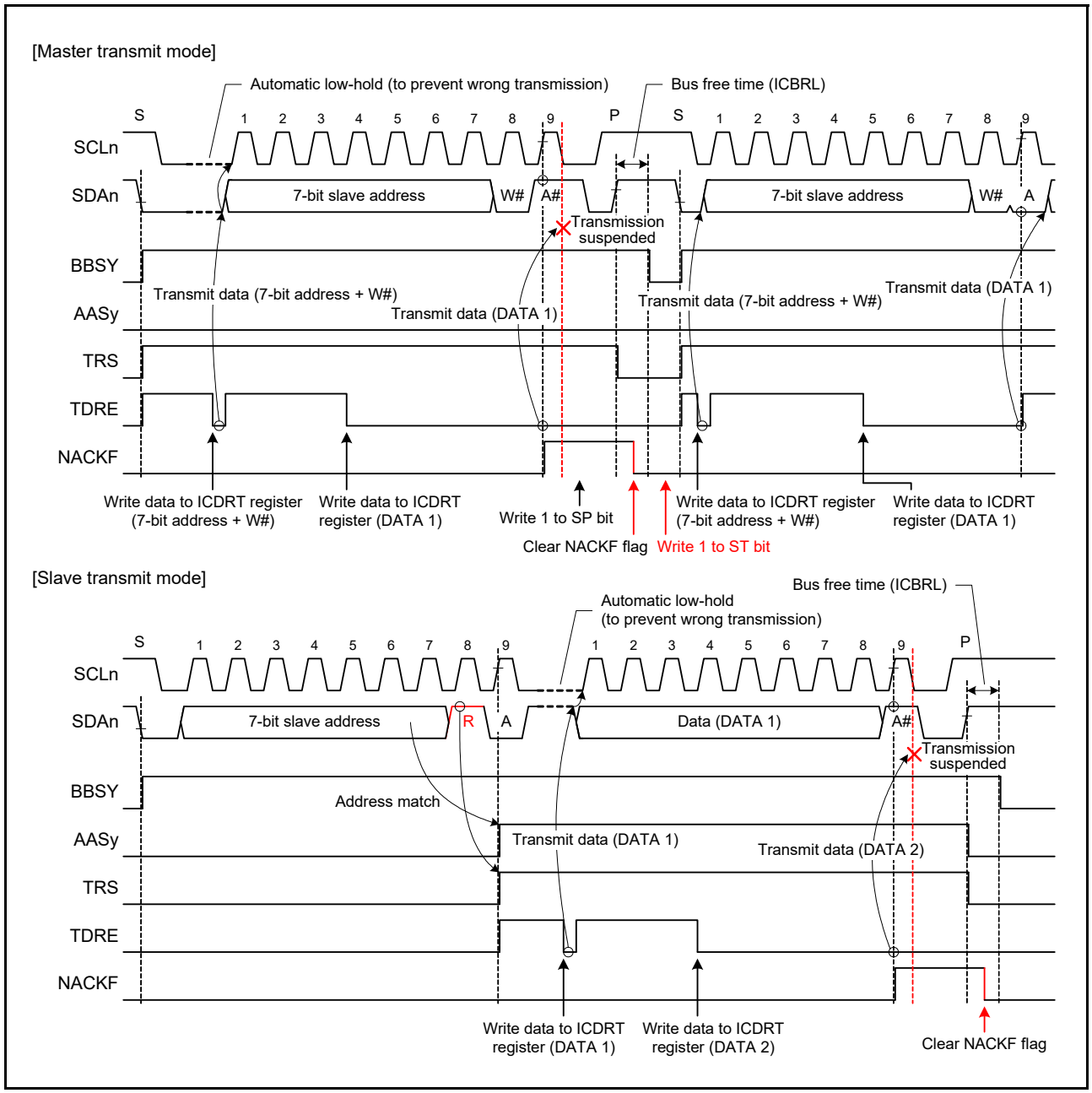

Figure 33.31 Suspension of Data Transmission When NACK is Received (NACKE = 1)

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The third paragraph in section 33.11.2, Extra SCL Clock Cycle Output Function is modified as follows.

Before correction

When the CLO bit in ICCR1 is set to 1 in master mode, a single cycle of the SCL clock at the frequency corresponding to the transfer rate settings (settings of the CKS[2:0] bits in ICMR1, and of the ICBRH and ICBRL registers) is output as an extra clock cycle. After output of this single cycle of the SCL clock, the CLO bit is automatically cleared to 0. Therefore, further extra clock cycles can be output consecutively by the software program writing 1 to the CLO bit after having read CLO = 0.

After correction

When the ICCR1.CLO bit is set to 1, an additional clock pulse at the frequency set by the ICMR1.CKS[2:0] bits and the ICBRH and ICBRL registers is output from the SCLn pin. After output of this clock pulse, the CLO bit automatically becomes 0. The SCLn pin is held low when the ICCR2.BBSY flag is 1 and held high when the BBSY flag is 0. Consecutive additional clock pulses can be output by writing 1 to the CLO bit after confirming the CLO bit to be 0.

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The second sentence in the fifth paragraph of section 33.11.2, Extra SCL Clock Cycle Output Function is deleted as follows.

Before correction

Use this facility with the MALE bit (master arbitration-lost detection disabled) in ICFER cleared to 0. If the MALE bit is set to 1 (master arbitration-lost detection enabled), arbitration is lost when the value of the SDAO bit in ICCR1 does not match the state of the SDAn line, so take care on this point.

After correction

Use this function with the ICFER.MALE bit set to 0 (master arbitration-lost detection is disabled).

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Figure 33.40 in section 33.11.2, Extra SCL Clock Cycle Output Function is corrected as follows.

Before correction

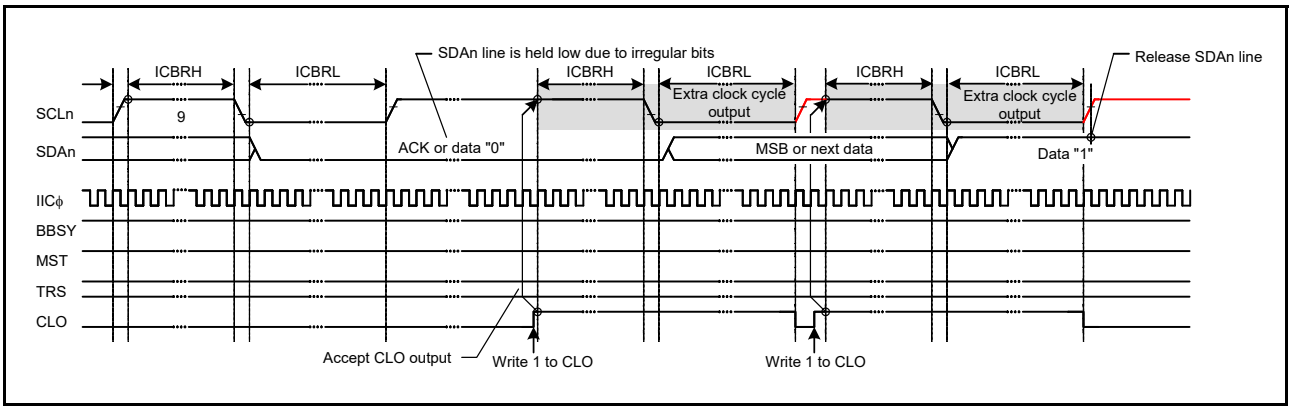

Figure 33.40 Extra SCL Clock Cycle Output Function (CLO Bit)

After correction

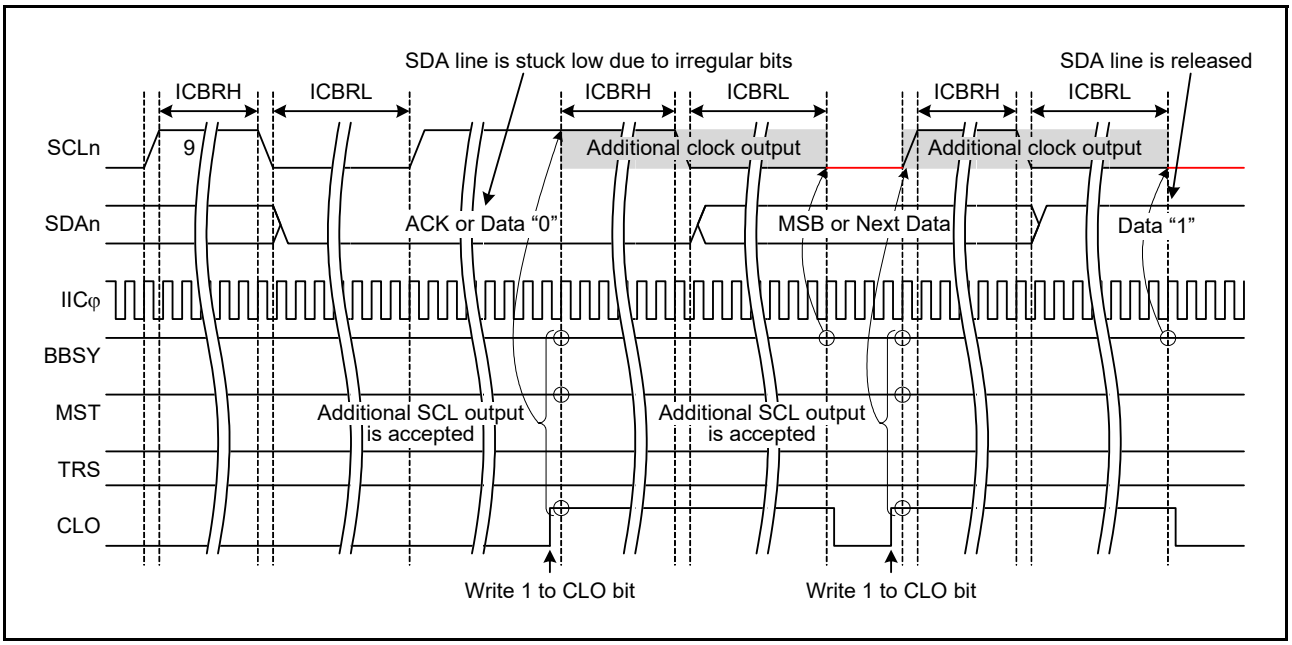

Figure 33.40 Additional SCL Output Function (CLO Bit)

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Table 33.8 in section 33.14, Reset States is corrected as follows.

Before correction

Table 33.8 Reset Conditions

		Chip Reset	RIIC Reset (ICE = 0, IICRST = 1)	Internal Reset (ICE = 1, IICRST = 1)	Start Condition/ Restart Condition Detection	Stop Condition Detection
ICCR1	ICE, IICRST	At a reset	Retained	Retained	Operation (retained)	Operation (retained)
	SCLO, SDAO		At a reset	At a reset		
	Others			Retained		
ICCR2	BBSY	At a reset	At a reset	Operation	Operation	Operation
	ST			At a reset	At a reset	Operation (retained)
	Others					At a reset
ICMR1	BC[2:0]	At a reset	At a reset	At a reset	At a reset	Operation (retained)
	Others			Retained	Operation (retained)	
ICMR2		At a reset	At a reset	Retained	Operation (retained)	Operation (retained)
ICMR3		At a reset	At a reset	Retained	Operation (retained)	Operation (retained)
ICFER		At a reset	At a reset	Retained	Operation (retained)	Operation (retained)
ICSER		At a reset	At a reset	Retained	Operation (retained)	Operation (retained)
ICIER		At a reset	At a reset	Retained	Operation (retained)	Operation (retained)
ICSR1		At a reset	At a reset	At a reset	Operation (retained)	At a reset
ICSR2	TDRE, TEND	At a reset	At a reset	At a reset	Operation (retained)	At a reset
	START				Operation	
	STOP				Operation (retained)	Operation
	Others					Operation (retained)
SARL0, 1, 2 SARU0, 1, 2		At a reset	At a reset	Retained	Operation (retained)	Operation (retained)
ICBRH, ICBRL		At a reset	At a reset	Retained	Operation (retained)	Operation (retained)
ICDRT		At a reset	At a reset	Retained	Operation (retained)	Operation (retained)
ICDRR		At a reset	At a reset	Retained	Operation (retained)	Operation (retained)
ICDRS		At a reset	At a reset	At a reset	Operation (retained)	Operation (retained)
Timeout function		At a reset	At a reset	Operation	Operation	Operation
Bus free time measurement		At a reset	At a reset	Operation	Operation	Operation

After correction

Table 33. Reset States of Registers and Functions When a Reset is Applied or a Condition is Detected

		MCU Reset	RIIC Reset (ICE = 0, IICRST = 1)	Internal Reset (ICE = 1, IICRST = 1)	Start Condition/ Restart Condition Detection	Stop Condition Detection
ICCR1	SDAO, SCLO	To be reset	To be reset	To be reset	Retained	Retained
	IICRST, ICE		Retained	Retained		
	Others		To be reset			
ICCR2	ST, RS	To be reset	To be reset	To be reset	To be reset	Retained
	SP					To be reset
	TRS				See note 1	
	MST				See note 1	
	BBSY			Retained	Becomes 1	
ICMR1	BC[2:0]	To be reset	To be reset	To be reset	To be reset	Retained
	Others			Retained	Retained	
ICMR2		To be reset	To be reset	Retained	Retained	Retained
ICMR3	ACKBT	To be reset	To be reset	Retained	Retained	To be reset
	Others					Retained
ICFER		To be reset	To be reset	Retained	Retained	Retained
ICSER		To be reset	To be reset	Retained	Retained	Retained
ICIER		To be reset	To be reset	Retained	Retained	Retained
ICSR1		To be reset	To be reset	To be reset	Retained	To be reset
ICSR2	START	To be reset	To be reset	To be reset	Becomes 1	To be reset
	STOP				Retained	Becomes 1
	TEND					To be reset
	TDRE				See note 1	
	Others				Retained	Retained
SARL0, SARL1, SARL2, SARU0, SARU1, SARU2		To be reset	To be reset	Retained	Retained	Retained
ICBRH, ICBRL		To be reset	To be reset	Retained	Retained	Retained
ICDRT		To be reset	To be reset	Retained	Retained	Retained
ICDRR		To be reset	To be reset	Retained	Retained	Retained
ICDRS		To be reset	To be reset	To be reset	Retained	Retained
Timeout function		To be reset	To be reset	To be reset	Operation	Operation
Bus free time measurement		To be reset	To be reset	Operation	Operation	Operation

Note 1. This bit is not reset. This bit becomes 0 or 1 in accordance with the conditions.

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Note for the ICSR2.TDRE flag	Page 1185 33.2.10	Page 1461 36.2.10	Page 1274 30.2.10
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