

# RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A0243A/E	Rev.	1.00
Title	Errata to the Section on Electrical Characteristics in the User's Manuals for the RX72M and RX72N Groups		Information Category	Technical Notification		
Applicable Product	RX72M Group, RX72N Group	Lot No.	Reference Document	RX72M Group User's Manual: Hardware Rev.1.00 (R01UH0804EJ0100) RX72N Group User's Manual: Hardware Rev.1.00 (R01UH0824EJ0100)		
		All				

This document describes corrections to the section on Electrical Characteristics in the User's Manual: Hardware, Rev.1.00 for the applicable products stated above. Page, table, and figure numbers are based on the manual for the RX72M Group. Refer to the table on the last page of this update for the corresponding page, table, and figure numbers in the manual for the RX72N Group.

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The frequency of ICLK described in Conditions of Table 65.26, Bus Timing is corrected as follows.

### Before correction

#### Table 65.26 Bus Timing

Conditions 1: VCC = AVCC0 = AVCC1 = VCC\_USB = V<sub>BATT</sub> = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,

VSS = AVSS0 = AVSS1 = VREFL0 = VSS\_USB = 0 V,

I<sub>CLK</sub> = PCLKA = 8 to 120 MHz, PCLKB = BCLK = SDCLK = 8 to 60 MHz, T<sub>a</sub> = T<sub>opr</sub>,

Output load conditions: V<sub>OH</sub> = VCC × 0.5, V<sub>OL</sub> = VCC × 0.5, C = 30 pF,

High-drive output is selected by the **driving ability** control register.

Conditions 2: VCC = AVCC0 = AVCC1 = VCC\_USB = V<sub>BATT</sub> = 3.0 to 3.6 V, 3.0 V ≤ VREFH0 ≤ AVCC0,

VSS = AVSS0 = AVSS1 = VREFL0 = VSS\_USB = 0 V,

I<sub>CLK</sub> = PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, 60 MHz < BCLK = SDCLK ≤ 80 MHz, T<sub>a</sub> = T<sub>opr</sub>,

Output load conditions: V<sub>OH</sub> = VCC × 0.5, V<sub>OL</sub> = VCC × 0.5,

C = 15 pF for the SDCLK pin, C = 30 pF for other pins.

To control the drive capacity when using the SDRAM: set the PFBCR3.SDCLKDRV bit in external bus control register 1 to 1 to select the drive capacity of the SDCLK pin, and set the SDRAM pins other than the SDCLK pin as high-speed-interface driving outputs.

### After correction

#### Table 61.26 Bus Timing

Conditions 1: VCC = AVCC0 = AVCC1 = VCC\_USB = V<sub>BATT</sub> = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,

VSS = AVSS0 = AVSS1 = VREFL0 = VSS\_USB = 0 V,

I<sub>CLK</sub> = 8 to 240 MHz, PCLKA = 8 to 120 MHz, PCLKB = BCLK = SDCLK = 8 to 60 MHz, T<sub>a</sub> = T<sub>opr</sub>,

Output load conditions: V<sub>OH</sub> = 0.5 × VCC, V<sub>OL</sub> = 0.5 × VCC, C = 30 pF,

High-drive output is selected by the **drive capacity** control register.

Conditions 2: VCC = AVCC0 = AVCC1 = VCC\_USB = V<sub>BATT</sub> = 3.0 to 3.6 V, 3.0 V ≤ VREFH0 ≤ AVCC0,

VSS = AVSS0 = AVSS1 = VREFL0 = VSS\_USB = 0 V,

I<sub>CLK</sub> = 60 to 240 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, 60 MHz < BCLK = SDCLK ≤ 80 MHz,

T<sub>a</sub> = T<sub>opr</sub>,

Output load conditions: V<sub>OH</sub> = 0.5 × VCC, V<sub>OL</sub> = 0.5 × VCC,

C = 15 pF for the SDCLK pin, C = 30 pF for other pins.

To control the drive capacity when using the SDRAM: set the PFBCR3.SDCLKDRV bit in external bus control register 1 to 1 to select the drive capacity of the SDCLK pin, and set the SDRAM pins other than the SDCLK pin as high-speed-interface driving outputs.

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The frequency of ICLK described in Conditions of Table 65.27, EXDMAC Timing is corrected as follows.

Before correction

**Table 65.27 EXDMAC Timing**

Conditions:  $VCC = AVCC0 = AVCC1 = VCC\_USB = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq$   $VREFH0 \leq AVCC0$ ,  
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS\_USB = 0$  V,  
**ICLK = 8 to 120 MHz**, PCLKA = 8 to 60 MHz, PCLKB = 8 to 60 MHz, BCLK = SDCLK = 8 to 80 MHz,  $T_a = T_{opr}$ ,  
 Output load conditions:  $V_{OH} = VCC \times 0.5$ ,  $V_{OL} = VCC \times 0.5$ ,  $C = 30$  pF,  
 High-drive output is selected by the **driving ability** control register.

After correction

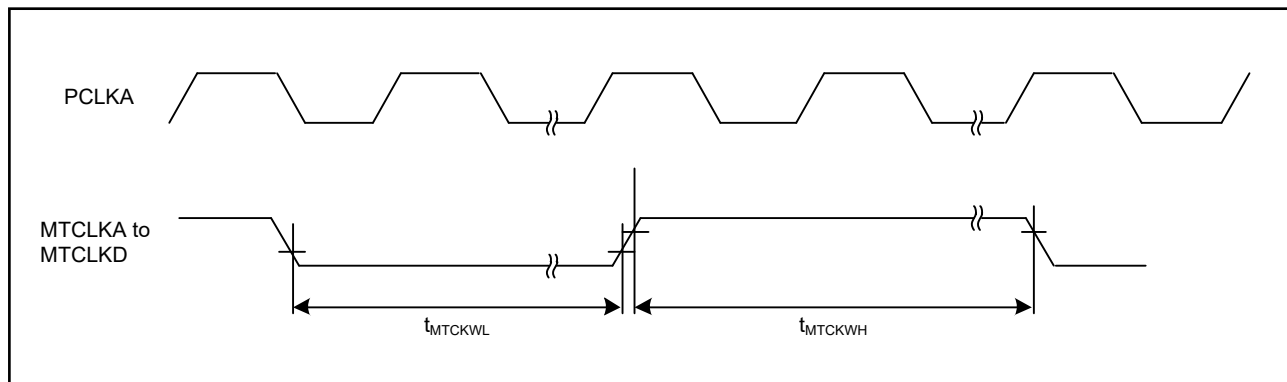
**Table 65.27 EXDMAC Timing**

Conditions:  $VCC = AVCC0 = AVCC1 = VCC\_USB = V_{BATT} = 2.7$  to  $3.6$  V,  $2.7$  V  $\leq$   $VREFH0 \leq AVCC0$ ,  
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS\_USB = 0$  V,  
**ICLK = 8 to 240 MHz**, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, BCLK = SDCLK = 8 to 80 MHz,  $T_a = T_{opr}$ ,  
 Output load conditions:  $V_{OH} = 0.5 \times VCC$ ,  $V_{OL} = 0.5 \times VCC$ ,  $C = 30$  pF,  
 High-drive output is selected by the **drive capacity** control register.

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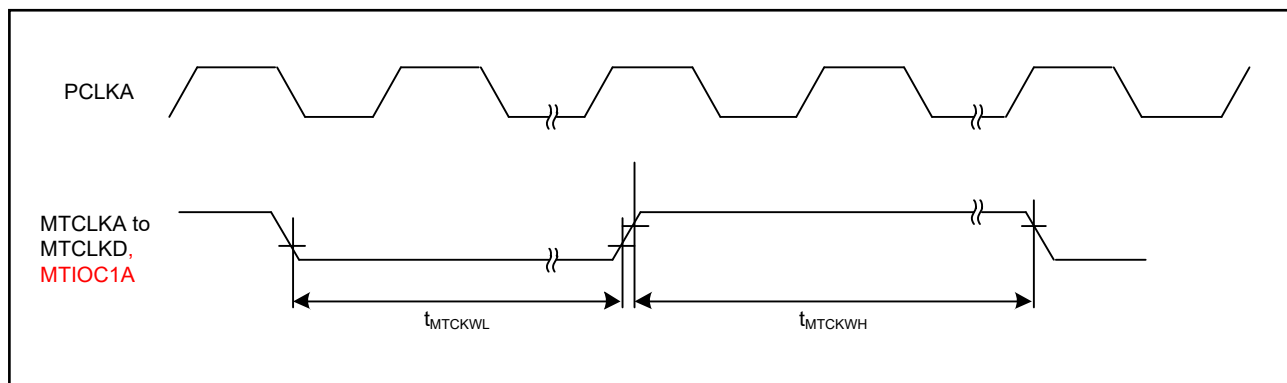
The MTIOC1A pin is added to Figure 65.41, MTU Clock Input Timing as follows.

Before correction



**Figure 65.41 MTU Clock Input Timing**

After correction

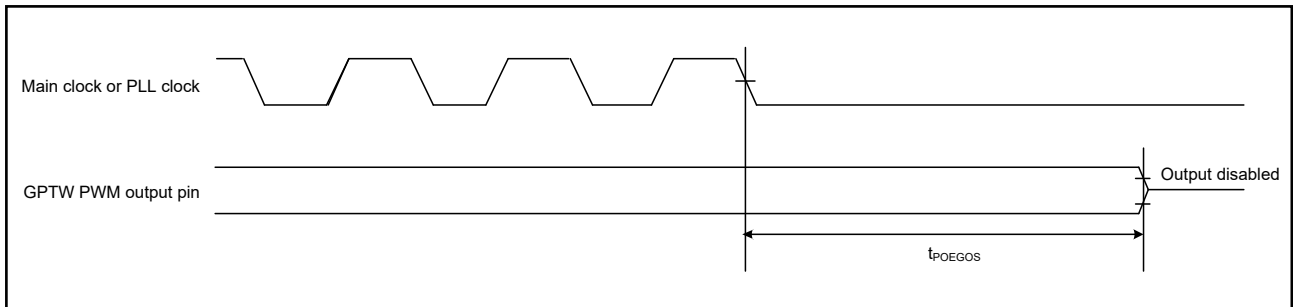


**Figure 65.41 MTU Clock Input Timing**

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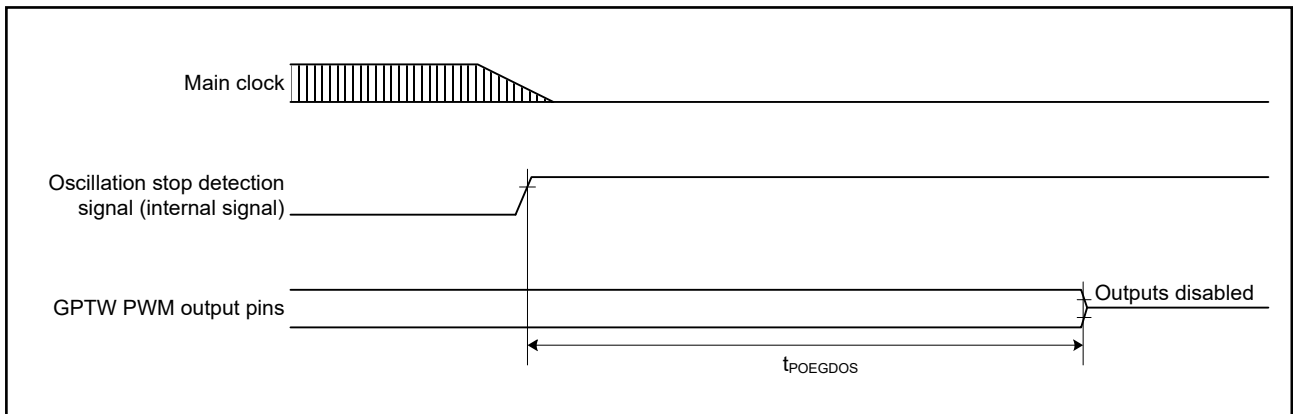
Figure 65.51, Output Disable Time of POEG in Response to the Oscillation Stop Detection is corrected as follows.

Before correction



**Figure 65.51 Output Disable Time of POEG in Response to the Oscillation Stop Detection**

After correction

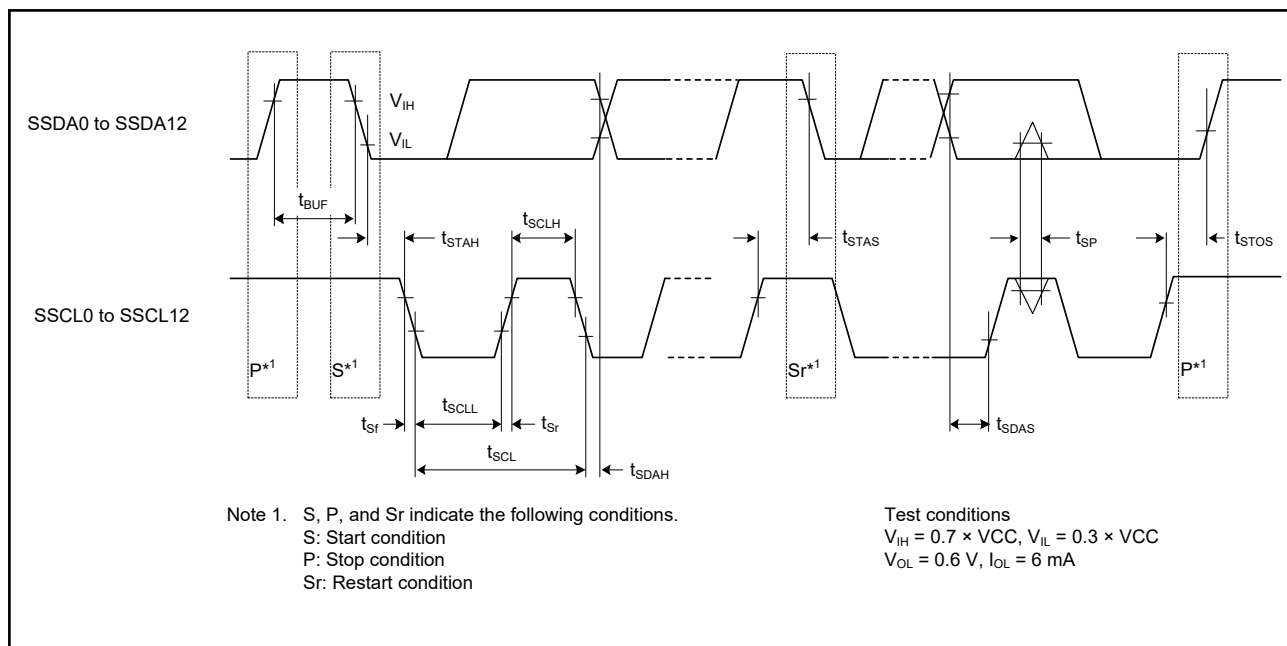


**Figure 65.51 Output Disable Time of POEG in Response to the Oscillation Stop Detection**

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The following figure is added to illustrate the input and output timing of the simple IIC bus interface.

After correction



**Figure 65.xx Simple IIC Bus Interface Input/Output Timing**

•Page, Table, and Figure Numbers

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Figure of Output Disable Time of POEG in Response to the Oscillation Stop Detection	Page 3264 of 3322 Figure 65.51	Page 3164 of 3222 Figure 63.51
Figure of RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing	Page 3280 of 3322 Figure 65.72	Page 3180 of 3222 Figure 63.72