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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A202A/E	Rev.	1.00
Title	Errata to RX65N Group, RX651 Group User's Manual: Hardware		Information Category	Technical Notification		
Applicable Product	RX65N Group, RX651 Group	Lot No. All	Reference Document	RX65N Group, RX651 Group User's Manual: Hardware Rev.2.10 (R01UH0590EJ0210)		

This document describes corrections to the RX65N Group, RX651 Group User's Manual: Hardware, Rev.2.10.

The corrections are indicated in red as shown below.

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The "Bit Name" column in Table 49.8, Boundary Scan Register (Products with at least 1.5 Mbytes of code flash memory) 145-Pin TFLGA is corrected as follows:

After correction

Table 49.8 Boundary Scan Register (Products with at Least 1.5 Mbytes of Code Flash Memory) 145-Pin TFLGA (1/8)

Pin No.	Pin Name	Input/Output	Bit Name
From TDI			
B3	P05	Output	333
		Output enable	332
		Input	331
D3	P03	Output	330
		Output enable	329
		Input	328
C2	P02	Output	327
		Output enable	326
		Input	325
D4	P01	Output	324
		Output enable	323
		Input	322
D1	P00	Output	321
		Output enable	320
		Input	319
D2	PF5	Output	318
		Output enable	317
		Input	316
E3	PJ5	Output	315
		Output enable	314
		Input	313
F3	PJ3	Output	312
		Output enable	311
		Input	310
G3	MD	Output	309
		Output enable	308
		Input	307
H4	P35	Input	303
J2	P33	Output	299
		Output enable	298
		Input	297
J3	P32	Output	296
		Output enable	295
		Input	294
L1	P25	Output	281
		Output enable	280
		Input	279
L4	P24	Output	278
		Output enable	277
		Input	276
L2	P23	Output	275
		Output enable	274
		Input	273

Table 49.8 Boundary Scan Register (Products with at Least 1.5 Mbytes of Code Flash Memory) 145-Pin TFLGA (2/8)

Pin No.	Pin Name	Input/Output	Bit Name
M1	P22	Output	272
		Output enable	271
		Input	270
N1	P21	Output	269
		Output enable	268
		Input	267
N2	P20	Output	266
		Output enable	265
		Input	264
M2	P17	Output	263
		Output enable	262
		Input	261
N3	P87	Output	260
		Output enable	259
		Input	258
L3	P16	Output	257
		Output enable	256
		Input	255
M3	P86	Output	254
		Output enable	253
		Input	252
K4	P15	Output	251
		Output enable	250
		Input	249
N4	P14	Output	248
		Output enable	247
		Input	246
L5	P13	Output	245
		Output enable	244
		Input	243
M4	P12	Output	242
		Output enable	241
		Input	240
L6	P56	Output	239
		Output enable	238
		Input	237
N7	P55	Output	236
		Output enable	235
		Input	234
K5	P54	Output	233
		Output enable	232
		Input	231

Table 49.8 Boundary Scan Register (Products with at Least 1.5 Mbytes of Code Flash Memory) 145-Pin TFLGA (3/8)

Pin No.	Pin Name	Input/Output	Bit Name
K6	P53	Output	230
		Output enable	229
		Input	228
L7	P52	Output	227
		Output enable	226
		Input	225
K7	P51	Output	224
		Output enable	223
		Input	222
M7	P50	Output	221
		Output enable	220
		Input	219
L8	P83	Output	218
		Output enable	217
		Input	216
N9	PC7	Output	215
		Output enable	214
		Input	213
M8	PC6	Output	212
		Output enable	211
		Input	210
L9	PC5	Output	209
		Output enable	208
		Input	207
N10	P82	Output	206
		Output enable	205
		Input	204
M9	P81	Output	203
		Output enable	202
		Input	201
K9	P80	Output	200
		Output enable	199
		Input	198
L10	PC4	Output	197
		Output enable	196
		Input	195
N11	PC3	Output	194
		Output enable	193
		Input	192
M10	P77	Output	191
		Output enable	190
		Input	189

Table 49.8 Boundary Scan Register (Products with at Least 1.5 Mbytes of Code Flash Memory) 145-Pin TFLGA (4/8)

Pin No.	Pin Name	Input/Output	Bit Name
K10	P76	Output	188
		Output enable	187
		Input	186
L11	PC2	Output	185
		Output enable	184
		Input	183
N12	P75	Output	182
		Output enable	181
		Input	180
N13	P74	Output	179
		Output enable	178
		Input	177
M12	PC1	Output	176
		Output enable	175
		Input	174
M11	PC0	Output	173
		Output enable	172
		Input	171
L12	P73	Output	170
		Output enable	169
		Input	168
K11	PB7	Output	167
		Output enable	166
		Input	165
K12	PB6	Output	164
		Output enable	163
		Input	162
K13	PB5	Output	161
		Output enable	160
		Input	159
J11	PB4	Output	158
		Output enable	157
		Input	156
J10	PB3	Output	155
		Output enable	154
		Input	153
J12	PB2	Output	152
		Output enable	151
		Input	150
J13	PB1	Output	149
		Output enable	148
		Input	147

Table 49.8 Boundary Scan Register (Products with at Least 1.5 Mbytes of Code Flash Memory) 145-Pin TFLGA (5/8)

Pin No.	Pin Name	Input/Output	Bit Name
H10	P72	Output	146
		Output enable	145
		Input	144
H11	P71	Output	143
		Output enable	142
		Input	141
H12	PB0	Output	140
		Output enable	139
		Input	138
H13	PA7	Output	137
		Output enable	136
		Input	135
G11	PA6	Output	134
		Output enable	133
		Input	132
G10	PA5	Output	131
		Output enable	130
		Input	129
G13	PA4	Output	128
		Output enable	127
		Input	126
F10	PA3	Output	125
		Output enable	124
		Input	123
F13	PA2	Output	122
		Output enable	121
		Input	120
F12	PA1	Output	119
		Output enable	118
		Input	117
E10	PA0	Output	116
		Output enable	115
		Input	114
E13	P67	Output	113
		Output enable	112
		Input	111
E11	P66	Output	110
		Output enable	109
		Input	108
E12	P65	Output	107
		Output enable	106
		Input	105

Table 49.8 Boundary Scan Register (Products with at Least 1.5 Mbytes of Code Flash Memory) 145-Pin TFLGA (6/8)

Pin No.	Pin Name	Input/Output	Bit Name
D10	PE7	Output	104
		Output enable	103
		Input	102
D13	PE6	Output	101
		Output enable	100
		Input	99
C12	P70	Output	98
		Output enable	97
		Input	96
D12	PE5	Output	95
		Output enable	94
		Input	93
B13	PE4	Output	92
		Output enable	91
		Input	90
A13	PE3	Output	89
		Output enable	88
		Input	87
B12	PE2	Output	86
		Output enable	85
		Input	84
A12	PE1	Output	83
		Output enable	82
		Input	81
C11	PE0	Output	80
		Output enable	79
		Input	78
D9	P64	Output	77
		Output enable	76
		Input	75
C10	P63	Output	74
		Output enable	73
		Input	72
A11	P62	Output	71
		Output enable	70
		Input	69
B11	P61	Output	68
		Output enable	67
		Input	66
D8	P60	Output	65
		Output enable	64
		Input	63

Table 49.8 Boundary Scan Register (Products with at Least 1.5 Mbytes of Code Flash Memory) 145-Pin TFLGA (7/8)

Pin No.	Pin Name	Input/Output	Bit Name
C9	PD7	Output	62
		Output enable	61
		Input	60
A9	PD6	Output	59
		Output enable	58
		Input	57
D7	PD5	Output	56
		Output enable	55
		Input	54
B9	PD4	Output	53
		Output enable	52
		Input	51
C8	PD3	Output	50
		Output enable	49
		Input	48
A8	PD2	Output	47
		Output enable	46
		Input	45
C7	PD1	Output	44
		Output enable	43
		Input	42
B8	PD0	Output	41
		Output enable	40
		Input	39
D6	P93	Output	38
		Output enable	37
		Input	36
A7	P92	Output	35
		Output enable	34
		Input	33
B7	P91	Output	32
		Output enable	31
		Input	30
A6	P90	Output	29
		Output enable	28
		Input	27
B6	P47	Output	26
		Output enable	25
		Input	24
C5	P46	Output	23
		Output enable	22
		Input	21

Table 49.8 Boundary Scan Register (Products with at Least 1.5 Mbytes of Code Flash Memory) 145-Pin TFLGA (8/8)

Pin No.	Pin Name	Input/Output	Bit Name
A5	P45	Output	20
		Output enable	19
		Input	18
E5	P44	Output	17
		Output enable	16
		Input	15
B5	P43	Output	14
		Output enable	13
		Input	12
A4	P42	Output	11
		Output enable	10
		Input	9
C4	P41	Output	8
		Output enable	7
		Input	6
A3	P40	Output	5
		Output enable	4
		Input	3
A2	P07	Output	2
		Output enable	1
		Input	0
To TDO			

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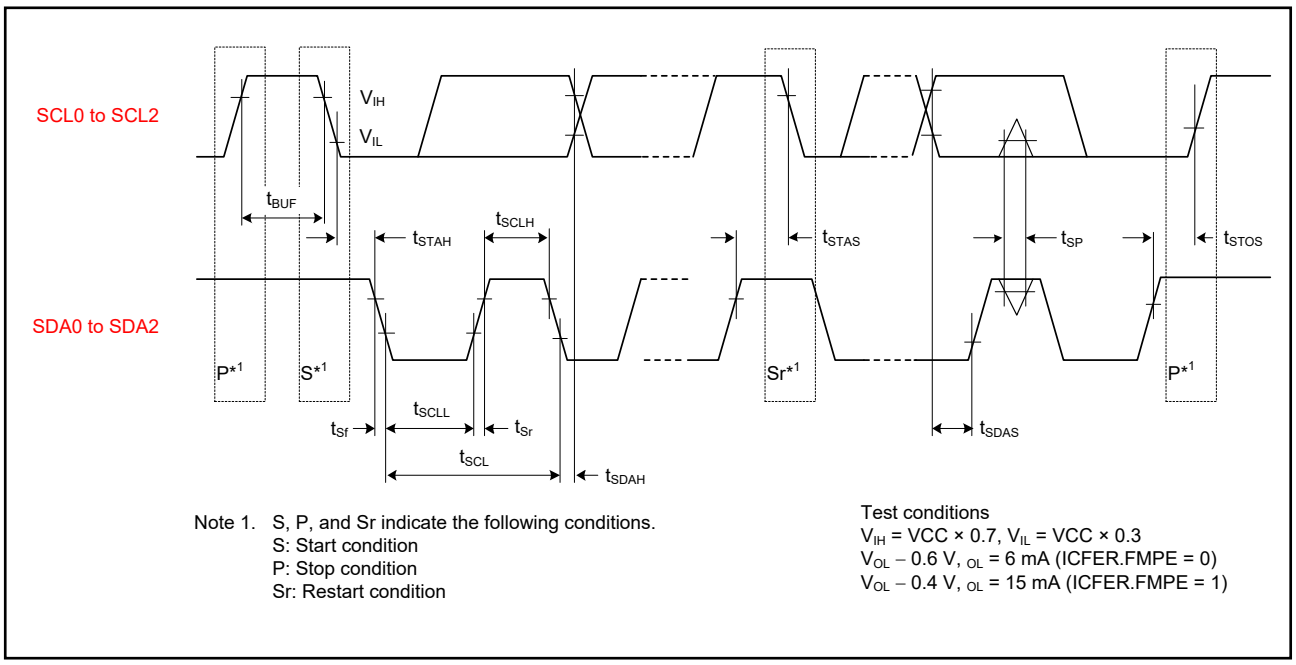
The signal names in Figure 60.54, RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing are corrected as follows:

Before correction

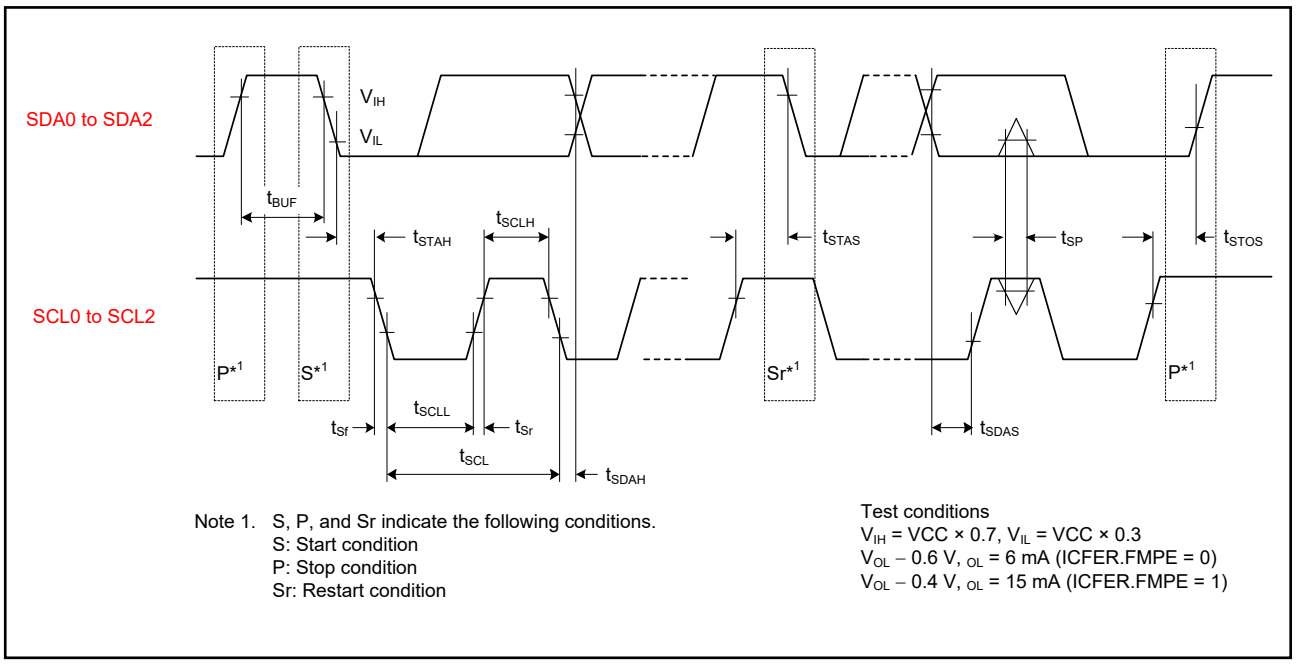


Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} – 0.6 V, $_{OL}$ = 6 mA (ICFER.FMPE = 0)
V_{OL} – 0.4 V, $_{OL}$ = 15 mA (ICFER.FMPE = 1)

Figure 60.54 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

After correction



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
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V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} – 0.6 V, $_{OL}$ = 6 mA (ICFER.FMPE = 0)
V_{OL} – 0.4 V, $_{OL}$ = 15 mA (ICFER.FMPE = 1)

Figure 60.54 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing