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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A182A/E	Rev.	1.00
Title	Errata to RX65N Group, RX651 Group User's Manual: Hardware		Information Category	Technical Notification		
Applicable Product	RX65N Group, RX651 Group	Lot No. All	Reference Document	RX65N Group, RX651 Group User's Manual: Hardware Rev.2.10 (R01UH0590EJ0210)		

This document describes corrections, as shown below, to the RX65N Group, RX651 Group User's Manual: Hardware, Rev.2.10.

No.	Section Number	Summary
1	1. Overview	Addition of description of function and error correction in Table 1.5 and Table 1.6.
2	22. I/O Ports	Description of Port functions in Table 22.3 is corrected.
3	60. Electrical Characteristics	The title of Table 60.9 is modified.
4		The value of 12-bit A/D conversion time in Table 60.46 is corrected.

The corrections are indicated in red.

No.1. 1.5 Pin Assignments

- Addition of description of function and error correction in Table 1.5 as follows.

Before correction

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-pin LFBGA)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	**Power Supply Clock System Control**	**I/O Port**	**Bus EXDMAC SDRAMC**	**Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)**	**Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)**	**Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)**	**GLCDC**	**Interrupt**	**A/D D/A**
					Omitted				
M8		P55	D0[A0/D0]/ EDREQ0	MTIOC4D/ TMO3	ET0_EXOUT/ TXD7/SMOSI7/ SSDA7/MISOC-B/CRX1		LCD_DATA5-A	IRQ10	
					Omitted				
N8		P54	D1[A1/D1]/ EDACK0	MTIOC4B/ TMCI1	ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/MOSIC-B/ CTX1		LCD_DATA6-A		
					Omitted				
P5	VSS_USB								
P6	VCC_USB								
					Omitted				

After correction

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-pin LFBGA)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
					Omitted				
M8		P55	D0[A0/D0]/ EDREQ0/ WAIT#	MTIOC4D/ TMO3	ET0_EXOUT/ TXD7/SMOSI7/ SSDA7/MISOC-B/CRX1		LCD_DATA5-A	IRQ10	
					Omitted				
N8		P54	D1[A1/D1]/ EDACK0/ ALE	MTIOC4B/ TMCI1	ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/MOSIC-B/ CTX1		LCD_DATA6-A		
					Omitted				
P5	VCC_USB								
P6	VSS_USB								
					Omitted				

- Addition of description of function in Table 1.6 as follows.

Before correction

Table 1.6 List of Pin and Pin Functions (176-pin LFQFP)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
Omitted									
65		P55	D0[A0/D0]/ EDREQ0	MTIOC4D/ TMO3	ET0_EXOUT/ TXD7/SMOSI7/ SSDA7/MISOC-B/CRX1		LCD_DATA5-A	IRQ10	
66		P54	D1[A1/D1]/ EDACK0	MTIOC4B/ TMCI1	ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/MOSIC-B/ CTX1		LCD_DATA6-A		
Omitted									

After correction

Table 1.6 List of Pin and Pin Functions (176-pin LFQFP)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, CAN, USB)	Memory Interface Camera Interface (QSPI, SDHI, SDSI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A
Omitted									
65		P55	D0[A0/D0]/ EDREQ0/ WAIT#	MTIOC4D/ TMO3	ET0_EXOUT/ TXD7/SMOSI7/ SSDA7/MISOC-B/CRX1		LCD_DATA5-A	IRQ10	
66		P54	D1[A1/D1]/ EDACK0/ ALE	MTIOC4B/ TMCI1	ET0_LINKSTA/ CTS2#/RTS2#/ SS2#/MOSIC-B/ CTX1		LCD_DATA6-A		
Omitted									

No.2. 22. I/O Ports

Description of Port functions in Table 22.3 is corrected as follows.

Before correction

Table 22.3 Port Functions (Products with at least 1.5 Mbytes of code flash memory)

Port	Pin	Input Pull-up	Open-Drain Output	Driving Ability Switching	5-V Tolerant
Omitted					
PORT8	P80 to P85	✓	✓	High drive / high-speed interface high-drive	—
	P86	✓	✓	Fixed to high driving ability output	—
	P87	✓	✓	High drive / high-speed interface high-drive	—
Omitted					

After correction

Table 22.3 Port Functions (Products with at least 1.5 Mbytes of code flash memory)

Port	Pin	Input Pull-up	Open-Drain Output	Driving Ability Switching	5-V Tolerant
Omitted					
PORT8	P80 to P85	✓	✓	Normal drive / high drive / high-speed interface high-drive	—
	P86	✓	✓	Fixed to high driving ability output	—
	P87	✓	✓	High drive / high-speed interface high-drive	—
Omitted					

No.3. 60.2 DC Characteristics

The title of Table 60.9 is modified as follows.

Before correction

Table 60.9 Heat Resistance Value (Reference)

Item	Package	Symbol	Max.	Unit	Test Conditions
Heat resistance	176-pin LFQFP (PLQP0176KB-A)	θja	48.0	°C/W	JESD51-2 and JESD51-7 compliant
	144-pin LFQFP (PLQP0144KA-B)		50.9		
	100-pin LFQFP (PLQP0100KB-B)		52.5		
	177-pin TFLGA (PTLG0177KA-A)		36.3		JESD51-2 and JESD51-9 compliant
	176-pin LFBGA (PLBG0176GA-A)		35.4		
	145-pin TFLGA (PTLG0145KA-A)		34.6		
	100-pin TFLGA (PTLG0100JA-A)		34.1		
	176-pin LFQFP (PLQP0176KB-A)	Ψjt	1.0	°C/W	JESD51-2 and JESD51-7 compliant
	144-pin LFQFP (PLQP0144KA-B)		1.5		
	100-pin LFQFP (PLQP0100KB-B)		1.5		
	177-pin TFLGA (PTLG0177KA-A)		0.3		JESD51-2 and JESD51-9 compliant
	176-pin LFBGA (PLBG0176GA-A)		0.3		
	145-pin TFLGA (PTLG0145KA-A)		0.4		
	100-pin TFLGA (PTLG0100JA-A)		0.4		

After correction

Table 60.9 Thermal Resistance Value (Reference)

Item	Package	Symbol	Max.	Unit	Test Conditions
Thermal resistance	176-pin LFQFP (PLQP0176KB-A)	θja	48.0	°C/W	JESD51-2 and JESD51-7 compliant
	144-pin LFQFP (PLQP0144KA-B)		50.9		
	100-pin LFQFP (PLQP0100KB-B)		52.5		
	177-pin TFLGA (PTLG0177KA-A)		36.3		JESD51-2 and JESD51-9 compliant
	176-pin LFBGA (PLBG0176GA-A)		35.4		
	145-pin TFLGA (PTLG0145KA-A)		34.6		
	100-pin TFLGA (PTLG0100JA-A)		34.1		
	176-pin LFQFP (PLQP0176KB-A)	Ψjt	1.0	°C/W	JESD51-2 and JESD51-7 compliant
	144-pin LFQFP (PLQP0144KA-B)		1.5		
	100-pin LFQFP (PLQP0100KB-B)		1.5		
	177-pin TFLGA (PTLG0177KA-A)		0.3		JESD51-2 and JESD51-9 compliant
	176-pin LFBGA (PLBG0176GA-A)		0.3		
	145-pin TFLGA (PTLG0145KA-A)		0.4		
	100-pin TFLGA (PTLG0100JA-A)		0.4		

No.4. 60.5 A/D Conversion Characteristics

The value of 12-bit A/D conversion time in Table 60.46 is corrected as follows.

Before correction

Table 60.46 12-Bit A/D (Unit 0) Conversion Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VBATT = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = PCLKC = 1 MHz to 60 MHz, Ta = Topr

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		8	—	12	Bit	
Analog input capacitance		—	—	30	pF	
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time*1 (Operation at PCLK = 60 MHz) Permissible signal source impedance (max.) = 1.0 kΩ	1.6 (0.4 + 0.25) *2	—	—	µs	· Sampling of channel-dedicated sample-and-hold circuits in 24 states · Sampling in 15 states
Omitted						

After correction

Table 60.46 12-Bit A/D (Unit 0) Conversion Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VBATT = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = PCLKC = 1 MHz to 60 MHz, Ta = Topr

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		8	—	12	Bit	
Analog input capacitance		—	—	30	pF	
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time*1 (Operation at PCLK = 60 MHz) Permissible signal source impedance (max.) = 1.0 kΩ	1.06 (0.4 + 0.25) *2	—	—	µs	· Sampling of channel-dedicated sample-and-hold circuits in 24 states · Sampling in 15 states
Omitted						

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