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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A0211A/E	Rev.	1.00
Title	Errata to RX65N Group, RX651 Group User's Manual: Hardware		Information Category	Technical Notification		
Applicable Product	RX65N Group, RX651 Group	Lot No. All	Reference Document	RX65N Group, RX651 Group User's Manual: Hardware Rev.2.10 (R01UH0590EJ0210)		

This document describes corrections, as shown below, to the RX65N Group, RX651 Group User's Manual: Hardware, Rev.2.10.

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Description of pin name in Table 1.4 is corrected as follows.

Before correction

Table 1.4 Pin Functions (6/8)

Classifications	Pin Name	I/O	Description
	--- omitted ---		
SD host interface	SDHI_CLK-A/SDHI_CLK-B/ SDHI_CLK-C	Output	SD clock output pin
	SDHI_CMD-A/SDHI_CMD-B/ SDHI_CMD-C	I/O	SD command output, response input signal pin
	SDHI_D3-A/SDHI_D3-B/ SDHI_D3-C to SDHI_D0-A/ SDHI_D0-B/SDHI_D1-C	I/O	SD data bus pins
	SDHI_CD	Input	SD card detection pin
	SDHI_WP	Input	SD write-protect signal
	--- omitted ---		

After correction

Table 1.4 Pin Functions (6/8)

Classifications	Pin Name	I/O	Description
	--- omitted ---		
SD host interface	SDHI_CLK-A/SDHI_CLK-B/ SDHI_CLK-C	Output	SD clock output pin
	SDHI_CMD-A/SDHI_CMD-B/ SDHI_CMD-C	I/O	SD command output, response input signal pin
	SDHI_D3-A/SDHI_D3-B/ SDHI_D3-C to SDHI_D0-A/ SDHI_D0-B/SDHI_D0-C	I/O	SD data bus pins
	SDHI_CD	Input	SD card detection pin
	SDHI_WP	Input	SD write-protect signal
	--- omitted ---		

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Description of Number of Bits and Access Size in Table 5.1 is corrected as follows.

Before correction

Table 5.1 List of I/O Registers (Address Order)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Reference Page
						ICLK≥PCLK	ICLK<PCLK		
--- omitted ---									
0009 0856h	CAN0	Acceptance Filter Support Register	AFSR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN	1863
--- omitted ---									
0009 1856h	CAN1	Acceptance Filter Support Register	AFSR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN	1863
--- omitted ---									
0009 5800h to 0009 58FFh	SDSI	FN1 Data Register 10 to 163	FN1DATAR10 to 163	8, 32	32	10, 11 PCLKB	2 to 6 ICLK	SDSI	2105
0009 5900h to 0009 59FFh	SDSI	FN1 Data Register 20 to 263	FN1DATAR20 to 263	8, 32	32	10, 11 PCLKB	2 to 6 ICLK	SDSI	2105
0009 5A00h to 0009 5AFFh	SDSI	FN1 Data Register 30 to 363	FN1DATAR30 to 363	8, 32	32	10, 11 PCLKB	2 to 6 ICLK	SDSI	2106
--- omitted ---									
0009 5C00h to 0009 5FFFh	SDSI	FN1 Data Register 50 to 5255	FN1DATAR50 to 5255	8, 32	32	7, 8 PCLKB	2 to 5 ICLK	SDSI	2107
--- omitted ---									

After correction

Table 5.1 List of I/O Registers (Address Order)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Reference Page
						ICLK≥PCLK	ICLK<PCLK		
--- omitted ---									
0009 0856h	CAN0	Acceptance Filter Support Register	AFSR	16	16	2, 3 PCLKB	2 ICLK	CAN	1863
--- omitted ---									
0009 1856h	CAN1	Acceptance Filter Support Register	AFSR	16	16	2, 3 PCLKB	2 ICLK	CAN	1863
--- omitted ---									
0009 5800h to 0009 58FFh	SDSI	FN1 Data Register 10 to 163	FN1DATAR10 to 163	32	8, 32	10, 11 PCLKB	2 to 6 ICLK	SDSI	2105
0009 5900h to 0009 59FFh	SDSI	FN1 Data Register 20 to 263	FN1DATAR20 to 263	32	8, 32	10, 11 PCLKB	2 to 6 ICLK	SDSI	2105
0009 5A00h to 0009 5AFFh	SDSI	FN1 Data Register 30 to 363	FN1DATAR30 to 363	32	8, 32	10, 11 PCLKB	2 to 6 ICLK	SDSI	2106
--- omitted ---									
0009 5C00h to 0009 5FFFh	SDSI	FN1 Data Register 50 to 5255	FN1DATAR50 to 5255	32	8, 32	7, 8 PCLKB	2 to 5 ICLK	SDSI	2107
--- omitted ---									

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Description of Step in Table 8.7 is corrected as follows.

Before correction

Table 8.7 Procedures for Setting Bits Related to the Voltage Monitoring 2 Interrupt and Voltage Monitoring 2 Reset so that Voltage Monitoring Stops

Step		Voltage Monitoring 2 Interrupt (Voltage Monitoring 2 ELC Event Output), Voltage Monitoring 2 Reset
Settings to stop enabling of output	1	Set LVD2CR0.LVD2CMPE = 0 (disabling output of the results of comparison by voltage monitoring 2).
	2	Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). *1
	3	Set LVD2CR0.LVD2RIE = 0 (disabling the voltage monitoring 2 interrupt or reset). *2
Stopping the digital filter	4	Set LVD2CR0.LVD2DFDIS = 1 (disabling the digital filter). *1, *3
Stopping the voltage detection 1 circuit	5	Set LVCMPCR.LVD2E = 0 (disabling the voltage detection 2 circuit).

After correction

Table 8.7 Procedures for Setting Bits Related to the Voltage Monitoring 2 Interrupt and Voltage Monitoring 2 Reset so that Voltage Monitoring Stops

Step		Voltage Monitoring 2 Interrupt (Voltage Monitoring 2 ELC Event Output), Voltage Monitoring 2 Reset
Settings to stop enabling of output	1	Set LVD2CR0.LVD2CMPE = 0 (disabling output of the results of comparison by voltage monitoring 2).
	2	Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n). *1
	3	Set LVD2CR0.LVD2RIE = 0 (disabling the voltage monitoring 2 interrupt or reset). *2
Stopping the digital filter	4	Set LVD2CR0.LVD2DFDIS = 1 (disabling the digital filter). *1, *3
Stopping the voltage detection 2 circuit	5	Set LVCMPCR.LVD2E = 0 (disabling the voltage detection 2 circuit).

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Addition of description about Port Output Enable (POE) in Table 11.2 as follows.

Before correction

Table 11.2 Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Entering and Exiting Low Power Consumption Modes and Operating States	Sleep Mode	All-Module Clock Stop Mode	Software Standby Mode	Deep Software Standby Mode
Transition condition	Control register + instruction	Control register + instruction	Control register + instruction	Control register + instruction
		--- omitted ---		
8-bit timer (unit 0, unit 1) (TMR)	Operating possible	Operating possible*11	Stopped (Retained)	Stopped (Undefined)
Voltage detection circuit (LVDA)	Operating possible	Operating possible	Operating possible	Operating possible *12, *13
Power-on reset circuit	Operating	Operating	Operating	Operating*13
Peripheral modules	Operating possible	Stopped (Retained)	Stopped (Retained)	Stopped (Undefined)
I/O ports	Operating	Retained*14	Retained*15	Retained*15

“Operating possible” means that operating or stopped can be controlled by the control register setting.

“Stopped (Retained)” means that internal register values are retained and internal operations are suspended.

“Stopped (Undefined)” means that internal register values are undefined and power is not supplied to the internal circuit.

Note 1. “Interrupts” here indicates an external pin interrupt (the NMI or IRQ0 to IRQ15) or any of peripheral interrupts (the 8-bit timer, RTC alarm, RTC periodic, IWDT, USB suspend/resume, voltage monitoring 1, voltage monitoring 2, and main-clock oscillation stop detection).

--- omitted ---

Note 12. If the voltage monitoring 1 circuit mode selection bit in the voltage monitoring 1 circuit control register 0 (LVD1CR0.LVD1RI) or the voltage monitoring 2 circuit mode selection bit in the voltage monitoring 2 circuit control register 0 (LVD2CR0.LVD2RI) is 1, the transition is to software standby mode rather than deep software standby mode.

Note 13. When the deep cut bits in the deep standby control register (DPSBYCR.DEEPCUT[1:0]) are set to 11b and the LSI enters deep software standby mode, the voltage detection circuit stops and the low power consumption function of the power-on reset circuit is enabled.

Note 14. If pin P53 is being used for the BCLK signal, operation continues with as-is output of BCLK. While the 8-bit timer and RTC are operated, the related pins continue operation.

Note 15. Retention of levels or placement in the high-impedance state is selectable for the address bus and bus control signals (CS0# to CS7#, RD#, WR0# to WR3#, WR#, BC0# to BC3#, ALE, CKE, SDCS#, RAS#, CAS#, WE#, and DQM0 to DQM3) by the output port enable bit (OPE) in the standby control register (SBYCR).

After correction

Table 11.2 Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Entering and Exiting Low Power Consumption Modes and Operating States	Sleep Mode	All-Module Clock Stop Mode	Software Standby Mode	Deep Software Standby Mode
Transition condition	Control register + instruction	Control register + instruction	Control register + instruction	Control register + instruction
--- omitted ---				
8-bit timer (unit 0, unit 1) (TMR)	Operating possible	Operating possible*11	Stopped (Retained)	Stopped (Undefined)
Port Output Enable (POE)	Operating possible	Operating possible*12	Stopped (Retained)	Stopped (Undefined)
Voltage detection circuit (LVDA)	Operating possible	Operating possible	Operating possible	Operating possible *13, *14
Power-on reset circuit	Operating	Operating	Operating	Operating*14
Peripheral modules	Operating possible	Stopped (Retained)	Stopped (Retained)	Stopped (Undefined)
I/O ports	Operating	Retained*15	Retained*16	Retained*16

"Operating possible" means that operating or stopped can be controlled by the control register setting.

"Stopped (Retained)" means that internal register values are retained and internal operations are suspended.

"Stopped (Undefined)" means that internal register values are undefined and power is not supplied to the internal circuit.

Note 1. "Interrupts" here indicates an external pin interrupt (the NMI or IRQ0 to IRQ15) or any of peripheral interrupts (the 8-bit timer, RTC alarm, RTC periodic, IWDT, USB suspend/resume, voltage monitoring 1, voltage monitoring 2, and main-clock oscillation stop detection).

--- omitted ---

Note 12. When a source condition for POE interrupts is satisfied while POE interrupts are enabled and the chip is in all-module clock stop mode, the flag for the source condition is retained but return from all-module clock stop mode does not proceed. If a different source initiates return from all-module clock stop mode in this situation, the POE interrupt is generated after that.

Note 13. If the voltage monitoring 1 circuit mode selection bit in the voltage monitoring 1 circuit control register 0 (LVD1CR0.LVD1RI) or the voltage monitoring 2 circuit mode selection bit in the voltage monitoring 2 circuit control register 0 (LVD2CR0.LVD2RI) is 1, the transition is to software standby mode rather than deep software standby mode.

Note 14. When the deep cut bits in the deep standby control register (DPSBYCR.DEEPCUT[1:0]) are set to 11b and the LSI enters deep software standby mode, the voltage detection circuit stops and the low power consumption function of the power-on reset circuit is enabled.

Note 15. If pin P53 is being used for the BCLK signal, operation continues with as-is output of BCLK. While the 8-bit timer and RTC are operated, the related pins continue operation.

Note 16. Retention of levels or placement in the high-impedance state is selectable for the address bus and bus control signals (CS0# to CS7#, RD#, WR0# to WR3#, WR#, BC0# to BC3#, ALE, CKE, SDCS#, RAS#, CAS#, WE#, and DQM0 to DQM3) by the output port enable bit (OPE) in the standby control register (SBYCR).

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Addition of description of function at SSBY bit in 11.2.1 as follows.

Before correction

SSBY Bit (Software Standby)

The SSBY bit specifies the transition destination after the WAIT instruction is executed.

--- omitted ---

When the code flash P/E mode entry bit in the flash P/E mode entry register (FENTRYR.FENTRYC) is 1, the setting of this bit is ineffective. Sleep mode is entered on execution of the WAIT instruction even if this bit has been set to 1.

After correction

SSBY Bit (Software Standby)

The SSBY bit specifies the transition destination after the WAIT instruction is executed.

--- omitted ---

When the code flash P/E mode entry bit in the flash P/E mode entry register (FENTRYR.FENTRYC) is 1 or the data flash memory P/E mode entry bit (FENTRYR.FENTRYD)*1 is 1, the setting of this bit is ineffective. Sleep mode is entered on execution of the WAIT instruction even if this bit has been set to 1.

Note 1. This is only available for products with at least 1.5 Mbytes of code flash memory.

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Addition of description of function at ACSE bit in 11.2.2 as follows.

Before correction

ACSE Bit (All-Module Clock Stop Mode Enable)

The ACSE bit enables or disables a transition to all-module clock stop mode.
--- omitted ---
When the code flash P/E mode entry bit in the flash P/E mode entry register (FENTRYR.FENTRYC) is 1, the setting of this bit is ineffective. Sleep mode is entered on execution of the WAIT instruction if this bit has been set to 1.

After correction

ACSE Bit (All-Module Clock Stop Mode Enable)

The ACSE bit enables or disables a transition to all-module clock stop mode.
--- omitted ---
When the code flash P/E mode entry bit in the flash P/E mode entry register (FENTRYR.FENTRYC) is 1 or the data flash memory P/E mode entry bit (FENTRYR.FENTRYD)*1 is 1, the setting of this bit is ineffective. Sleep mode is entered on execution of the WAIT instruction if this bit has been set to 1.

Note 1. This is only available for products with at least 1.5 Mbytes of code flash memory.

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Description of bit function in 13.1.1 is corrected as follows.

Before correction

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect Bit 0	Enables writing to the registers related to the clock generation circuit. 0: Write disabled 1: Write enabled	R/W
b1	PRC1	Protect Bit 1	Enables writing to the registers related to operating modes, low power consumption, and software reset. 0: Write disabled 1: Write enabled	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	PRC3	Protect Bit 3	Enables writing to the registers related to the LVD. 0: Write disabled 1: Write enabled	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	PRKEY[7:0]	PRC Key Code	These bits control permission and prohibition of writing to the PRCR register. To modify the PRCR register, write A5h to the eight higher-order bits and the desired value to the eight lower-order bits as a 16-bit unit.	R/(W)*1

After correction

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect Bit 0	Enables writing to the registers related to the clock generation circuit. 0: Write disabled 1: Write enabled	R/W
b1	PRC1	Protect Bit 1	Enables writing to the registers related to operating modes, clock generation circuit, low power consumption, and software reset. 0: Write disabled 1: Write enabled	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	PRC3	Protect Bit 3	Enables writing to the registers related to the LVD. 0: Write disabled 1: Write enabled	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	PRKEY[7:0]	PRC Key Code	These bits control permission and prohibition of writing to the PRCR register. To modify the PRCR register, write A5h to the eight higher-order bits and the desired value to the eight lower-order bits as a 16-bit unit.	R/(W)*1

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Addition of description in 17.3.3 as follows.

Before correction

17.3.3 Protection of Registers Related to the Memory-Protection Unit

Registers related to the memory-protection unit are not accessible through means of access other than operand access by the CPU (i.e. by instruction fetching or DMA). Attempted access to registers related to the memory-protection unit in user mode through operand access by the CPU leads to a data memory-protection error regardless of whether or not memory protection is in effect at the given location.

After correction

17.3.3 Protection of Registers Related to the Memory-Protection Unit

Registers related to the memory-protection unit are not accessible through means of access other than operand access by the CPU (i.e. by instruction fetching or DMA). The registers related to the memory-protection unit are only accessible in supervisor mode. Attempted access to registers related to the memory-protection unit in user mode through operand access by the CPU leads to a data memory-protection error regardless of whether or not memory protection is in effect at the given location.

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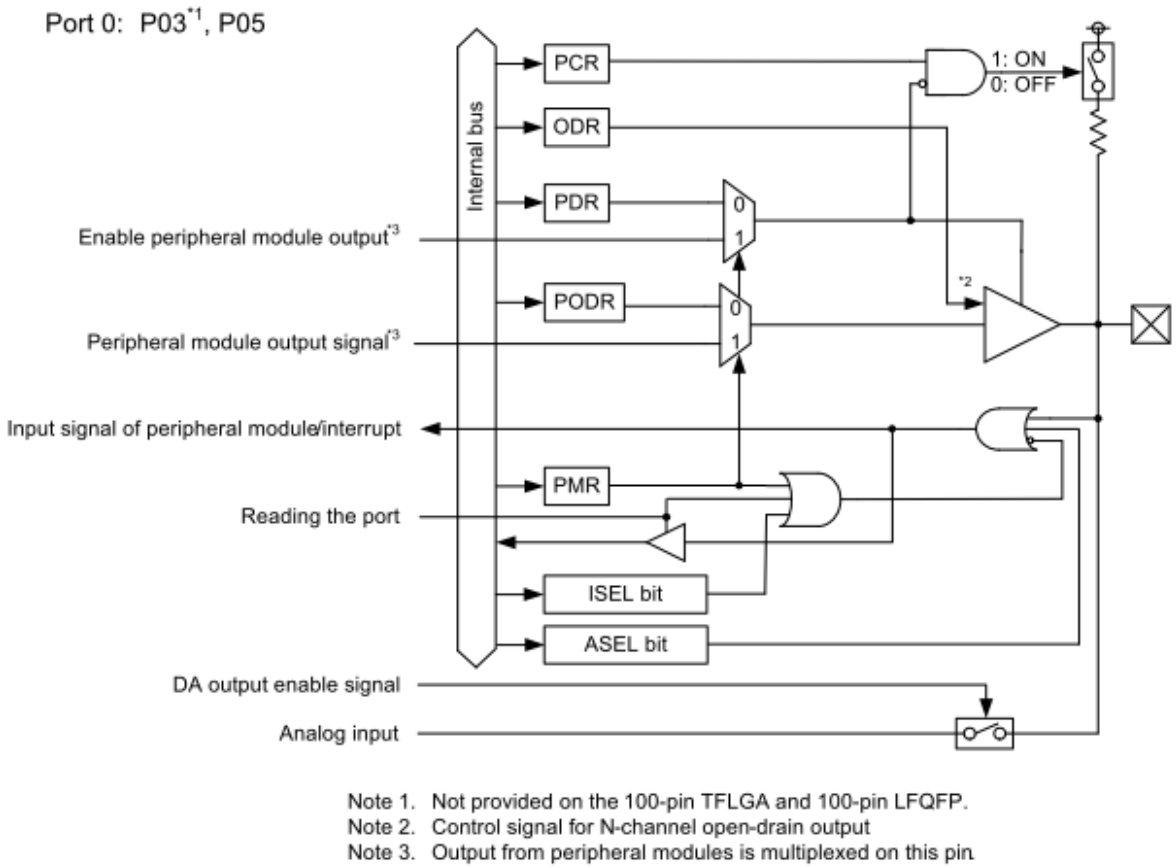
Description of signal direction in Figure 22.1 is corrected as follows.

Before correction

--- upper part omitted ---

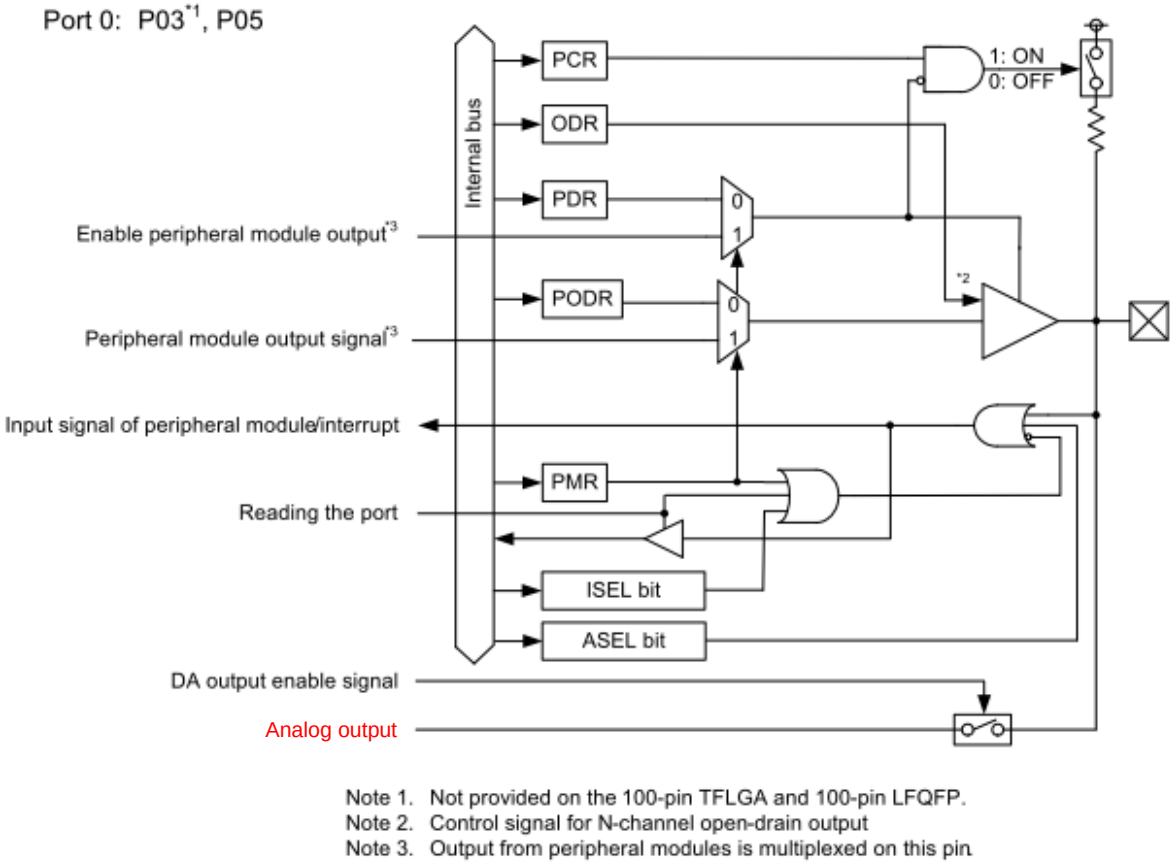


Note 1. Not provided on the 100-pin TFLGA and 100-pin LFQFP.
Note 2. Control signal for N-channel open-drain output
Note 3. Output from peripheral modules is multiplexed on this pin.

Figure 22.1 I/O Port Configuration (1)

After correction

--- upper part omitted ---



Note 1. Not provided on the 100-pin TFLGA and 100-pin LFQFP.
Note 2. Control signal for N-channel open-drain output
Note 3. Output from peripheral modules is multiplexed on this pin.

Figure 22.1 I/O Port Configuration (1)

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Description of Port Output Data Register (PODR) in 22.3.2 is corrected as follows.

Before correction

PODR is a register which holds the data to be output from the pins used for general I/O.
Bits that correspond to port m on the 176-pin product but do not exist on a product with fewer pins are reserved. When writing, write 0 (low output) to these bits.
The B5 bit in PORT3.PDR is reserved, because the P35 pin is input only. Data is not output from the corresponding pins even if these bits are set.
The bit corresponding to a pin that does not exist is reserved. A reserved bit is always read as 0. The write value should always be 0.

After correction

PODR is a register which holds the data to be output from the pins used for general I/O.
Bits that correspond to port m on the 176-pin product but do not exist on a product with fewer pins are reserved. When writing, write 0 (low output) to these bits.
The B5 bit in PORT3.PODR is reserved, because the P35 pin is input only. Data is not output from the corresponding pins even if these bits are set.
The bit corresponding to a pin that does not exist is reserved. A reserved bit is always read as 0. The write value should always be 0.

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Description of multiplexed pin function in Table 23.1 is corrected as follows.

Before correction

Table 23.1 Functions Assigned to Each Multiplexed Pin (13/18)

Module/Function	Channel	Pin Functions	Allocation Port	Package 177-pin 176-pin	145-pin 144-pin	100-pin
I2C bus interface	RIIC0	SCL0[FM+] (input/output)	P12	✓	✓	✓
		SDA0[FM+] (input/output)	P13	✓	✓	✓
	RIIC1*2	SCL1 (input/output)	P21	✓	✓	×
		SDA1 (input/output)	P20	✓	✓	×
	RIIC2	SCL2-DS (input/output)	P16	✓	✓	✓
		SDA2-DS (input/output)	P17	✓	✓	✓
--- omitted ---						

After correction

Table 23.1 Functions Assigned to Each Multiplexed Pin (13/18)

Module/Function	Channel	Pin Functions	Allocation Port	Package 177-pin 176-pin	145-pin 144-pin	100-pin
I2C bus interface	RIIC0	SCL0[FM+] (input/output)	P12	✓	✓	✓
		SDA0[FM+] (input/output)	P13	✓	✓	✓
	RIIC1*2	SCL1 (input/output)	P21	✓	✓	✓
		SDA1 (input/output)	P20	✓	✓	✓
	RIIC2	SCL2-DS (input/output)	P16	✓	✓	✓
		SDA2-DS (input/output)	P17	✓	✓	✓
--- omitted ---						

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Description of register settings for input/output pin function in Table 23.6 is corrected as follows.

Before correction

Table 23.6 Register Settings for Input/Output Pin Function in 177-/145-/100-Pin TFLGA, 176-Pin LFBGA, 176-/144-/100-Pin LFQFP

PSEL[5:0] settings	Pin P20	P21	P22	P23	P24	P25	P26	P27
000000b (initial value)	Hi-Z							
--- omitted ---								
001101b	–	–	–	–	–	–	MOSIB-A	RSPCKB-A
001111b*1, *2	SDA1	SCL1	–	–	–	–	–	–
011000b	–	–	EDREQ0	EDACK0	EDREQ1	EDACK1	–	–
011010b*1, *2	SDHI_CMD-C	SDHI_CLK-C	SDHI_D0-C	SDHI_D1-C	SDHI_WP	SDHI_CD	–	–
011100b*1	PIXD4	PIXD5	PIXD6	PIXD7	PIXCLK	HSYNC	–	–

After correction

Table 23.6 Register Settings for Input/Output Pin Function in 177-/145-/100-Pin TFLGA, 176-Pin LFBGA, 176-/144-/100-Pin LFQFP

PSEL[5:0] settings	Pin							
	P20	P21	P22	P23	P24	P25	P26	P27
000000b (initial value)	Hi-Z							
--- omitted ---								
001101b	–	–	–	–	–	–	MOSIB-A	RSPCKB-A
001111b*2	SDA1	SCL1	–	–	–	–	–	–
011000b	–	–	EDREQ0	EDACK0	EDREQ1	EDACK1	–	–
011010b*1, *2	SDHI_CMD-C	SDHI_CLK-C	SDHI_D0-C	SDHI_D1-C	SDHI_WP	SDHI_CD	–	–
011100b*1	PIXD4	PIXD5	PIXD6	PIXD7	PIXCLK	HSYNC	–	–

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Description of register settings for input/output pin function in Table 23.8 is corrected as follows.

Before correction

Table 23.8 Register Settings for Input/Output Pin Function in 177-Pin TFLGA, 176-Pin LFBGA, 176-Pin LFQFP

PSEL[5:0] Settings	Pin						
	P50	P51	P52	P54	P55	P56	P57
000000b (initial value)	Hi-Z						
--- omitted ---							
010001b	–	–	–	ET0_LINKSTA	ET0_EXOUT	–	–
011000b	–	–	–	EDACK0	EDREQ0	EDACK1	–
011001b	–	–	–	LCD_DATA6-A	LCD_DATA5-A	LCD_DATA4-A	LCD_DATA3-A

After correction

Table 23.8 Register Settings for Input/Output Pin Function in 177-Pin TFLGA, 176-Pin LFBGA, 176-Pin LFQFP

PSEL[5:0] Settings	Pin						
	P50	P51	P52	P54	P55	P56	P57
000000b (initial value)	Hi-Z						
--- omitted ---							
010001b	–	–	–	ET0_LINKSTA	ET0_EXOUT	–	–
011000b	–	–	–	EDACK0	EDREQ0	EDACK1	–
100101b	–	–	–	LCD_DATA6-A	LCD_DATA5-A	LCD_DATA4-A	LCD_DATA3-A

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Description of register settings for input/output pin function in Table 23.19 is corrected as follows.

Before correction

Table 23.19 Register Settings for Input/Output Pin Function in 177-/145-/100-Pin TFLGA, 176-Pin LFBGA, 176-/144-/100-Pin LFQFP

PSEL[5:0] Settings	Pin							
	PC0	PC1	PC2	PC3	PC4	PC5	PC6	PC7
000000b (initial value)	Hi-Z							
--- omitted ---								
011001b*1	–	–	MMC_CD-A	MMC_D0-A	MMC_D1-A	MMC_D5-A	MMC_D6-A	MMC_D7-A
011010b*1	–	–	**SDHI_CD-A**	SDHI_D0-A	SDHI_D1-A	–	–	–
011011b*1	–	–	–	QIO0-A QMO-A	QIO1-A QMI-A	–	–	–
--- omitted ---								

After correction

Table 23.19 Register Settings for Input/Output Pin Function in 177-/145-/100-Pin TFLGA, 176-Pin LFBGA, 176-/144-/100-Pin LFQFP

PSEL[5:0] Settings	Pin							
	PC0	PC1	PC2	PC3	PC4	PC5	PC6	PC7
000000b (initial value)	Hi-Z							
--- omitted ---								
011001b*1	–	–	MMC_CD-A	MMC_D0-A	MMC_D1-A	MMC_D5-A	MMC_D6-A	MMC_D7-A
011010b*1	–	–	**SDHI_D3-A**	SDHI_D0-A	SDHI_D1-A	–	–	–
011011b*1	–	–	–	QIO0-A QMO-A	QIO1-A QMI-A	–	–	–
--- omitted ---								

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Description of bit name of External Bus Control Register 0 (PFBCR0) in 23.2.24 is corrected as follows.

Before correction

Bit	Symbol	Bit Name	Description	R/W
b0	ADRLE	A0 to A7 Output Enable	0: Configures PA0 to PA7 as the I/O port pins. 1: Configures PA0 to PA7 as the external address bus A0 to A7.	R/W
b1	ADRHMS	A16 to A23 Output Enable	See Table 23.25.	R/W
b2	ADRHMS2	A16 to A23 Output Enable		R/W
b3	BCLKO	BCLK Forced Output	0: BCLK is output when EXBE = 1 and not output when EXBE = 0. 1: BCLK is output regardless of the setting of EXBE.	R/W
--- omitted ---				

After correction

Bit	Symbol	Bit Name	Description	R/W
b0	ADRLE	A0 to A7 Output Enable	0: Configures PA0 to PA7 as the I/O port pins. 1: Configures PA0 to PA7 as the external address bus A0 to A7.	R/W
b1	ADRHMS	A16 to A23 Output Enable	See Table 23.25.	R/W
b2	ADRHMS2	A16 to A23 Output Enable 2		R/W
b3	BCLKO	BCLK Forced Output	0: BCLK is output when EXBE = 1 and not output when EXBE = 0. 1: BCLK is output regardless of the setting of EXBE.	R/W
--- omitted ---				

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Description of usage notes in 49.4 is corrected as follows.

Before correction

49.4 Usage Notes

(1) Pin serial transfer, data are input or output in LSB order (see Figure 49.3).

--- omitted ---

(14) Figure 49.4 (2) shows the pin configuration of the pins P00 to P02, P40 to P47, P90 to P93, PD0 to PD7, and PE0 to PE7. When the boundary scan function is used with pins P00 to P02, P40 to P47, P90 to P93, PD0 to PD7, and PE0 to PE7 to be used as AD input pins (AN000 to AN007, ANEX0, ANEX1, and AN100 to AN120), the conflict with open-drain output or sneak current might be generated.

--- omitted ---

After correction

49.4 Usage Notes

(1) Pin serial transfer, data are input or output in LSB order (see Figure 49.3).

--- omitted ---

(14) Figure 49.4 (2) shows the pin configuration of the pins P00 to P02, P40 to P47, P90 to P93, PD0 to PD7, and PE0 to PE7. When the boundary scan function is used with pins P00 to P02, P40 to P47, P90 to P93, PD0 to PD7, and PE0 to PE7 to be used as AD input pins (AN000 to AN007, ANEX0, ANEX1, and AN100 to AN120), the conflict with the AD input or sneak current might be generated.

--- omitted ---

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Description of pin handling in Table 59.10 is corrected as follows.

Before correction

Table 59.10 Pin Handling in Boot Mode (FINE Interface)

Pin Name	Name	I/O	Function
VCC, VSS	Power supply input	Input	Input 2.7V or higher to the VCC pin. Input 0V to the VSS pin.
VCL	Decoupling capacitor connect pin	–	Connect to the VSS pin via a 0.22-µF multilayer ceramic capacitor for stabilizing the internal voltage.
MD	Operating mode control/ data I/O	I/O	Connect the **VSS** pin via a resistor (pull up).
RES#	Reset input	Input	Reset pin. Connect to the reset circuit.

After correction

Table 59.10 Pin Handling in Boot Mode (FINE Interface)

Pin Name	Name	I/O	Function
VCC, VSS	Power supply input	Input	Input 2.7V or higher to the VCC pin. Input 0V to the VSS pin.
VCL	Decoupling capacitor connect pin	–	Connect to the VSS pin via a 0.22-µF multilayer ceramic capacitor for stabilizing the internal voltage.
MD	Operating mode control/ data I/O	I/O	Connect the **VCC** pin via a resistor (pull up).
RES#	Reset input	Input	Reset pin. Connect to the reset circuit.

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Description of data packet structure in 59.13.25 is corrected as follows.

Before correction

(2) Data packet structure

SOD	LNH	LNL	RES	NOA	SUM	ETX

SOD : 81h
LNH : 00h
LNL : **01h**
RES : 53h (OK)
NOA : Number of area information (1 byte)
05h (for products with at least 1.5 Mbytes of code flash memory in linear mode)
08h (for products with at least 1.5 Mbytes of code flash memory in dual mode)
04h (for products with 1 Mbyte of code flash memory or less)
SUM : Sum of values
ETX : 03h

After correction

(2) Data packet structure

SOD	LNH	LNL	RES	NOA	SUM	ETX

SOD : 81h
LNH : 00h
LNL : **02h**
RES : 53h (OK)
NOA : Number of area information (1 byte)
05h (for products with at least 1.5 Mbytes of code flash memory in linear mode)
08h (for products with at least 1.5 Mbytes of code flash memory in dual mode)
04h (for products with 1 Mbyte of code flash memory or less)
SUM : Sum of values
ETX : 03h

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Description of SAD address in 59.13.26 is corrected as follows.

Before correction

(2) Data packet structure

For products with 1 Mbyte of code flash memory or less

NUM	KOA	SAD	EAD	EAU	WAU	Description
00h	00h	FFFF 0000h	FFFF FFFFh	0000 2000h	0000 0080h	Code flash memory (8-Kbyte block)
01h	00h	**FFE0 0000h**	FFFE FFFFh	0000 8000h	0000 0080h	Code flash memory (32-Kbyte block)
02h	30h	FE7F 5D00h	FE7F 5D7Fh	0000 0080h	0000 0010h	Option-setting memory
03h	40h	FFFE 0000h	FFFE FFFFh	0000 8000h	0000 0080h	Trusted memory
	41h	FFFE 0000h	FFFE FFFFh	0000 8000h	0000 0080h	Trusted memory

After correction

(2) Data packet structure

For products with 1 Mbyte of code flash memory or less

NUM	KOA	SAD	EAD	EAU	WAU	Description
00h	00h	FFFF 0000h	FFFF FFFFh	0000 2000h	0000 0080h	Code flash memory (8-Kbyte block)
01h	00h	**FFF0 0000h**	FFFE FFFFh	0000 8000h	0000 0080h	Code flash memory (32-Kbyte block)
02h	30h	FE7F 5D00h	FE7F 5D7Fh	0000 0080h	0000 0010h	Option-setting memory
03h	40h	FFFE 0000h	FFFE FFFFh	0000 8000h	0000 0080h	Trusted memory
	41h	FFFE 0000h	FFFE FFFFh	0000 8000h	0000 0080h	Trusted memory

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Description of note of DC characteristics in Table 60.5 is corrected as follows.

Before correction

Table 60.5 DC Characteristics (3) (Products with 1 Mbyte of code flash memory or less)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V, Ta = Topr

Item	Symbol	D version		G version		Unit	Test Conditions
		Typ.	Max.	Typ.	Max.		
--- omitted ---							

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripheral modules is stopped in this state.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK/PCLKA:PCLKB/PCLKC/PCLKD:BCLK:BCLK pin = 10:5:10:5 when EXTAL = 12 MHz)
[D version]
I_{CC} Max. = 0.31 × f + 6.5 (max. operation in high-speed operating mode)
I_{CC} Typ. = 0.16 × f + 2.8 **(ICLK 1 MHz max)** (normal operation in high-speed operating mode)
I_{CC} Typ. = **0.4 × f + 1.1** (low-speed operating mode 1)
I_{CC} Max. = 0.15 × f + 6.5 (sleep mode)
[G version]
I_{CC} Max. = 0.33 × f + 9 (max. operation in high-speed operating mode)
I_{CC} Typ. = 0.16 × f + 2.8 **(ICLK 1 MHz max)** (normal operation in high-speed operating mode)
I_{CC} Typ. = **0.4 × f + 1.1** (low-speed operating mode 1)
I_{CC} Max. = 0.21 × f + 9 (sleep mode)
Note 4. Whether supply of the clock signal to peripheral modules continues or is stopped only depends on the state determined by the settings of the bits in module stop control registers A to D.
The setting for the peripheral module clock stopped state is FCLK = BCLK = PCLKA = PCLKB = PCLKC = PCLKD = BCLK pin = 3.75 MHz (division by 64).
Note 5. The low power consumption function is disabled and DEEPCUT[1:0] = 01b.
Note 6. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.
Note 7. Reference value

After correction

Table 60.5 DC Characteristics (3) (Products with 1 Mbyte of code flash memory or less)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V, Ta = Topr

Item	Symbol	D version		G version		Unit	Test Conditions
		Typ.	Max.	Typ.	Max.		
--- omitted ---							

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Peripheral module clocks are supplied.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK/PCLKA:PCLKB/PCLKC/PCLKD:BCLK:BCLK pin = 10:5:10:5 when EXTAL = 12 MHz)
[D version]
I_{CC} Max. = 0.31 × f + 6.5 (max. operation in high-speed operating mode)
I_{CC} Typ. = 0.16 × f + 2.8 (normal operation in high-speed operating mode)
I_{CC} Typ. = **0.1 × f + 1.0 (ICLK 1 MHz max)** (low-speed operating mode 1)
I_{CC} Max. = 0.15 × f + 6.5 (sleep mode)
[G version]
I_{CC} Max. = 0.33 × f + 9 (max. operation in high-speed operating mode)
I_{CC} Typ. = 0.16 × f + 2.8 (normal operation in high-speed operating mode)
I_{CC} Typ. = **0.1 × f + 1.0 (ICLK 1 MHz max)** (low-speed operating mode 1)
I_{CC} Max. = 0.21 × f + 9 (sleep mode)
Note 4. Whether supply of the clock signal to peripheral modules continues or is stopped only depends on the state determined by the settings of the bits in module stop control registers A to D.
The setting for the peripheral module clock stopped state is FCLK = BCLK = PCLKA = PCLKB = PCLKC = PCLKD = BCLK pin = 3.75 MHz (division by 64).
Note 5. The low power consumption function is disabled and DEEPCUT[1:0] = 01b.
Note 6. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.
Note 7. Reference value

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Description of note of DC characteristics in Table 60.6 is corrected as follows.

Before correction

Table 60.6 DC Characteristics (3) (Products for products with at least 1.5 Mbytes of code flash memory)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V, Ta = Topr

Item	Symbol	D version		G version		Unit	Test Conditions
		Typ.	Max.	Typ.	Max.		
--- omitted ---							

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripheral modules is stopped in this state.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK/PCLKA:PCLKB/PCLKC/PCLKD:BCLK:BCLK pin = 10:5:10:5 when EXTAL = 12 MHz)
[D version]
I_{CC} Max. = 0.38 × f + 14 (max. operation in high-speed operating mode)
I_{CC} Typ. = 0.18 × f + 4 **(ICLK 1 MHz max)** (normal operation in high-speed operating mode)
I_{CC} Typ. = **0.4 × f + 1.2** (low-speed operating mode 1)
I_{CC} Max. = 0.2 × f + 14 (sleep mode)
[G version]
I_{CC} Max. = 0.44 × f + 20 (max. operation in high-speed operating mode)
I_{CC} Typ. = 0.18 × f + 4 **(ICLK 1 MHz max)** (normal operation in high-speed operating mode)
I_{CC} Typ. = **0.4 × f + 1.2** (low-speed operating mode 1)
I_{CC} Max. = 0.27 × f + 20 (sleep mode)
Note 4. Whether supply of the clock signal to peripheral modules continues or is stopped only depends on the state determined by the settings of the bits in module stop control registers A to D.
The setting for the peripheral module clock stopped state is FCLK = BCLK = PCLKA = PCLKB = PCLKC = PCLKD = BCLK pin = 3.75 MHz (division by 64).
Note 5. The low power consumption function is disabled and DEEPCUT[1:0] = 01b.
Note 6. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.
Note 7. These are the increases during programming of the code flash memory after the code flash memory (limitations apply to the combinations of address ranges of the program area and the readable area) or the data flash memory has been programmed or erased.
Note 8. Reference value

After correction

Table 60.6 DC Characteristics (3) (Products for products with at least 1.5 Mbytes of code flash memory)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V, Ta = Topr

Item	Symbol	D version		G version		Unit	Test Conditions
		Typ.	Max.	Typ.	Max.		
--- omitted ---							

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Peripheral module clocks are supplied.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK/PCLKA:PCLKB/PCLKC/PCLKD:BCLK:BCLK pin = 10:5:10:5 when EXTAL = 12 MHz)
[D version]
I_{CC} Max. = 0.38 × f + 14 (max. operation in high-speed operating mode)
I_{CC} Typ. = 0.18 × f + 4 (normal operation in high-speed operating mode)
I_{CC} Typ. = **0.1 × f + 1.5 (ICLK 1 MHz max)** (low-speed operating mode 1)
I_{CC} Max. = 0.2 × f + 14 (sleep mode)
[G version]
I_{CC} Max. = 0.44 × f + 20 (max. operation in high-speed operating mode)
I_{CC} Typ. = 0.18 × f + 4 (normal operation in high-speed operating mode)
I_{CC} Typ. = **0.1 × f + 1.5 (ICLK 1 MHz max)** (low-speed operating mode 1)
I_{CC} Max. = 0.27 × f + 20 (sleep mode)
Note 4. Whether supply of the clock signal to peripheral modules continues or is stopped only depends on the state determined by the settings of the bits in module stop control registers A to D.
The setting for the peripheral module clock stopped state is FCLK = BCLK = PCLKA = PCLKB = PCLKC = PCLKD = BCLK pin = 3.75 MHz (division by 64).
Note 5. The low power consumption function is disabled and DEEPCUT[1:0] = 01b.
Note 6. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.
Note 7. These are the increases during programming of the code flash memory after the code flash memory (limitations apply to the combinations of address ranges of the program area and the readable area) or the data flash memory has been programmed or erased.
Note 8. Reference value

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Description of DC characteristics in Table 60.7 is corrected as follows.

Before correction

Table 60.7 DC Characteristics (4)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
Ta = Topr

Item			Symbol	D version			G version			Unit	Test Conditions
				Min.	Typ.	Max.	Min.	Typ.	Max.		
Analog power supply current*1	During 12-bit A/D conversion (unit 0)		AI_{CC}	—	0.8	1	—	0.8	1	mA	IAVCC0_AD
	During 12-bit A/D conversion (unit 0) with the channel-dedicated sample-and-hold circuits for 3 channels operating			—	1.7	2.5	—	1.7	2.5	mA	IAVCC0_AD+SH
	During 12-bit A/D conversion (unit 1)			—	0.6	1	—	0.6	1	mA	IAVCC1_AD
	During 12-bit A/D conversion (unit 1) with the temperature sensor operating			—	0.7	1.1	—	0.7	1.1	mA	IAVCC1_AD+TEMP
	During D/A conversion (per unit)	Unbuffered output		—	0.25	0.4	—	0.25	0.4	mA	IAVCC1_DA
		Buffered output		—	0.57	0.8	—	0.57	0.8	mA	
	Waiting for A/D, D/A, or temperature sensor conversion (all units)			—	0.9	1.4	—	0.9	1.4	mA	IAVCC0 + IAVCC1
	A/D, D/A converter, temperature sensor in standby mode (all units)			—	1.4	6.7	—	1.4	9.0	μA	IAVCC0 + IAVCC1
--- omitted ---											

After correction

Table 60.7 DC Characteristics (4)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
Ta = Topr

Item			Symbol	D version			G version			Unit	Test Conditions
				Min.	Typ.	Max.	Min.	Typ.	Max.		
Analog power supply current*1	During 12-bit A/D conversion (unit 0)		AI_{CC}	—	0.8	1	—	0.8	1	mA	IAVCC0_AD
	During 12-bit A/D conversion (unit 0) with the channel-dedicated sample-and-hold circuits for 3 channels operating			—	1.7	2.5	—	1.7	2.5	mA	IAVCC0_AD+SH
	During 12-bit A/D conversion (unit 1)			—	0.6	1	—	0.6	1	mA	IAVCC1_AD
	During 12-bit A/D conversion (unit 1) with the temperature sensor operating			—	0.7	1.1	—	0.7	1.1	mA	IAVCC1_AD+TEMP
	During D/A conversion (per unit)	Unbuffered output		—	0.25	0.4	—	0.25	0.4	mA	IAVCC1_DA
		Buffered output		—	0.75	1.1	—	0.75	1.1	mA	
	Waiting for A/D, D/A, or temperature sensor conversion (all units)			—	0.9	1.4	—	0.9	1.4	mA	IAVCC0 + IAVCC1
	A/D, D/A converter, temperature sensor in standby mode (all units)			—	1.4	6.7	—	1.4	9.0	μA	IAVCC0 + IAVCC1
--- omitted ---											