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RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-RX*-A081A/E	Rev.	1.00
Title	Errata to RX63N Group, RX631 Group User's Manual regarding the RAM		Information Category	Technical Notification		
Applicable Product	RX63N Group, RX631 Group	Lot No. All	Reference Document	RX63N Group, RX631 Group User's Manual: Hardware Rev.1.70 (R01UH0041EJ0170)		

This document describes corrections to descriptions for the RAM in RX63N Group, RX631 Group User's Manual: Hardware Rev.1.70.

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The address for the RAM in Figure 4.1 is corrected as follows:

Before correction

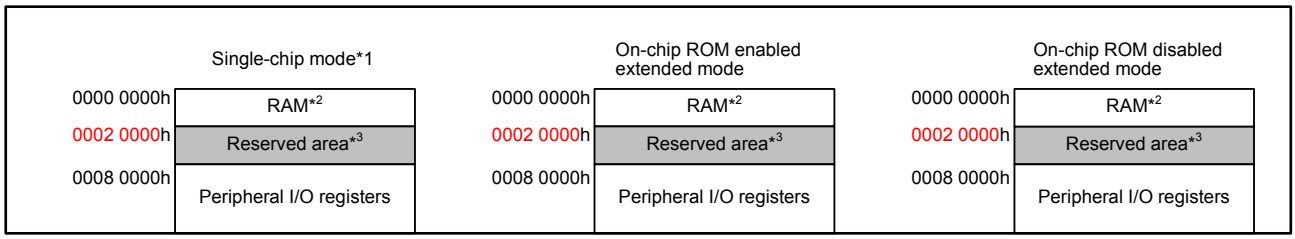

Figure 4.1 Memory Map in Each Operating Mode

After correction

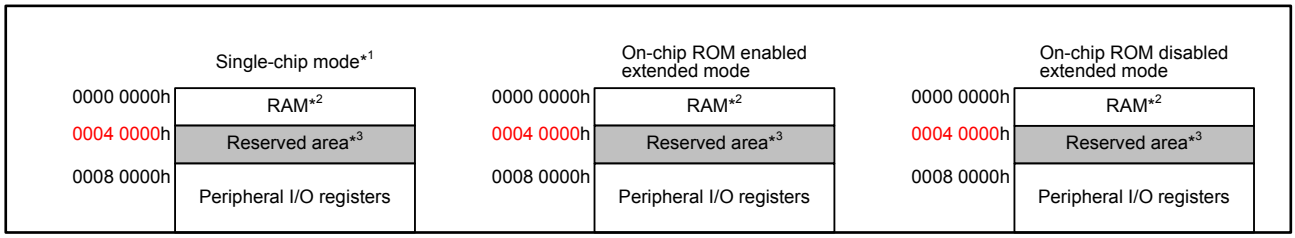

Figure 4.1 Memory Map in Each Operating Mode

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The address for the RAM in Figure 4.2 is corrected as follows:

Before correction

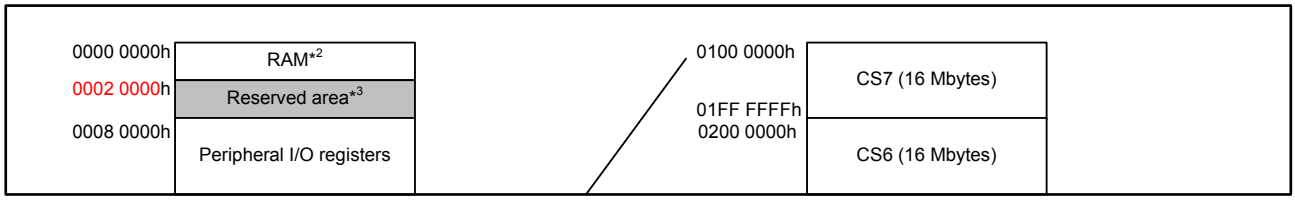

Figure 4.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)

After correction

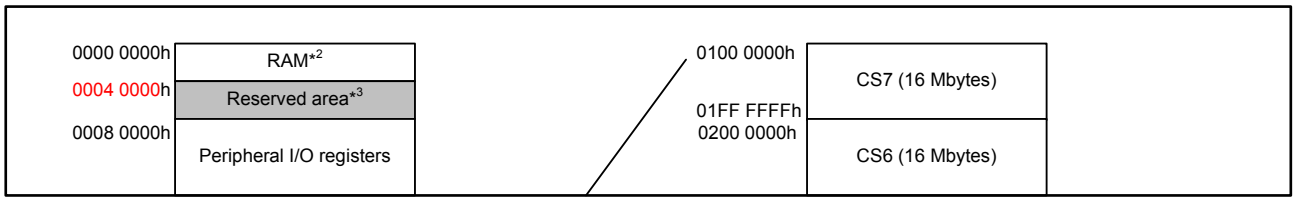

Figure 4.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)

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Table 11.2 is corrected as follows:

Before correction

Table 11.2 Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Entering and Exiting Low Power Consumption Modes and Operating States	Sleep Mode	All-Module Clock Stop Mode	Software Standby Mode	Deep Software Standby Mode
		⋮ *Omitted*		
CPU	Stopped (Retained)	Stopped (Retained)	Stopped (Retained)	Stopped (Undefined)
RAM3 (0003 0000h to 0003 FFFFh)	Operating possible (Retained)	Stopped (Retained)	Stopped (Retained)	Stopped (Undefined)
RAM2 (0002 0000h to 0002 FFFFh)	Operating possible (Retained)	Stopped (Retained)	Stopped (Retained)	Stopped (Undefined)
RAM1 (0001 0000h to 0001 FFFFh)	Operating possible (Retained)	Stopped (Retained)	Stopped (Retained)	Stopped (Undefined)
RAM0 (0000 0000h to 0000 FFFFh)	Operating possible (Retained)	Stopped (Retained)	Stopped (Retained)	Stopped (Retained/Undefined)*8
Flash memory	Operating	Stopped (Retained)	Stopped (Retained)	Stopped (Retained)
		⋮ *Omitted*		

After correction

Table 11.2 Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Entering and Exiting Low Power Consumption Modes and Operating States	Sleep Mode	All-Module Clock Stop Mode	Software Standby Mode	Deep Software Standby Mode
		⋮ *Omitted*		
CPU	Stopped (Retained)	Stopped (Retained)	Stopped (Retained)	Stopped (Undefined)
RAM1 (0001 0000h to 0003 FFFFh)	Operating possible (Retained)	Stopped (Retained)	Stopped (Retained)	Stopped (Undefined)
RAM0 (0000 0000h to 0000 FFFFh)	Operating possible (Retained)	Stopped (Retained)	Stopped (Retained)	Stopped (Retained/Undefined)*8
Flash memory	Operating	Stopped (Retained)	Stopped (Retained)	Stopped (Retained)
		⋮ *Omitted*		

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11.2.4 Module Stop Control Register C (MSTPCRC) is corrected as follows:

Before correction

Address: 0008 0018h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	MSTPC27	MSTPC26	MSTPC25	MSTPC24	—	MSTPC22	—	—	MSTPC19	MSTPC18	MSTPC17	MSTPC16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	MSTPC3	MSTPC2	MSTPC1	MSTPC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MSTPC0	RAM0 Module Stop*1	Target module: RAM0 (0000 0000h to 0000 FFFFh) 0: RAM0 operating 1: RAM0 stopped	R/W
b1	MSTPC1	RAM1 Module Stop*1	Target module: RAM1 (0001 0000h to 0001 FFFFh) 0: RAM1 operating 1: RAM1 stopped	R/W
b2	MSTPC2	RAM2 Module Stop*1	Target module: RAM2 (0002 0000h to 0002 FFFFh) 0: RAM2 operating 1: RAM2 stopped	R/W
b3	MSTPC3	RAM3 Module Stop*1	Target module: RAM3 (0003 0000h to 0003 FFFFh) 0: RAM3 operating 1: RAM3 stopped	R/W
b15 to b4	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

⋮

Omitted

Note 1. The MSTPC0 to MSTPC3 bits should not be set to 1 during access to the corresponding on-chip RAM. The corresponding RAM should not be accessed while the MSTPC0 to MSTPC3 bits are set to 1.

Note 2. For entering software standby mode after rewriting the MSTPC18 bit, wait for two IEBUS clock (IECLK) cycles after rewriting, and execute the WAIT instruction.

After correction

Address: 0008 0018h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	MSTPC27	MSTPC26	MSTPC25	MSTPC24	—	MSTPC22	—	—	MSTPC19	MSTPC18	MSTPC17	MSTPC16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MSTPC1	MSTPC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MSTPC0	RAM0 Module Stop*1	Target module: RAM0 (0000 0000h to 0000 FFFFh) 0: RAM0 operating 1: RAM0 stopped	R/W
b1	MSTPC1	RAM1 Module Stop*1	Target module: RAM1 (0001 0000h to 0003 FFFFh) 0: RAM1 operating 1: RAM1 stopped	R/W
b15 to b2	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

⋮

Omitted

Note 1. The MSTPC0 and MSTPC1 bits should not be set to 1 during access to the corresponding on-chip RAM. The corresponding RAM should not be accessed while bits MSTPC0 and MSTPC1 are set to 1.

Note 2. For entering software standby mode after rewriting the MSTPC18 bit, wait for two IEBUS clock (IECLK) cycles after rewriting, and execute the WAIT instruction.

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Note 2 in 11.6.4.1 Transition to Deep Software Standby Mode is corrected as follows:

Before correction

Note 2. The RAM address space is divided into the RAM0 area to RAM3 area. For the RAM address space, see Table 11.2.

After correction

Note 2. The RAM address space is divided into the RAM0 area and RAM1 area. For the RAM address space, see Table 11.2.

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The address for the RAM in Table 16.2 is corrected as follows:

Before correction

Table 16.2 Addresses Assigned for Each Bus

	Type of Bus		Area	
	On-Chip ROM Mode		On-Chip ROM Mode	
Address	Enabled	Disabled	Enabled	Disabled
0000 0000h to 0001 FFFFh	Memory bus 1		On-chip RAM	
0002 0000h to 0007 FFFFh			Reserved area	

⋮
Omitted

After correction

Table 16.2 Addresses Assigned for Each Bus

	Type of Bus		Area	
	On-Chip ROM Mode		On-Chip ROM Mode	
Address	Enabled	Disabled	Enabled	Disabled
0000 0000h to 0003 FFFFh	Memory bus 1		On-chip RAM	
0004 0000h to 0007 FFFFh			Reserved area	

⋮
Omitted

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Table 46.1 is corrected as follows:

Before correction

Table 46.1 Specifications of RAM

Item	Description
RAM capacity	64 Kbytes (RAM0: 64 Kbytes) 128 Kbytes (RAM0: 64 Kbytes, RAM1: 64 Kbytes) 192 Kbytes (RAM0: 64 Kbytes, RAM1: 64 Kbytes, RAM2: 64 Kbytes) 256 Kbytes (RAM0: 64 Kbytes, RAM1: 64 Kbytes, RAM2: 64 Kbytes, RAM3: 64 Kbytes)
RAM address	RAM0: 0000 0000h to 0000 FFFFh (64 Kbytes) RAM1: 0001 0000h to 0001 FFFFh (64 Kbytes) RAM2: 0002 0000h to 0002 FFFFh (64 Kbytes) RAM3: 0003 0000h to 0003 FFFFh (64 Kbytes)
Access	• Single-cycle access is possible for both reading and writing. • RAM can be enabled or disabled.*1
Data retention function	Data in RAM0 can be retained in deep software standby mode.
Low-power consumption function	The module-stop state is independently selectable for RAM0 to RAM3.

After correction

Table 46.1 Specifications of RAM

Item	Description
RAM capacity	64 Kbytes (RAM0: 64 Kbytes) 128 Kbytes (RAM0: 64 Kbytes, RAM1: 64 Kbytes) 192 Kbytes (RAM0: 64 Kbytes, RAM1: 128 Kbytes) 256 Kbytes (RAM0: 64 Kbytes, RAM1: 192 Kbytes)
RAM address	• When the RAM capacity is 64 Kbytes RAM0: 0000 0000h to 0000 FFFFh (64 Kbytes) RAM1: None • When the RAM capacity is 128 Kbytes RAM0: 0000 0000h to 0000 FFFFh (64 Kbytes) RAM1: 0001 0000h to 0001 FFFFh (64 Kbytes) • When the RAM capacity is 192 Kbytes RAM0: 0000 0000h to 0000 FFFFh (64 Kbytes) RAM1: 0001 0000h to 0002 FFFFh (128 Kbytes) • When the RAM capacity is 256 Kbytes RAM0: 0000 0000h to 0000 FFFFh (64 Kbytes) RAM1: 0001 0000h to 0003 FFFFh (192 Kbytes)
Access	• Single-cycle access is possible for both reading and writing. • RAM can be enabled or disabled.*1
Data retention function	Data in RAM0 can be retained in deep software standby mode.
Low-power consumption function	The module-stop state is independently selectable for RAM0 and RAM1.

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Descriptions in 46.2.1 Data Retention are corrected as follows:

Before correction

The address space for RAM is divided into the RAM0 to RAM3 areas. The difference between the two is whether internal power can be supplied in deep software standby mode. Whether or not the supply of internal power to RAM0 continues in deep software standby mode is selectable by the DPSBYCR.DEEPCUT[1:0] bits.
If continuation of the supply of internal power is selected, data in RAM0 are retained in deep software standby mode. The supply of internal power supply to RAM1 to RAM3 is stopped at this time, so data are not retained in RAM1 to RAM3.
See section 11, Low Power Consumption, for details on the DPSBYCR.DEEPCUT[1:0] bits.

After correction

The address space for RAM is divided into the RAM0 and RAM1 areas. The difference between the two is whether internal power can be supplied in deep software standby mode. Whether or not the supply of internal power to RAM0 continues in deep software standby mode is selectable by the DPSBYCR.DEEPCUT[1:0] bits.
If continuation of the supply of internal power is selected, data in RAM0 are retained in deep software standby mode. The supply of internal power supply to RAM1 is stopped at this time, so data are not retained in RAM1.
See section 11, Low Power Consumption, for details on the DPSBYCR.DEEPCUT[1:0] bits.

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Description in 46.2.2 Low-Power Consumption Function is corrected as follows:

Before correction

If the MSTPCn bit in MSTPCRC is set to 1, supply of the clock signal to RAMn is stopped (n = 0 to 3).
The respective modules (RAM0 to RAM3) are thus placed in the module-stop state by stopping supply of the clock signals. The RAM operates after a reset.

After correction

If the MSTPCn bit in MSTPCRC is set to 1, supply of the clock signal to RAMn is stopped (n = 0, 1).
The respective modules (RAM0 and RAM1) are thus placed in the module-stop state by stopping supply of the clock signals. The RAM operates after a reset.

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The address for the RAM in Figure 49.1 is corrected as follows:

Before correction

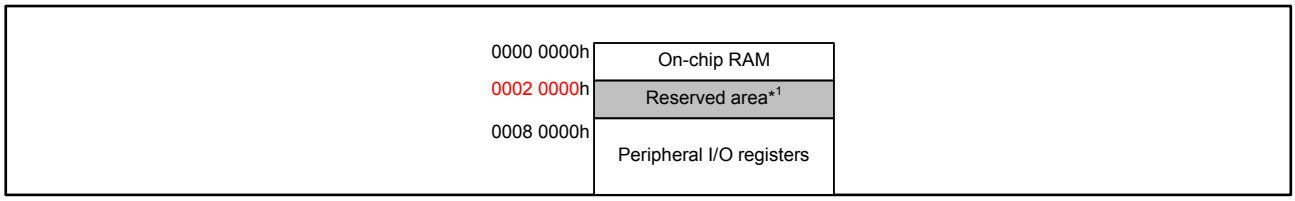

Figure 49.1 Memory Map in On-chip ROM Disabled Extended Mode

After correction

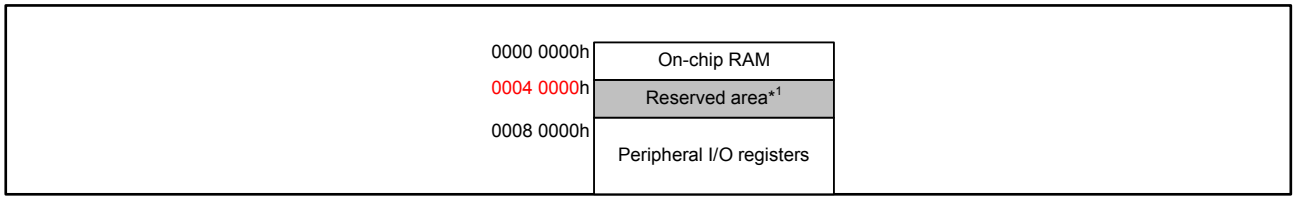

Figure 49.1 Memory Map in On-chip ROM Disabled Extended Mode