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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A0264A/E	Rev.	1.00
Title	Errata to the RX230 Group, RX231 Group User's Manual: Hardware		Information Category	Technical Notification		
Applicable Product	RX230 Group, RX231 Group	Lot No. All	Reference Document	RX230 Group, RX231 Group User's Manual: Hardware Rev.1.20 (R01UH0496EJ0120)		

This document describes corrections to the DC characteristics for P30 to P32 and PH0 to PH3 in the RX230 Group, RX231 Group User's Manual: Hardware, Rev.1.20.

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Number of the 5-V tolerant pins in Table 1.1, Outline of Specifications (2/4) is corrected as follows.

Before correction

Table 1.1 Outline of Specifications (2/4)

Classification	Module/Function	Description
		(Omitted)
I/O ports	General I/O ports	100-pin/64-pin/48-pin I/O: 79/43/30 (RX231 Group), 83/47/34 (RX230 Group) • Input: 1/1/1 Pull-up resistors: 79/43/30(RX231 Group), 83/47/34 (RX230 Group) • Open-drain outputs: 58/34/26 • 5-V tolerance: 8/5/5
		(Omitted)

After correction

Table 1.1 Outline of Specifications (2/4)

Classification	Module/Function	Description
		(Omitted)
I/O ports	General I/O ports	100-pin/64-pin/48-pin • I/O: 79/43/30 (RX231 Group), 83/47/34 (RX230 Group) • Input: 1/1/1 • Pull-up resistors: 79/43/30 (RX231 Group), 83/47/34 (RX230 Group) • Open-drain outputs: 58/34/26 • 5-V tolerance: 5/3/3
		(Omitted)

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Functions of P30 to P32 in Table 21.2, Port Functions are corrected as follows.

Before correction

Table 21.2 Port Functions

Port	Pin	Input Pull-up	Open Drain Output	Drive Capacity Switching	5-V Tolerant
(Omitted)					
PORT3	P30 to P32	○	○	○	○
(Omitted)					

After correction

Table 21.2 Port Functions

Port	Pin	Input Pull-up	Open Drain Output	Drive Capacity Switching	5-V Tolerant
(Omitted)					
PORT3	P30 to P32	○	○	○	—
(Omitted)					

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Description of Note 1 in Table 50.1, Absolute Maximum Ratings is corrected and Note 3 is added as follows.

Before correction

Table 50.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = VREFL= VSS_USB = 0 V

Item		Symbol	Value	Unit
(Omitted)				
Input voltage	Ports for 5 V tolerant*1	V_{in}	–0.3 to +6.5	V
	P03, P05, P07, P40 to P47		–0.3 to AVCC0 +0.3	
	Ports other than above		–0.3 to VCC +0.3	
(Omitted)				

Note 1. Ports 12, 13, 16, 17, 30, 31, 32, and B5 are 5 V tolerant.
Note 2. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, refer to section 1.2, List of Products.

After correction

Table 50.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = VREFL = VSS_USB = 0 V

Item		Symbol	Value	Unit
(Omitted)				
Input voltage	Ports for 5 V tolerant*1	V_{in}	–0.3 to +6.5	V
	P03, P05, P07, P40 to P47		–0.3 to AVCC0 + 0.3	
	Ports other than above*3		–0.3 to VCC + 0.3	
(Omitted)				

Note 1. P12, P13, P16, P17, and PB5 are 5 V tolerant.
Note 2. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, refer to section 1.2, List of Products.
Note 3. When the VBATT power supply is selected, P30 to P32 are rated from –0.3 V to VBATT + 0.3 V.

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ΔV_T of P30 to P32 and characteristics of PH0 to PH3 are added to Table 50.3, DC Characteristics (1) as follows; and the expression “other than RIIC input pin” is changed to specific pin names.

Before correction

Table 50.3 DC Characteristics (1)

Conditions: 2.7 V ≤ VCC = VCC_USB ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, Ta = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)		V_{IH}	VCC × 0.7	—	5.8	V	
	Ports 12, 13, 16, 17, port B5 (5 V tolerant)			VCC × 0.8	—	5.8		
	Ports 14 to 15, ports 20 to 27, ports 33 to 37, ports 50 to 55, ports A0 to A7, ports B0 to B4, B6, B7 ports C0 to C7, ports D0 to D7, ports E0 to E7, port J3, Ports 30 to 32 (when time capture event input is not selected), RES#			VCC × 0.8	—	VCC + 0.3		
	Ports 03, 05, 07, ports 40 to 47			AVCC0 × 0.8	—	AVCC0 + 0.3		
	Ports 30 to 32 (when time capture event input is selected)	When VCC is supplied		VCC × 0.8	—	VCC + 0.3		
		When VBATT is supplied		VBATT × 0.8	—	VBATT + 0.3		
	Ports 03, 05, 07, ports 40 to 47		V_{IL}	–0.3	—	AVCC0 × 0.2		
	RIIC input pin (except for SMBus)			–0.3	—	VCC × 0.3		
	Other than RIIC input pin or ports 30 to 32			–0.3	—	VCC × 0.2		
	Ports 30 to 32 (when time capture event input is selected)	When VCC is supplied		–0.3	—	VCC × 0.3		
		When VBATT is supplied		–0.3	—	VBATT × 0.3		
	Ports 03, 05, 07, ports 40 to 47		ΔV_T	AVCC0 × 0.1	—	—		
	RIIC input pin (except for SMBus)			VCC × 0.05	—	—		
	Ports 12, 13, 16, 17, Port B5			VCC × 0.05	—	—		
	Other than RIIC input pin			VCC × 0.1	—	—		
(Omitted)								

After correction

Table 50.3 DC Characteristics (1)

Conditions: 2.7 V ≤ VCC = VCC_USB ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = VSS_USB = 0 V, Ta = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)		V_{IH}	VCC × 0.7	—	5.8	V	
	P12, P13, P16, P17, PB5 (5 V tolerant)			VCC × 0.8	—	5.8		
	P14 to P15, P20 to P27, P33 to P37, P50 to P55, PA0 to PA7, PB0 to PB4, PB6, PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PH0 to PH3, PJ3, P30 to P32 (other than RTCICn pin), RES#			VCC × 0.8	—	VCC + 0.3		
	P03, P05, P07, P40 to P47			AVCC0 × 0.8	—	AVCC0 + 0.3		
	P30 to P32 (RTCICn pin)	When VCC is supplied		VCC × 0.8	—	VCC + 0.3		
		When VBATT is supplied		VBATT × 0.8	—	VBATT + 0.3		
	RIIC input pin (except for SMBus)		V_{IL}	–0.3	—	VCC × 0.3		
	P12 o P17, P20 to P27, P33 to P37, P50 to P55, PA0 to PA7, PB0 to PB7 PC0 to PC7, PD0 to PD7, PE0 to PE7, PH0 to PH3, PJ3, P30 to P32 (other than RTCICn pin), RES#			–0.3	—	VCC × 0.2		
	P03, P05, P07, P40 to P47			–0.3	—	AVCC0 × 0.2		
	P30 to P32 (RTCICn pin)	When VCC is supplied		–0.3	—	VCC × 0.3		
		When VBATT is supplied		–0.3	—	VBATT × 0.3		
	RIIC input pin (except for SMBus), P12, P13, P16, P17, PB5		ΔV_T	VCC × 0.05	—	—		
	P14 to P15, P20 to P27, P33 to P37, P50 to P55, PA0 to PA7, PB0 to PB4, PB6, PB7 PC0 to PC7, PD0 to PD7, PE0 to PE7, PH0 to PH3, PJ3, P30 to P32 (other than RTCICn pin), RES#			VCC × 0.1	—	—		
	P03, P05, P07, P40 to P47			AVCC0 × 0.1	—	—		
(Omitted)								

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Characteristics of P30 to P32 and PH0 to PH3 are added to Table 50.4, DC Characteristics (2) as follows; and the expression “Ports other than above” is changed to specific pin names.

Before correction

Table 50.4 DC Characteristics (2)

Conditions: 1.8 V ≤ VCC = VCC_USB < 2.7 V, 1.8 V ≤ AVCC0 < 2.7 V, VSS = AVSS0 = VSS_USB = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	Ports 12, 13, 16, 17, port B5 (5 V tolerant)	V_{IH}	VCC × 0.8	—	5.8	V	
	Ports 14 to 15, ports 20 to 27, ports 30 to 37, ports 50 to 55, ports A0 to A7, ports B0 to B4, B6, B7, ports C0 to C7, ports D0 to D7, ports E0 to E7, port J3, RES#		VCC × 0.8	—	VCC + 0.3		
	Ports 03, 05, 07, ports 40 to 47		AVCC0 × 0.8	—	AVCC0 + 0.3		
	Ports 03, 05, 07, ports 40 to 47	V_{IL}	–0.3	—	AVCC0 × 0.2		
	Ports other than above		–0.3	—	VCC × 0.2		
	Ports 03, 05, 07, ports 40 to 47	ΔV_T	AVCC0 × 0.01	—	—		
	Ports other than above		VCC × 0.01	—	—		
(Omitted)							

After correction

Table 50.4 DC Characteristics (2)

Conditions: 1.8 V ≤ VCC = VCC_USB < 2.7 V, 1.8 V ≤ AVCC0 < 2.7 V, VSS = AVSS0 = VSS_USB = 0 V, Ta = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	P12, P13, P16, P17, PB5 (5 V tolerant)		V_{IH}	VCC × 0.8	—	5.8	V	
	P14 to P15, P20 to P27, P33 to P37, P50 to P55, PA0 to PA7, PB0 to PB4, PB6, PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PH0 to PH3, PJ3, P30 to P32 (other than RTCICn pin), RES#			VCC × 0.8	—	VCC + 0.3		
	P03, P05, P07, P40 to P47			AVCC0 × 0.8	—	AVCC0 + 0.3		
	P30 to P32 (RTCICn pin)	When VCC is supplied		VCC × 0.8	—	VCC + 0.3		
		When VBATT is supplied		VBATT × 0.8	—	VBATT + 0.3		
	P12 to P17, P20 to P27, P33 to P37, P50 to P55, PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PH0 to PH3, PJ3, P30 to P32 (other than RTCICn pin), RES#		V_{IL}	–0.3	—	VCC × 0.2		
	P03, P05, P07, P40 to P47			–0.3	—	AVCC0 × 0.2		
	P30 to P32 (RTCICn pin)	When VCC is supplied		–0.3	—	VCC × 0.2		
		When VBATT is supplied		–0.3	—	VBATT × 0.2		
	P12 to P17, P20 to P27, P33 to P37, P50 to P55, PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PH0 to PH3, PJ3, P30 to P32 (other than RTCICn pin), RES#		ΔV_T	VCC × 0.01	—	—		
	P03, P05, P07, P40 to P47			AVCC0 × 0.01	—	—		
(Omitted)								