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RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RX*-A041A/E	Rev.	1.00
Title	Errata to RX210 Group Electrical Characteristics		Information Category	Technical Notification		
Applicable Product	RX210 Group	Lot No. All	Reference Document	RX210 Group User's Manual: Hardware Rev.1.10 (R01UH0037EJ0110)		

This document describes corrections to RX210 Group User's Manual: Hardware Rev.1.10.

Corrections are shown in red, and deletions are shown in strikethrough.

- Page 1340 of 1420

  Table 41.2 DC Characteristics (1) is corrected as follows:

  Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = -40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)	V_{IH}	VCC × 0.7	—	5.8	V	
	Ports 12, 13, 16, and 17 (5 V tolerant)		VCC × 0.8	—	5.8		
	~~Other pins~~ Ports 0, 14, 15, 2, 3, 4, 5, A, B, C, D, E, H, J, and RES#		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (except for SMBus)	V_{IL}	-0.3	—	VCC × 0.3		
	Other than RIIC input pin		-0.3	—	VCC × 0.2		
	RIIC input pin (except for SMBus)	ΔV_T	VCC × 0.05	—	—		
	Other than RIIC input pin		VCC × 0.1	—	—		
Input level voltage (except for Schmitt trigger input pins)	MD pin	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL, WAIT#~~, XCIN RSPI input pins~~		VCC × 0.8	—	VCC + 0.3		
	D0 to D15		VCC × 0.7	—	VCC + 0.3		
	RIIC input pin (SMBus)		2.1	—	VCC + 0.3		
	MD pin	V_{IL}	-0.3	—	VCC × 0.1		
	EXTAL, WAIT#~~, XCIN, RSPI input pins~~		-0.3	—	VCC × 0.2		
	D0 to D15		-0.3	—	VCC × 0.3		
	RIIC input pin (SMBus)		-0.3	—	0.8		

Table 41.3 DC Characteristics (2) is corrected as follows:

Conditions: VCC = AVCC0 = 1.62 to 2.7 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = -40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	Ports 12, 13, 16, and 17 (5 V tolerant)		V_{IH}	VCC × 0.8	—	5.8	V	
	~~Other pins~~ Ports 0, 14, 15, 2, 3, 4, 5, A, B, C, D, E, H, J, and RES#			VCC × 0.8	—	VCC + 0.3		
	All input pins		V_{IL}	-0.3	—	VCC × 0.2		
	~~All input pins~~ Ports 0, 1, 2, 3, 4, 5, A, B, C, D, E, H, and J	VCC ≥ 2.2V	ΔV_T	VCC × 0.05	—	—		
		VCC < 2.2V		VCC × 0.01	—	—		
	RES#			VCC × 0.1	—	—		
Input level voltage (except for Schmitt trigger input pins)	MD pin		V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL, WAIT#~~, XCIN RSPI input pins~~			VCC × 0.8	—	VCC + 0.3		
	D0 to D15			VCC × 0.7	—	VCC + 0.3		
	MD pin		V_{IL}	-0.3	—	VCC × 0.1		
	EXTAL, WAIT#~~, XCIN, RSPI input pins~~			-0.3	—	VCC × 0.2		
	D0 to D15			-0.3	—	VCC × 0.3		

- Page 1342 of 1420

Table 41.6 DC Characteristics (5) is corrected as follows:

Before correction

Item					Symbol	Typ.	Unit	Test Conditions
Current drawn *1	High-speed operating mode	Normal operating mode	No peripheral operating	ICLK = 50 MHz	I_{CC}	10	mA	Ta = 25°C
			All peripherals operating	ICLK = 50 MHz		28.5		
		Sleep mode		ICLK = 50 MHz		7.5		
		All-module clock stop mode				6.7		
		Increase during BGO *2				25		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state. BCLK, FCLK, and PCLK are ICLK divided by 64.

Note 2. This is the increase in current drawn if data are written to or erased from the ROM or the flash memory for data storage during program execution.

Corrections

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current *1	High-speed operating mode	Normal operating mode	No peripheral operation *2	ICLK = 50 MHz	I_{CC}	10	—	mA	
			All peripheral operation: Normal *3	ICLK = 50 MHz		31.5	—		
			All peripheral operation: Max. *3	ICLK = 50 MHz		—	55		
		Sleep mode	No peripheral operation	ICLK = 50 MHz		7.5	—		
			All peripheral operation: Normal	ICLK = 50 MHz		17.5	—		
		All-module clock stop mode		ICLK = 50 MHz		6.7	—		
		Increase during BGO operation *4				25	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are ICLK divided by 2.

Note 4. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.

Table 41.7 DC Characteristics (6) is corrected as follows:

Before correction

Item					Symbol	Typ.	Unit	Test Conditions
Current drawn *1	Medium-speed operating modes A and B	Normal operating mode	No peripheral operating	ICLK = 32 MHz	I_{CC}	7.0	mA	Ta = 25°C
				ICLK = 20 MHz		6.0		
			All peripherals operating	ICLK = 32 MHz		22.5		
				ICLK = 20 MHz		16.5		
		Sleep mode		ICLK = 32 MHz		5.0		
				ICLK = 20 MHz		4.6		
		All-module clock stop mode		ICLK = 32 MHz		4.5		
				ICLK = 20 MHz		4.3		
		Increase during BGO *2	Medium-speed operating mode A			25		
			Medium-speed operating mode B			20		
	Low-speed operating mode 1	Normal operating mode	No peripheral operating	ICLK = 1 MHz		0.68		
			All peripherals operating	ICLK = 1 MHz		2.4		
		Sleep mode		ICLK = 1 MHz		0.6		
		All-module clock stop mode				0.58		
	Low-speed operating mode 2	Normal operating mode	No peripheral operating	ICLK = 32 kHz		0.024		
			All peripherals operating	ICLK = 32 kHz		0.05		
		Sleep mode		ICLK = 32 kHz		0.02		
		All-module clock stop mode				0.018		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
BCLK, FCLK, and PCLK are ICLK divided by 64. (However, divided by 32 when ICLK = 20 MHz.)

Note 2. This is the increase in current drawn if data are written to or erased from the ROM or the flash memory for data storage during program execution.

Corrections

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current *1	Medium-speed operating modes 1A and 1B	Normal operating mode	No peripheral operation *2	ICLK = 32 MHz	I_{CC}	7.0	—	mA	
				ICLK = 20 MHz		6.0	—		
			All peripheral operation: Normal *3	ICLK = 32 MHz		26	—		
				ICLK = 20 MHz		18.5	—		
			All peripheral operation: Max. *3	ICLK = 32 MHz		—	40		
				ICLK = 20 MHz		—	30		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		5.0	—		
				ICLK = 20 MHz		4.6	—		
			All peripheral operation: Normal	ICLK = 32 MHz		15.5	—		
				ICLK = 20 MHz		12	—		
		All-module clock stop mode		ICLK = 32 MHz		4.5	—		
				ICLK = 20 MHz		4.3	—		
		Increase during BGO operation *4	Medium-speed operating mode 1A			25	—		
			Medium-speed operating mode 1B			20	—		
	Low-speed operating mode 1	Normal operating mode	No peripheral operation *5	ICLK = 1 MHz		0.68	—		
			All peripheral operation: Normal *6	ICLK = 1 MHz		2.4	—		
			All peripheral operation: Max. *6	ICLK = 1 MHz		—	7		
		Sleep mode	No peripheral operation	ICLK = 1 MHz		0.6	—		
			All peripheral operation: Normal	ICLK = 1 MHz		2	—		
		All-module clock stop mode				0.58	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation *7	ICLK = 32 kHz		0.024	—		
			All peripheral operation: Normal *8	ICLK = 32 kHz		0.05	—		
			All peripheral operation: Max. *8	ICLK = 32 kHz		—	3 *9		
		Sleep mode	No peripheral operation	ICLK = 32 kHz		0.02	—		
			All peripheral operation: Normal	ICLK = 32 kHz		0.04	—		
		All-module clock stop mode				0.018	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequencies are 64 MHz and 40 MHz, respectively. BCLK, FCLK, and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequencies are 64 MHz and 40 MHz, respectively. BCLK, FCLK, and PCLK are ICLK divided by 1.

Note 4. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.

Note 5. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 6. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.

Note 7. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are set to divided by 64.

Note 8. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are ICLK divided by 1.

Note 9. Value when the main clock continues oscillating at 12.5 MHz.

- Page 1348 of 1420

Table 41.10 DC Characteristics (9) is corrected as follows:

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VREFH = 1.8 to AVCC0, VREFH0 = 1.62 to AVCC0,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = -40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion	AI_{CC}	—	~~1.6~~ 1.0	~~3.0~~ 3.2	mA	
	During D/A conversion (per channel) *1		—	0.25	~~0.50~~ 0.75		
	Temperature sensor		—	60	200	µA	
	Waiting for A/D, D/A conversion (all units)		—	0.2	~~0.4~~ 5.0		
Reference power supply current	During A/D conversion	I_{REFH}, I_{REFH0}	—	~~0.01~~ 0.1	~~0.03~~ 0.2	mA	
	Waiting for A/D, D/A conversion (all units)		—	0.2	0.4	µA	

Note: • The values for A/D conversion apply when the sample and hold circuit is not in use.
Note 1. The reference power supply current is included in the power supply current value for D/A conversion.

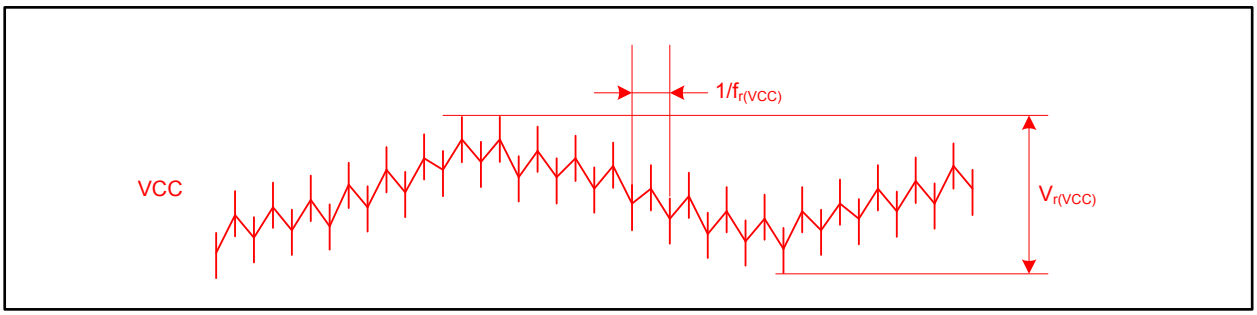
- Pages 1348 and 1349 of 1420

Table 41.12 DC Characteristics (11) is corrected as follows:

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = -40 to +105°C
The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (1.62 V). When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_{r(VCC)}$	—	—	10	kHz	Figure 41.18 VCC × 0.1 < $V_{r(VCC)}$ ≤ VCC × 0.2
		—	—	1	MHz	Figure 41.18 VCC × 0.05 < $V_{r(VCC)}$ ≤ VCC × 0.1
		—	—	10	MHz	Figure 41.18 $V_{r(VCC)}$ ≤ VCC × 0.05
Allowable voltage change rising/falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

Figure 41.9 Ripple Waveform is corrected as follows:



- Page 1353 of 1420

Table 41.24 BCLK Timing (3) is corrected as follows:

Conditions: VCC = AVCC0 = 1.62 to 1.8 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK = up to 12 MHz (BCLK pin output frequency = up to 6 MHz), T_a = -40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	~~166.7~~ 166.6	—	—	ns	Figure 41.10
BCLK pin output high pulse width*1	t_{CH}	42	—	—	ns	
BCLK pin output low pulse width*1	t_{CL}	42	—	—	ns	
BCLK pin output rising time	t_{Cr}	—	—	35	ns	
BCLK pin output falling time	t_{Cf}	—	—	35	ns	

Note: • Set high driving ability for the output port pin to be used for the BCLK pin function.
Note 1. When the EXTAL external clock input is used with divided by 1 (SCKCR.BCK[3:0] bits = 0000b and BCKCR.BCLKDIV bit = 0) to output from the BCLK pin, the above should be satisfied with a duty cycle of 45 to 55%.

Note 1 described above is also added to Table 41.22 BCLK Timing (1) and Table 41.23 BCLK Timing (2).

- Page 1354 of 1420

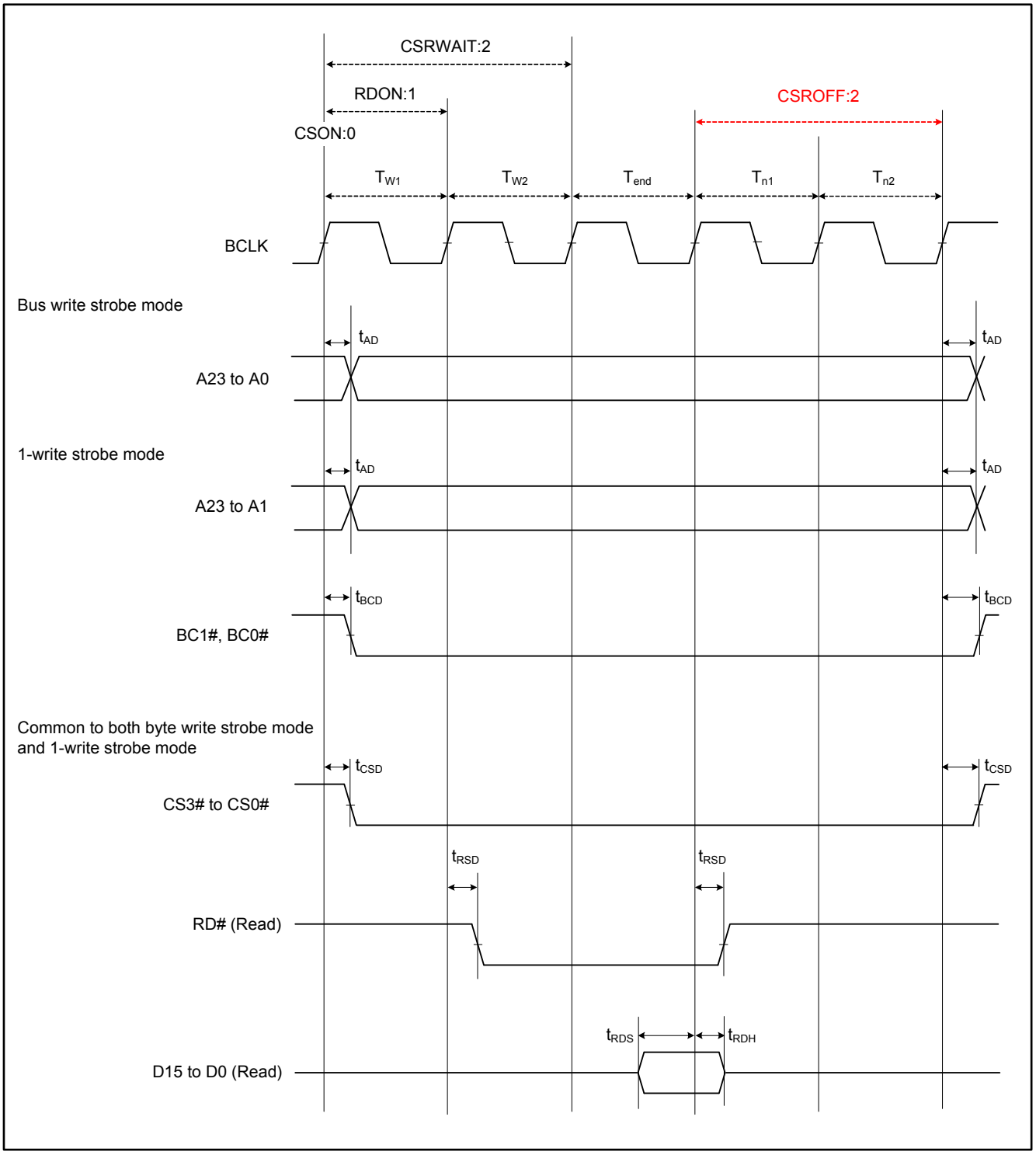
Sub-clock oscillation stabilization wait time is added to Table 41.25 Clock Timing.

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = -40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Sub-clock oscillation stabilization wait time*5	$t_{SUBOSCWT}$	4	—	—	s	Figure 41.19

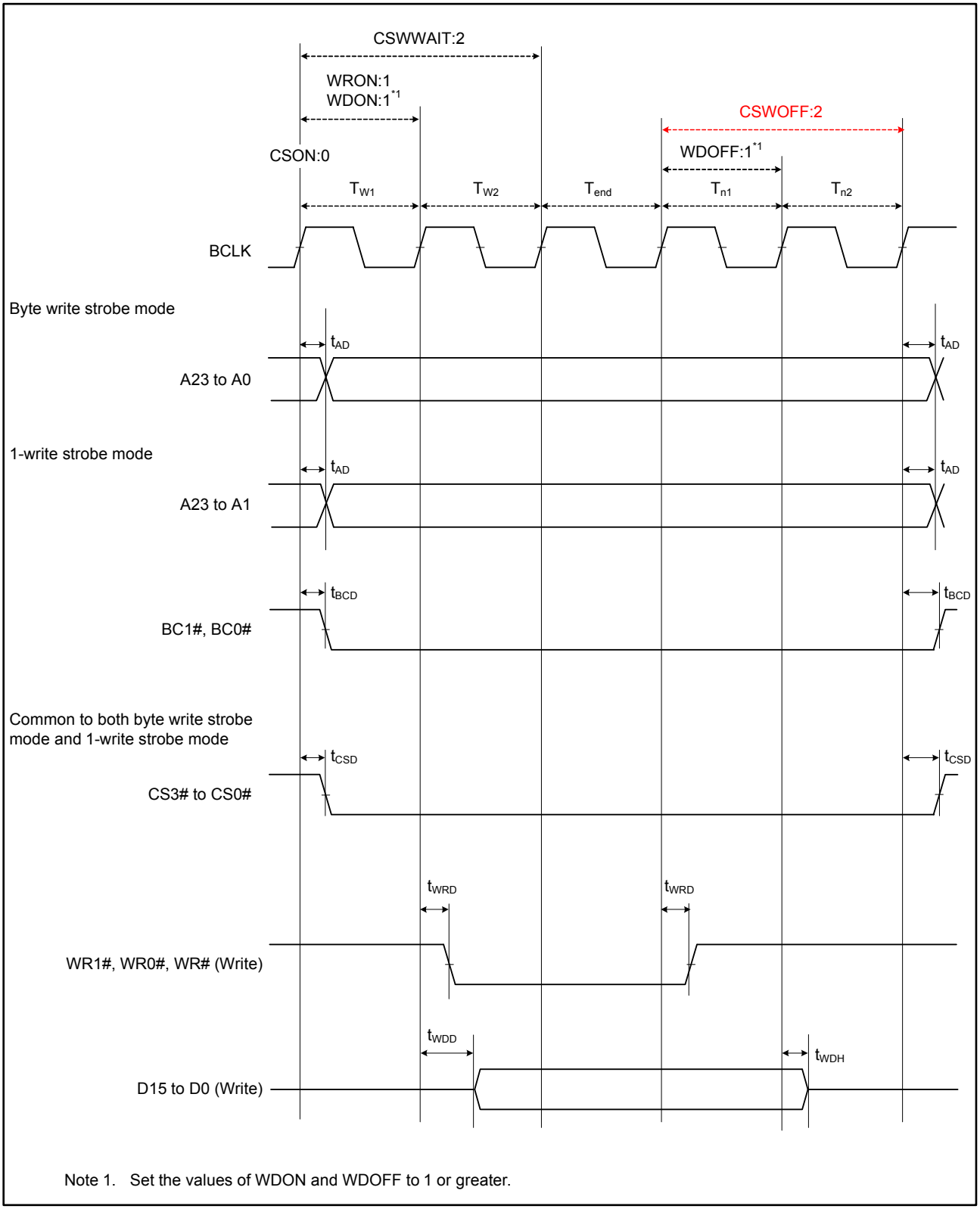
- Page 1364 of 1420

Description of CSROFF in Figure 41.26 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized) is corrected as follows:



- Page 1365 of 1420

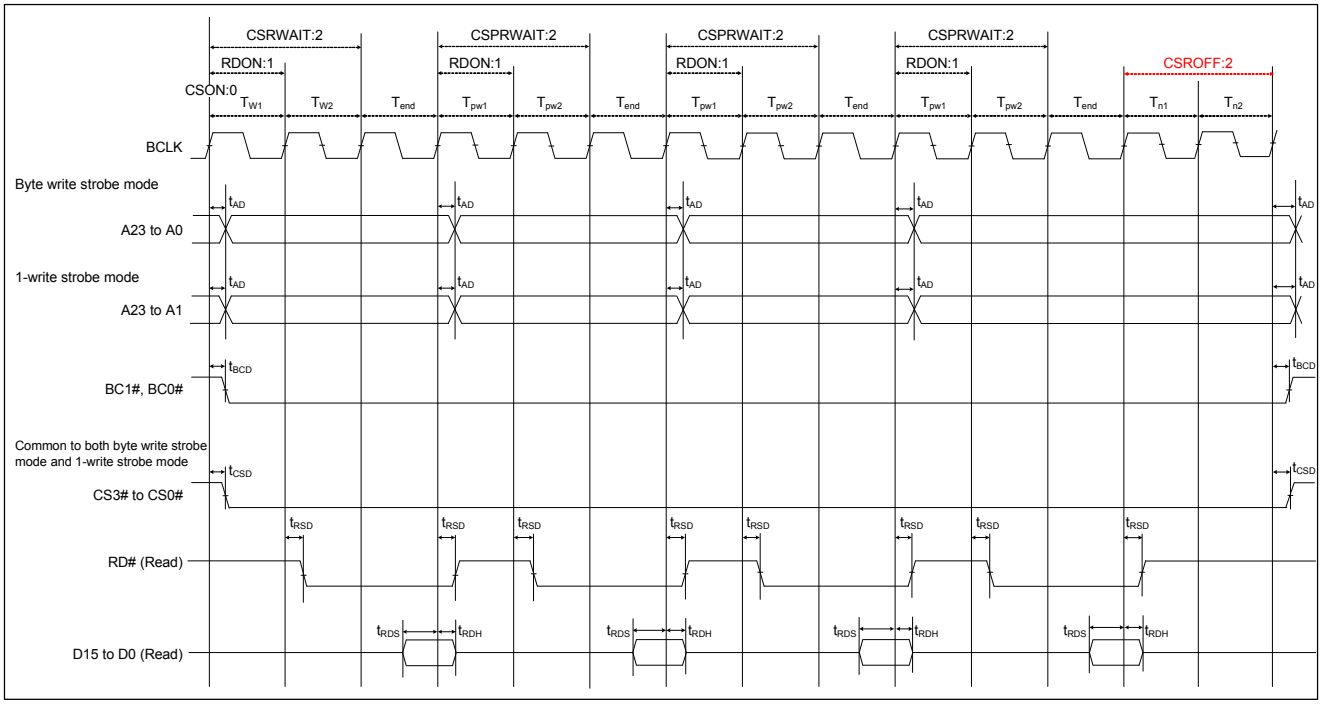
Description of CSWOFF in Figure 41.27 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized) is corrected as follows:



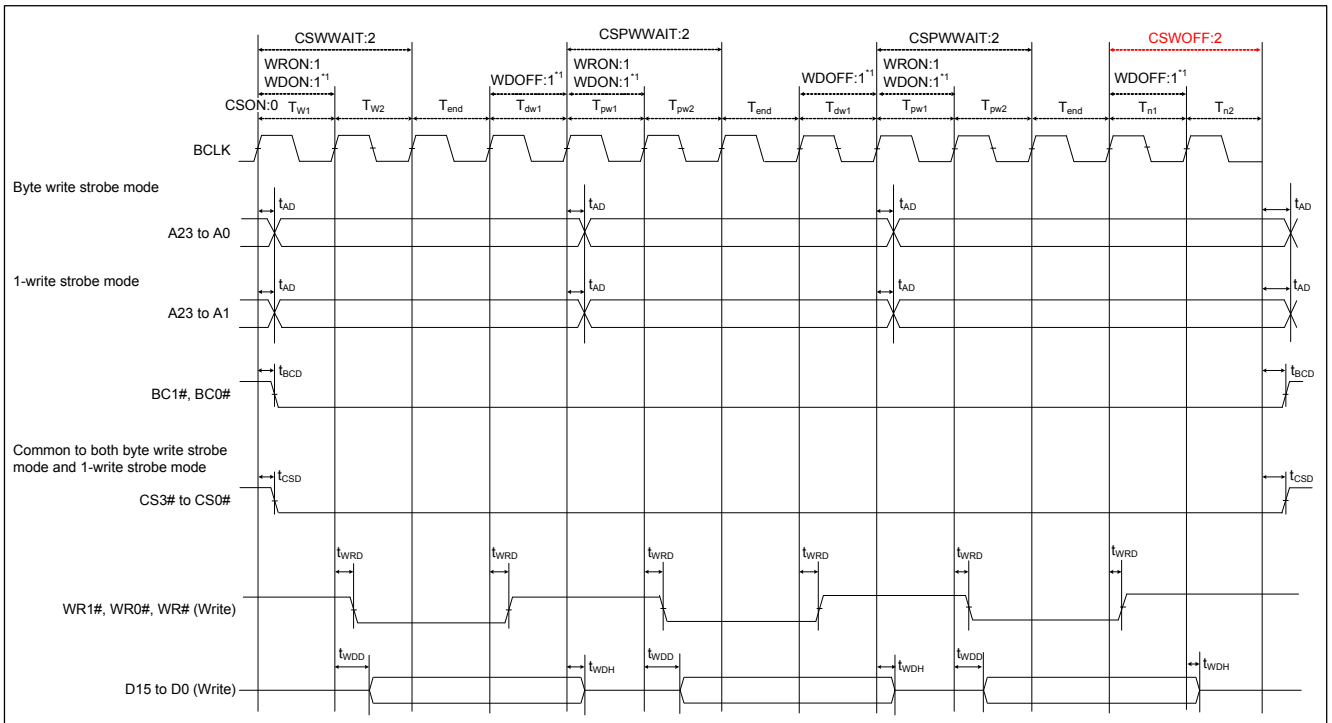
Note 1. Set the values of WDON and WDOFF to 1 or greater.

- Page 1366 of 1420

Description of CSROFF in Figure 41.28 External Bus Timing/Page Read Cycle (Bus Clock Synchronized) is corrected as follows:



Description of CSWOFF in Figure 41.29 External Bus Timing/Page Write Cycle (Bus Clock Synchronized) is corrected as follows:



Note 1. Set the values of WDON and WDOFF to 1 or greater.

- Page 1382 of 1420

Table 41.40 A/D Conversion Characteristics (1) is corrected as follows:

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, ~~VREFH =~~ 2.7 V ≤ VREFH0 = (AVCC0 - 0.9 V) to AVCC0[*4],
VSS = AVSS0 = VREFL = VREFL0 = 0 V, fPCLKD = 1 to 50 MHz, T_a = -40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		—	—	12	Bit	
Conversion time[*1] (Operation at fPCLKD = 50 MHz)[*3]	Permissible signal source impedance (Max.) = 0.5 kΩ	1.0 (0.4)[*2]	—	—	μs	Sampling in 20 states
	Permissible signal source impedance (Max.) = 1 kΩ	1.1 (0.5)[*2]	—	—		Sampling in 25 states
	Permissible signal source impedance (Max.) = 5 kΩ	1.5 (0.9)[*2]	—	—		Sampling in 45 states
Analog input capacitance		—	—	30	pF	
Offset error		—	±0.5	±4.5	LSB	High-precision channel
				±7.5		Normal-precision channel
Full-scale error		—	±0.75	±4.5	LSB	High-precision channel
				±7.5		Normal-precision channel
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel
		—	±1.25	±8.0	LSB	Normal-precision channel
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.0	±3.0	LSB	

Note: • PCLKD must be set to 40 MHz or lower when HOCO is to be selected as the A/D conversion clock. The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, fullscale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Note 3. The lower-limit frequency of PCLKD is 1 MHz.

Note 4. When using the temperature sensor, use it when AVCC0 = VREFH0.

- Page 1383 of 1420

Table 41.43 A/D Conversion Characteristics (2) is corrected as follows:

Conditions: VCC = AVCC0 = 1.8 to ~~2.7~~3.6 V, ~~VREFH =~~ VREFH0 = (AVCC0 - 0.9 V) to AVCC0, VREFH0 = 1.8 to 2.7 V[*4],
VSS = AVSS0 = VREFL = VREFL0 = 0 V, fPCLKD = 1 to 32 MHz, T_a = -40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		—	—	12	Bit	
Conversion time[*1] (Operation at fPCLKD = 25 MHz)[*3]	Permissible signal source impedance (Max.) = 1 kΩ	2.0 (0.8)[*2]	—	—	μs	Sampling in 20 states
	Permissible signal source impedance (Max.) = 5 kΩ	2.2 (1.0)[*2]	—	—		Sampling in 25 states
Analog input capacitance		—	—	30	pF	
Offset error		—	±0.5	±7.5	LSB	
Full-scale error		—	±1.25	±7.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	
DNL differential nonlinearity error		—	±1.25	—	LSB	
INL integral nonlinearity error		—	±1.5	±3.0	LSB	

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Note 3. The lower-limit frequency of PCLKD is 1 MHz.

Note 4. When using the temperature sensor, use it when AVCC0 = VREFH0.

Table 41.44 A/D Conversion Characteristics (3) is corrected as follows:

Conditions: VCC = AVCC0 = 1.62 to 1.8 V, ~~VREFH =~~ VREFH0 = ~~(AVCC0 – 0.9 V) to~~ AVCC0,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, fPCLKD = 1 to 16 MHz, T_a = -40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at fPCLKD = 12.5 MHz)*3	Permissible signal source impedance (Max.) = 1 kΩ	3.36 (0.96) *2	—	—	µs	Sampling in 12 states
	Permissible signal source impedance (Max.) = 5 kΩ	3.6 (1.2) *2	—	—		Sampling in 15 states
Analog input capacitance		—	—	30	pF	
Offset error		—	±0.5	±7.5	LSB	
Full-scale error		—	±1.25	±7.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±2.75	±8.0	LSB	
DNL differential nonlinearity error		—	±1.25	—	LSB	
INL integral nonlinearity error		—	±1.25	±3.0	LSB	

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Note 3. The lower-limit frequency of PCLKD is 1 MHz.

- Page 1384 of 1420

Conditions in Table 41.47 Temperature Sensor Characteristics are corrected as follows:

Conditions: VCC = AVCC0 = VREFH0 = 1.8 to 5.5 V, ~~VREFH = VREFH0 = (AVCC0 – 0.9 V) to AVCC0,~~
VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = -40 to +105°C

- Page 1391 of 1420

Table 41.53 ROM (Flash Memory for Code Storage) Characteristics (2): high-speed operating mode, medium-speed operating mode A is corrected as follows:
Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V Temperature range for the programming/erasure operation: T_a = -40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{P2}	—	0.52	4.8	—	~~0.5~~ 0.19	2.5	ms
	8 bytes	t_{P8}	—	0.52	4.9	—	~~0.5~~ 0.19	2.5	
	128 bytes	t_{P128}	—	1.50	10.7	—	~~1.0~~ 0.57	4.8	
Programming time when N_{PEC} > 100 times	2 bytes	t_{P2}	—	0.61	5.7	—	0.23	3.0	ms
	8 bytes	t_{P8}	—	0.61	6.2	—	0.23	3.2	
	128 bytes	t_{P128}	—	1.71	13.2	—	0.65	6.0	
Erasure time when N_{PEC} ≤ 100 times	2 Kbytes	t_{E2K}	—	17.0	92.9	—	~~16~~ 11.0	29	ms
Erasure time when N_{PEC} > 100 times	2 Kbytes	t_{E2K}	—	20.8	195.8	—	13.5	60	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	0.9	—	—	0.8	ms
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	0.9	—	—	0.8	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	0.9	—	—	0.8	ms
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	0.9	—	—	0.8	ms
FCU reset time		t_{FCUR}	20 µs or longer and FCLK × 6 or greater	—	—	20 µs or longer and FCLK × 6 or greater	—	—	µs

- Page 1392 of 1420

Table 41.54 ROM (Flash Memory for Code Storage) Characteristics (3): medium-speed operating mode B is corrected as follows:
Conditions: VCC = AVCC0 = 1.62 to 3.6 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V Temperature range for the programming/erasure operation: T_a = -40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{P2}	—	0.69	6.0	—	~~0.8~~ 0.30	3.5	ms
	8 bytes	t_{P8}	—	0.69	6.0	—	~~0.8~~ 0.30	3.5	
	128 bytes	t_{P128}	—	1.76	14.2	—	~~1.6~~ 0.85	8.3	
Programming time when N_{PEC} > 100 times	2 bytes	t_{P2}	—	0.81	7.1	—	0.35	4.2	ms
	8 bytes	t_{P8}	—	0.81	7.6	—	0.35	4.5	
	128 bytes	t_{P128}	—	1.99	17.5	—	0.96	10	
Erasure time when N_{PEC} ≤ 100 times	2 Kbytes	t_{E2K}	—	24.5	113.7	—	~~27~~ 19.0	46	ms
Erasure time when N_{PEC} > 100 times	2 Kbytes	t_{E2K}	—	29.8	225.8	—	23.2	~~90~~ 90 (1000 times ≥ N_{PEC} > 100 times), 98 (10000 times ≥ N_{PEC} > 1000 times)	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	1.7	—	—	1.6	ms
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	1.7	—	—	1.6	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	1.7	—	—	1.6	ms
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.6	ms
FCU reset time		t_{FCUR}	20 µs or longer and FCLK × 6 or greater	—	—	20 µs or longer and FCLK × 6 or greater	—	—	µs

Note 1. The operating frequency is 20 MHz (max.) when the voltage is in the range from 1.62 V to less than 1.8 V.

- Page 1393 of 1420

Table 41.56 E2 DataFlash Characteristics (2): high-speed operating mode, medium-speed operating mode A is corrected as follows:

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V Temperature range for the programming/erasure operation: T_a = -40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{DP2}	—	0.40	4.4	—	~~0.3~~ 0.16	2.0	ms
	8 bytes	t_{DP8}	—	0.45	5.1	—	~~0.4~~ 0.17	2.2	
Programming time when N_{PEC} > 100 times	2 bytes	t_{DP2}	—	0.62	6.4	—	0.25	3.0	ms
	8 bytes	t_{DP8}	—	0.69	7.5	—	0.26	3.2	
Erasure time when N_{PEC} ≤ 100 times	128 byte	t_{DE128}	—	5.6	27.1	—	~~4.5~~ 2.8	8	ms
Erasure time when N_{PEC} > 100 times	128 byte	t_{DE128}	—	6.8	45.1	—	3.4	12	ms
Blank check time	2 bytes	t_{DBC2}	—	—	98	—	—	35	µs
	2 Kbytes	t_{DBC2K}	—	—	16	—	—	2.5	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{DSPD}	—	—	0.9	—	—	0.8	ms
First suspend delay time during programming (in suspend priority mode)		t_{DSPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{DSPSD2}	—	—	0.9	—	—	0.8	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{DSED}	—	—	0.9	—	—	0.8	ms
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	0.9	—	—	0.8	ms

- Page 1394 of 1420

Table 41.57 E2 DataFlash Characteristics (3): medium-speed operating mode B is corrected as follows:

Conditions: VCC = AVCC0 =1.62 to 3.6 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V Temperature range for the programming/erasure operation: T_a = -40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{DP2}	—	0.52	5.1	—	~~0.6~~ 0.24	2.8	ms
	8 bytes	t_{DP8}	—	0.57	6.0	—	~~0.6~~ 0.26	3.2	
Programming time when N_{PEC} > 100 times	2 bytes	t_{DP2}	—	0.77	7.6	—	0.36	4.2	ms
	8 bytes	t_{DP8}	—	0.84	8.8	—	0.38	4.5	
Erasure time when N_{PEC} ≤ 100 times	128 byte	t_{DE128}	—	6.8	32.5	—	~~7~~ 4.4	12	ms
Erasure time when N_{PEC} > 100 times	128 byte	t_{DE128}	—	8.2	51.4	—	5.3	17	ms
Blank check time	2 bytes	t_{DBC2}	—	—	110	—	—	40	µs
	2 Kbytes	t_{DBC2K}	—	—	16.3	—	—	2.6	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{DSPD}	—	—	1.7	—	—	1.6	ms
First suspend delay time during programming (in suspend priority mode)		t_{DSPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{DSPSD2}	—	—	1.7	—	—	1.6	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{DSED}	—	—	1.7	—	—	1.6	ms
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	220	—	—	~~12~~ 120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	1.7	—	—	1.6	ms

Note 1. The operating frequency is 20 MHz (max.) when the voltage is in the range from 1.62 V to less than 1.8 V.