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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A0258A/E	Rev.	1.00
Title	Errata to the RX140 Group User's Manual: Hardware Rev.1.00		Information Category	Technical Notification		
Applicable Product	RX140 Group	Lot No. All	Reference Document	RX140 Group User's Manual: Hardware Rev.1.00 (R01UH0905EJ0100)		

This document describes corrections to the RX140 Group User's Manual: Hardware Rev.1.00.

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The descriptions in Low power design and architecture in Features are corrected as follows.

Before correction

■ Low power design and architecture

- Operation from a single 1.8-V to 5.5-V supply
- Four low power consumption modes
- Low power timer (LPT) that operates during the software standby state
- Supply current
  High-speed operating mode: 58 µA/MHz
  Supply current in software standby mode: 0.21 µA (typ. T_a = 25°C)
- Recovery time from software standby mode: 6.2 µs (Clock Source: HOCO 32 MHz)

After correction

■ Low power design and architecture

- Operation from a single 1.8-V to 5.5-V supply
- Four low power consumption modes
- Low power timer (LPT) that operates during the software standby state
- Supply current
  High-speed operating mode: 58 µA/MHz
  Supply current in software standby mode: 0.25 µA (typ.) (T_a = 25°C)
- Recovery time from software standby mode: 6.2 µs (typ.) (Clock Source: HOCO 32 MHz, T_a = 25°C)

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The setting for the CTSU internal clock is added to the description of the CKOSEL[3:0] bits in section 9.2.15, CLKOUT Output Control Register (CKOCR) as follows.

Before correction

Bit	Symbol	Bit Name	Description	R/W
b11 to b8	CKOSEL[3:0]	CLKOUT Output Source Select	b11 b8 0 0 0 0: LOCO clock 0 0 0 1: HOCO clock 0 0 1 0: Main clock oscillator 0 0 1 1: Sub-clock oscillator 0 1 0 0: PLL Settings other than above are prohibited.	R/W

After correction

Bit	Symbol	Bit Name	Description	R/W
b11 to b8	CKOSEL[3:0]	CLKOUT Output Source Select	b11 b8 0 0 0 0: LOCO clock 0 0 0 1: HOCO clock 0 0 1 0: Main clock oscillator 0 0 1 1: Sub-clock oscillator 0 1 0 0: PLL 1 0 0 0: CTSU internal clock Settings other than above are prohibited.	R/W

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The module and interrupt symbols for the true random number generator in Table 14.3, Interrupt Vector Table (3/6) are corrected as follows.

Before correction

Table 14.3 Interrupt Vector Table (3/6)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Interrupt Detection Method	CPU Interrupt	Start DTC	SSBY Return	IER	IPR	DTCER
				(Omitted)						
TRNG	TRNGRDI	113	01C4h	Edge	✓	✓	N/A	IER0E.IEN1	IPR113	DTCER113
				(Omitted)						

After correction

Table 14.3 Interrupt Vector Table (3/6)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Interrupt Detection Method	CPU Interrupt	Start DTC	SSBY Return	IER	IPR	DTCER
				(Omitted)						
RNG	RNGRDI	113	01C4h	Edge	✓	✓	N/A	IER0E.IEN1	IPR113	DTCER113
				(Omitted)						

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The descriptions in section 35.8.3, A/D Conversion Restarting Timing and Termination Timing are modified as follows.

Before correction

It takes a maximum of six ADCLK cycles for the idle analog unit of the 12-bit A/D converter to be restarted by setting the ADCSR.ADST bit to 1. It takes a maximum of three ADCLK cycles for the operating analog unit of the 12-bit A/D converter to be terminated by setting the ADCSR.ADST bit to 0.

After correction

It takes a maximum of six ADCLK cycles for the idle analog unit of the 12-bit A/D converter to be restarted by setting the ADCSR.ADST bit to 1. It takes a maximum of three ADCLK cycles (1 PCLKB + 2 ADCLK when ADCLK is faster than PCLKB (PCLKB to ADCLK frequency ratio = 1:2)) for the operating analog unit of the 12-bit A/D converter to be terminated by setting the ADCSR.ADST bit to 0.

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Conditions of Table 42.12, DC Characteristics (9) are corrected as follows.

Before correction

Table 42.12 DC Characteristics (9)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power-on VCC rising gradient	At normal startup*1	SrVCC	0.02	—	20	ms/V	
	During fast startup time*2		0.02	—	2		
	Voltage monitoring 0 reset enabled at startup*3, *4		0.02	—	—		

After correction

Table 42.12 DC Characteristics (9)

Conditions: 0 V ≤ VCC ≤ 5.5 V, 0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power-on VCC rising gradient	At normal startup*1	SrVCC	0.02	—	20	ms/V	
	During fast startup time*2		0.02	—	2		
	Voltage monitoring 0 reset enabled at startup*3, *4		0.02	—	—		

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PJ7 in the second row of Permissible output low current in Table 42.15, Permissible Output Currents (2) is corrected to PG7 as follows.

Before correction

Table 42.15 Permissible Output Currents (2)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Max.	Unit
Permissible output low current	Total of P03 to P07, P40 to P47, PJ6, PJ7	ΣI_{OL}	30	mA
	Total of P12 to P17, P20, P21, P26 to P27, P30 to P32, P34 to P37, PH2, PH3, PJ1, PJ7		30	
	Total of P54, P55, PB0 to PB7, PC2 to PC7, PH0, PH1		30	
	Total of PA0 to PA6, PD0 to PD2, PE0 to PE5		30	
	Total of all output pins		60	

After correction

Table 42.15 Permissible Output Currents (2)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Max.	Unit
Permissible output low current	Total of P03 to P07, P40 to P47, PJ6, PJ7	ΣI_{OL}	30	mA
	Total of P12 to P17, P20, P21, P26 to P27, P30 to P32, P34 to P37, PG7, PH2, PH3, PJ1		30	
	Total of P54, P55, PB0 to PB7, PC2 to PC7, PH0, PH1		30	
	Total of PA0 to PA6, PD0 to PD2, PE0 to PE5		30	
	Total of all output pins		60	

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Note 5 is added to HOCO oscillation frequency error in Table 42.30, Clock Timing as follows.

Before correction

Table 42.30 Clock Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
(Omitted)						
HOCO oscillation frequency	f_{HOCO}	—	24, 32, 48	—	MHz	
HOCO oscillation frequency error	Δf_{HOCO}	—	—	±1.5	%	T_a = –40 to –20°C
		—	—	±1.0		T_a = –20 to +85°C
		—	—	±2.0		T_a = +85 to +105°C
HOCO clock oscillation stabilization time	t_{HOCO}	—	—	4.95	μs	Figure 42.13
(Omitted)						

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating).
Note 2. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that is has become 1, and then start using the main clock.
Note 3. Reference value when a 32.768-kHz resonator is used.
After changing the setting of the SOSCCR.SOSTP bit so that the sub-clock oscillator operates, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturer-recommended value has elapsed.
Note 4. Only 32.768-kHz can be used.

After correction

Table 42.30 Clock Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
(Omitted)						
HOCO oscillation frequency	f_{HOCO}	—	24, 32, 48	—	MHz	
HOCO oscillation frequency error*5	Δf_{HOCO}	—	—	±1.5	%	T_a = –40 to –20°C
		—	—	±1.0		T_a = –20 to +85°C
		—	—	±2.0		T_a = +85 to +105°C
HOCO clock oscillation stabilization time	t_{HOCO}	—	—	4.95	μs	Figure 42.13
(Omitted)						

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating).
Note 2. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that is has become 1, and then start using the main clock.
Note 3. Reference value when a 32.768-kHz resonator is used.
After changing the setting of the SOSCCR.SOSTP bit so that the sub-clock oscillator operates, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturer-recommended value has elapsed.
Note 4. Only 32.768-kHz can be used.
Note 5. Accuracy at production test.

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The typical value of INL integral nonlinearity error in Table 42.54, A/D Conversion Characteristics (5) is modified as follows.

Before correction

Table 42.54 A/D Conversion Characteristics (5)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ VREFH0 = AVCC0 ≤ 5.5 V*1, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C,
signal source impedance = 5 kΩ
Reference voltage = VREFH0

Item	Min.	Typ.	Max.	Unit	Test Conditions
(Omitted)					
INL integral nonlinearity error	—	±1.0	±3.5	LSB	

After correction

Table 42.54 A/D Conversion Characteristics (5)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ VREFH0 = AVCC0 ≤ 5.5 V*1, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C,
signal source impedance = 5 kΩ
Reference voltage = VREFH0

Item	Min.	Typ.	Max.	Unit	Test Conditions
(Omitted)					
INL integral nonlinearity error	—	±1.5	±3.5	LSB	

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The unit for DataFlash STOP recovery time in Table 42.69, E2 DataFlash Characteristics (2): high-speed operating mode is corrected as follows.

Before correction

Table 42.69 E2 DataFlash Characteristics (2): high-speed operating mode

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item	Symbol	FCLK = 1 MHz			FCLK = 32 MHz			FCLK = 48MHz			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
(Omitted)											
DataFlash STOP recovery time	t_{DSTOP}	250	—	—	250	—	—	250	—	—	µs

After correction

Table 42.69 E2 DataFlash Characteristics (2): high-speed operating mode

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item	Symbol	FCLK = 1 MHz			FCLK = 32 MHz			FCLK = 48MHz			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
(Omitted)											
DataFlash STOP recovery time	t_{DSTOP}	250	—	—	250	—	—	250	—	—	ns