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RENESAS TECHNICAL UPDATE

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Title	Errata to R32C/161 Group Hardware Manual		Information Category	Technical Notification		
Applicable Product	R32C/161 Group	Lot No.	Reference Document	R32C/161 Group Hardware Manual Rev. 1.02 (REJ09B0517-0102)		

This document describes corrections to the R32C/161 Group Hardware Manual, Rev. 1.02.
The corrections are indicated in red in the list below.

- Page 10 of 586, description “Output of the clock with the same frequency as fC, f8, or f32” in the description for the Clock output in Table 1.6 is corrected as follows:
  “Output of the clock with the same frequency as low speed clocks, f8, or f32”

- Page 13 of 586, register symbol “R3R0” in line 3 of 2.1.1 is corrected as follows:
  “R3R1”

- Page 23 of 586, description of register name “Group 0 Timer Measurement Prescaler Register 6/7” in Table 4.7 is corrected as follows:
  “Group 0 Time Measurement Prescaler Register 6/7”

- Page 28 of 586, description of register name “UART2 Transmission/Receive Mode Register” in Table 4.12 is corrected as follows:
  “UART2 Transmit/Receive Mode Register”

- Page 28 of 586, description of register name “Increment/Decrement Counting Select Register” in Table 4.12 is corrected as follows:
  “Increment/Decrement Select Register”

- Page 35 of 586, reset value of the IFS0 register “X000 X000b” in Table 4.19 is corrected as follows:
  “X0X0 X000b”

- Page 38 of 586, description of register name “External Interrupt Source Select Register 0” in Table 4.22 is corrected as follows:
  “External Interrupt Request Source Select Register 0”

- Pages 52 to 53 and 66 to 67 of 586, description of register name “CAN1/0 Acceptance Mask Register 0/1/2/3/4/5/6/7” in Tables 4.36 to 4.37 and 4.50 to 4.51 is corrected as follows:
  “CAN1/0 Mask Register 0/1/2/3/4/5/6/7”

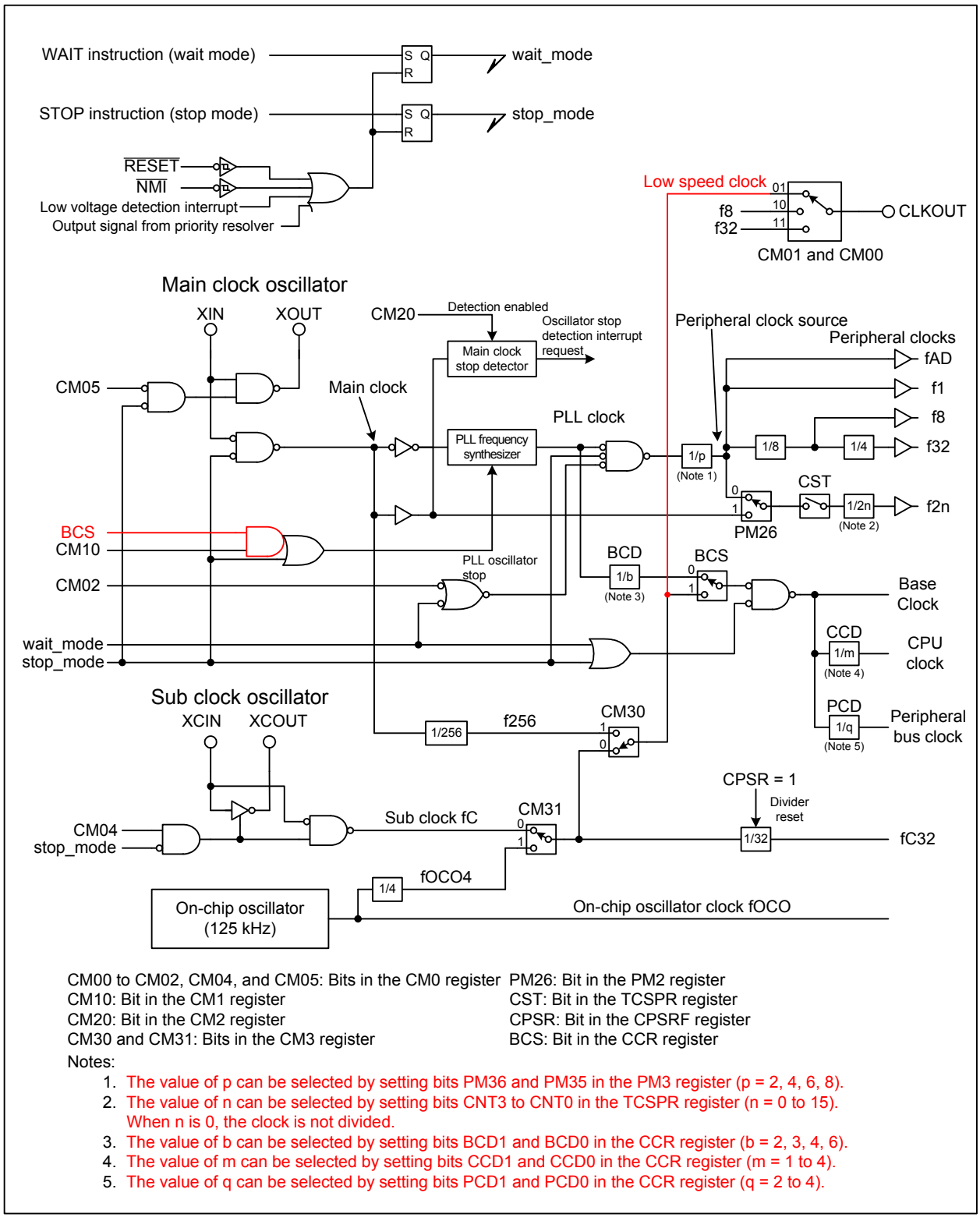
- Pages 55 and 69 of 586, descriptions of register names “CAN1/0 Reception Error Count Register” and “CAN1/0 Transmission Error Count Register” in Tables 4.39 and 4.53 are corrected as follows:
  “CAN1/0 Receive Error Count Register” and “CAN1/0 Transmit Error Count Register”

•Pages 55 and 69 of 586, reset value “XXXX XX00b” for registers C1MSMR and C0MSMR in Tables 4.39 and 4.53 is corrected as follows:
“0000 0000b”

•Page 77 of 586, descriptions for the VDEN bit in Figure 6.4 are modified as follows:

Bit Symbol	Bit Name	Function	RW
VDEN	Low Voltage Detector Enable Bit	0: Low voltage detector disabled 1: Low voltage detector enabled	RW

•Page 82 of 586, Figure 7.1 is corrected as follows:



CM00 to CM02, CM04, and CM05: Bits in the CM0 register
CM10: Bit in the CM1 register
CM20: Bit in the CM2 register
CM30 and CM31: Bits in the CM3 register
PM26: Bit in the PM2 register
CST: Bit in the TCSPR register
CPSR: Bit in the CPSRF register
BCS: Bit in the CCR register

Notes:
1. The value of p can be selected by setting bits PM36 and PM35 in the PM3 register (p = 2, 4, 6, 8).
2. The value of n can be selected by setting bits CNT3 to CNT0 in the TCSPR register (n = 0 to 15). When n is 0, the clock is not divided.
3. The value of b can be selected by setting bits BCD1 and BCD0 in the CCR register (b = 2, 3, 4, 6).
4. The value of m can be selected by setting bits CCD1 and CCD0 in the CCR register (m = 1 to 4).
5. The value of q can be selected by setting bits PCD1 and PCD0 in the CCR register (q = 2 to 4).

Figure 7.1 Clock Generation Circuitry

•Page 83 of 586, descriptions of Notes 2 and 6 in Figure 7.2 are corrected as follows:
Note 2: "The divide ratios of the base clock and peripheral bus clock should not be changed simultaneously. Doing so may cause the peripheral bus clock frequency to go over the maximum operating frequency." ("To increase the base clock frequency, the divide ratio of the peripheral bus clock should be increased before reducing the divide ratio of base clock." is deleted)
Note 6: "To use these low speed clocks, select one of them by setting bits CM31 and CM30 in the CM3 register and then set the BCS bit to 1."

•Pages 84, 98, 105, and 108 of 586, description "fC" for bits CM00 and CM01 in Figure 7.3, Section 7.6, Tables 7.3, 7.4, and 7.6 is corrected as follows:
Figure 7.3: "0 1 : Output a low speed clock"
Section 7.6: "Low speed clocks, f8, and f32 can be output from the CLKOUT pin."
Table 7.3: "Output a low speed clock"
Tables 7.4 and 7.6: "When a low speed clock is selected"

•Page 84 of 586, the following description is added to Figure 7.3 as Note 7:
"Set this bit before activating the watchdog timer. When rewriting this bit while the watchdog timer is running, set it immediately after writing to the WDTS register."

•Page 85 of 586, descriptions of bit names "PLL Clock Oscillator Stop Bit" and "XIN-XOUT Drive Power Select Bit" in Figure 7.4 are modified as follows:
"PLL Oscillator Stop Bit" and "XIN-XOUT Drive Strength Select Bit"

•Page 85 of 586, description of Note 2 in Figure 7.4 is corrected as follows:
"When the BCS bit in the CCR register is 0 (PLL clock selected as base clock source), the PLL frequency synthesizer does not stop oscillating even if the CM10 bit is set to 1."

•Page 85 of 586, the following description is added to Figure 7.4 as Note 4:
"This bit becomes 1 when the main clock is stopped. When setting to 0, rewrite it after the main clock oscillation is fully stabilized."

•Page 85 of 586, bit symbol "CM02" in Note 3 of Figure 7.5 is corrected as follows:
"CM20"

•Page 86 of 586, description of Note 1 in Figure 7.6 is modified as follows:
"Rewrite this register after setting the PRC27 bit in the PRCR2 register to 1 (write enabled) and while the BCS bit in the CCR register is 0 (PLL clock)."

•Page 88 of 586, descriptions in Note 3 in Figure 7.9 are modified as follows:
"CM05 bit in the CM0 register (main clock oscillator enabled/disabled)
CM10 bit in the CM1 register (PLL oscillator enabled/disabled)"

•Page 88 of 586, the following description is added to Figure 7.9 as Note 6:
"Stop all the peripherals that use f2n before rewriting this bit."

•Page 89 of 586, the following description is added to Note 1 in Figure 7.10:
"Stop all the peripherals that use fAD, f1, f8, f32, or f2n (when the clock source is the peripheral clock source) to rewrite this register."

•Page 93 of 586, descriptions for the SEO bit in Figure 7.15 are modified as follows:

Bit Symbol	Bit Name	Function	RW
SEO	Self-oscillating Setting Bit	0: PLL lock-in 1: Self-oscillating	RW

•Page 93 of 586, the following description is added to Figure 7.16 as Note 1:
"This register is reset after setting the SEO bit in the PLC1 register to 1 (self-oscillating). Stopping the main clock or PLL prevents the register from updating."

•Page 95 of 586, description of the last paragraph in 7.1.4 is modified as follows:
"When the CSPM bit in the OFS area is 1, the on-chip oscillator clock is stopped after a reset. It starts running if the CM31 bit in the CM3 register or the PM22 bit in the PM2 register is set to 1. It is not necessary to wait for stabilization because the on-chip oscillator instantly starts oscillating."

•Page 96 of 586, description "(Refer to Figure 7.18 "State Transition (when the sub clock is used)")" is deleted from 7.2.

•Page 96 of 586, description of the second paragraph in 7.2.1 is modified as follows:
"When the main clock oscillator resumes running after an oscillator stop is detected, the PLL clock frequency may temporarily exceed the preset value before the PLL frequency synthesizer oscillation stabilizes. As soon as an oscillator stop is detected, the main clock oscillator should be stopped from resuming (set the CM05 bit in the CM0 register to 1) or the divide ratios of the base clock and peripheral clock source should be increased by a program. They can be set using bits BCD1 and BCD0 in the CCR register and bits PM36 and PM35 in the PM3 register."

•Page 100 of 586, description "f(XPLL)" in the third row of Figure 7.18 is corrected as follows:
"f(PLL)"

•Page 101 of 586, description "CM0 = 1" in the fourth row of Figure 7.19 is corrected as follows:
"CM05 = 1"

•Page 102 of 586, descriptions "CM31 = 1" in the first row and "CM10 = 0" for "Low speed mode" in the second row of Figure 7.20 are corrected as follows:
"CM31 = 0" and "CM10 = 1"

•Page 104 of 586, description of 7.7.2 is modified as follows:
"The base clock stops in wait mode so that clocks generated by the base clock, the CPU clock and peripheral bus clock, stop running as well. Thus the CPU and watchdog timer, operated by these two clocks, also stop. However, the watchdog timer continues operating when the PM22 bit in the PM2 register is 1 (on-chip oscillator selected as count source for the watchdog timer). Since the main clock, sub clock, PLL clock, and on-chip oscillator clock continue running, peripheral functions using these clocks also continue operating."

•Page 107 of 586, description in 7.7.3 is corrected as follows:
"In stop mode, all of the clocks, except for those that are protected, stop running. That is, the CPU and peripherals, operated by the CPU clock and peripheral clock, also stop. This mode saves the most power."

•Page 108 of 586, description of the first paragraph in 7.7.3.3 is modified as follows:
"The MCU exits stop mode by a hardware reset, NMI, low voltage detection interrupt, or a peripheral interrupt assigned to software interrupt number from 0 to 63."

•Page 116 of 586, description of Note 1 in Figure 10.1 is modified as follows:
"The peripheral interrupts are generated by the corresponding peripherals in the MCU."

•Page 117 of 586, descriptions in the second paragraph of (5) in 10.2 are modified as follows:
"The stack pointer (SP) used for this interrupt differs depending on the software interrupt numbers. For software interrupt numbers 0 to 127, when an interrupt request is accepted, the U flag is saved and set to 0 to select the interrupt stack pointer (ISP) during the interrupt sequence. The saved data of the U flag is restored upon returning from the interrupt handler. For software interrupt numbers 128 to 255, the stack pointer does not change during the interrupt sequence."

•Page 119 of 586, description of 10.5 is corrected as follows:
"Each interrupt vector has a 4-byte memory space, in which the start address of the associated interrupt handler is stored. When an interrupt request is accepted, a jump to the address set in the interrupt vector takes place. Figure 10.2 shows an interrupt vector."

•Page 120 of 586, description in the Remarks for the BRK instruction in Table 10.1 is corrected as follows:
"If address FFFFFFE7h is FFh, a jump to the interrupt vector of software interrupt number 0 in the relocatable vector table takes place"

•Page 127 of 586, description for the IR bit below Figure 10.4 is corrected as follows:
"The IR bit becomes 1 (interrupt requested) when an interrupt request is generated; this bit setting is retained until the interrupt request is accepted. When the request is accepted and a jump to the corresponding interrupt vector takes place, the IR bit becomes 0 (no interrupt requested). The IR bit can be set to 0 by a program. This bit should not be set to 1."

•Page 131 of 586, description of Note 1 in Table 10.7 is corrected as follows:
"These are the values when the interrupt vectors are aligned to the addresses in multiples of 4 in the internal ROM. However, the condition does not apply to the fast interrupt."

•Page 134 of 586, Figure 10.8 is corrected as follows:

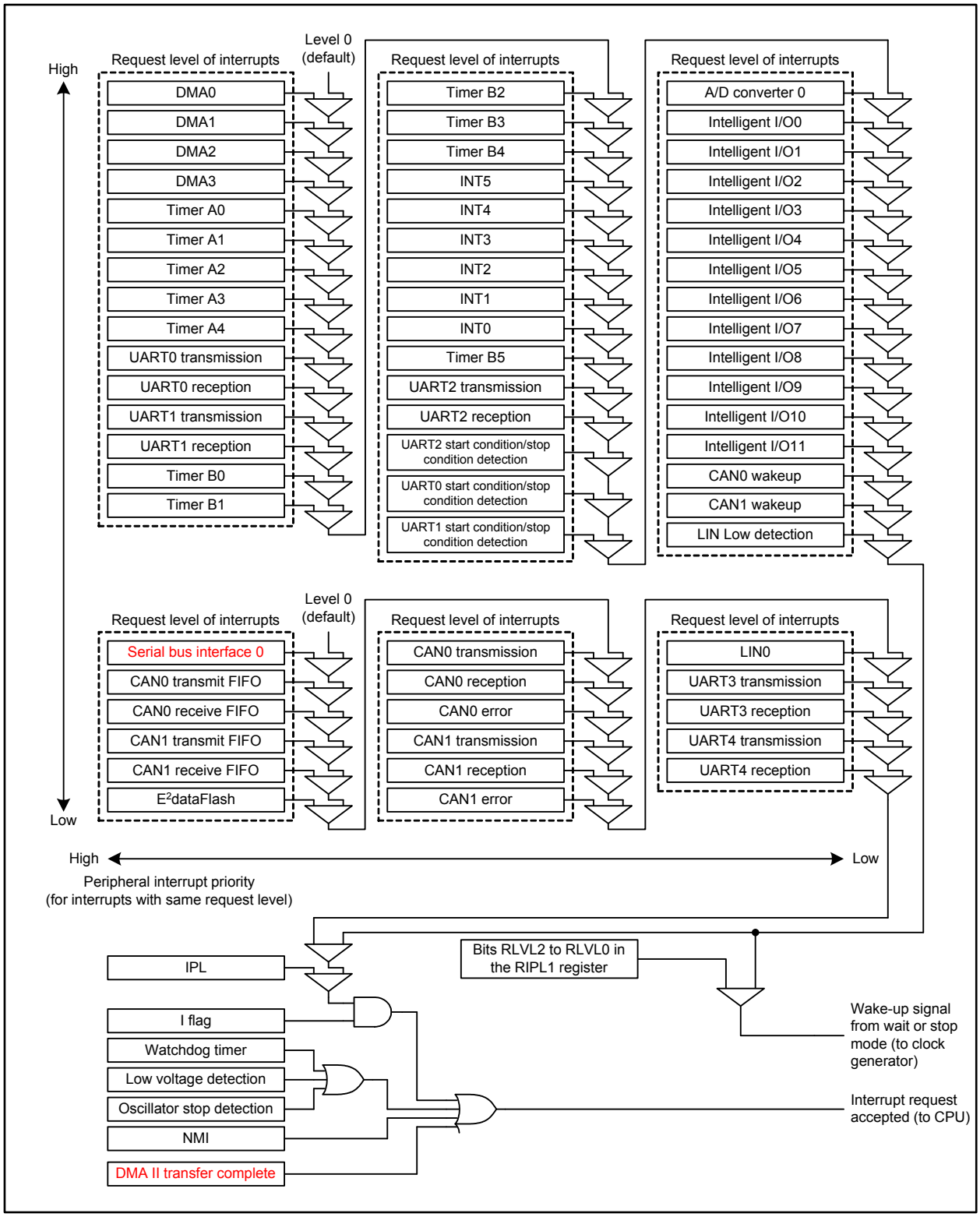


Figure 10.8 Priority Resolver

(Description “Bits RLVL2 to RLVL0 in the RIPL2 register” and associated signal lines are deleted from Figure 10.8)

•Page 137 of 586, register symbol “IIOiE” in line 16 of 10.12 is corrected as follows:
“IIOiIE”

•Page 138 of 586, descriptions for b0 and Note 3 in Figure 10.13 are corrected as follows:
b0: “No register bit; this bit is read as 1” (“should be written with 0 and” is deleted)
Note 3: “When this bit is function-assigned, it can only be set to 0. It should not be set to 1. To set it to 0, either the AND or BCLR instruction should be used; when the bit is not function-assigned (reserved), it should be set to 0.”

•Page 141 of 586, description of the second paragraph in 11. Watchdog Timer is corrected as follows:
“Select either an interrupt request or a reset with the CM06 bit in the CM0 register for when the watchdog timer underflows. Once the CM06 bit is set to 1 (reset), it cannot be changed to 0 (watchdog timer interrupt) by a program. It can be set to 0 only by a reset.”

•Page 141 of 586, register symbol “WKD” in line 9 of 11. Watchdog Timer is corrected as follows:
“WDK”

•Page 141 of 586, description of the paragraph below the formula in 11. Watchdog Timer is corrected as follows:
“For example, when the peripheral bus clock is selected as the count source and it is 1/2 of 48 MHz CPU clock and the prescaler has a divide-by-16 operation, the watchdog timer period is approximately 21.8 ms.”

•Page 142 of 586, the following descriptions are added to Figure 11.2 as Notes 1 and 2:
Note 1: “When the on-chip oscillator clock is used as the count source, the read value may be undefined due to a change in the count value while being read.”
Note 2: “Set this bit before activating the watchdog timer.”

•Page 143 of 586, the following description is added to Figure 11.3 as Note 2:
“Set these bits before activating the watchdog timer.”

•Page 144 of 586, the following description is added to Figure 11.5 as Note 3:
“These bit settings are disabled when the WDTON bit is 1. The values set to these bits are reflected to registers WDK and PM2 when the WDTON bit is 0.”

•Page 146 of 586, expression “a value more than 00000001h” in the Specification of the DMA transfer startup in Table 12.1 is corrected as follows:
“a value other than 00000000h”

•Page 154 of 586, description of the first paragraph in 12.1 is corrected as follows:
“The transfer cycle is composed of bus cycles to read data from (source read) or to write data to (destination write) memory or an SFR.”

•Page 160 of 586, address “FFFFFFFh” in Note 1 of Table 13.1 is corrected as follows:
“FFFFFFFFh”

•Page 160 of 586, bit symbol “IIRLT” in the fifth bullet point of 13.1 is corrected as follows:
“IRLT”

•Pages 162 and 163 of 586, expression “DMA II transfer complete interrupt vector address” in Figure 13.2 and the seventh bullet point of 13.1.2 is corrected as follows:
“jump address for the DMA II transfer complete interrupt handler”

•Pages 162 and 165 of 586, expression “interrupt vector” in Figure 13.2 and 13.1.4 is corrected as follows:
“interrupt vector space”

•Page 163 of 586, description “jump address” in the seventh bullet point of 13.1.2 is corrected as follows:
“start address”

•Page 164 of 586, bit names of the OPER bit and bits CNT0 to CNT2 in Figure 13.3 are modified as follows:
OPER: “Calculation Result Transfer Select Bit”
CNT0 to CNT2: “Number of Transfers Setting Bit”

•Page 173 of 586, Figure 15.2 is corrected as follows:

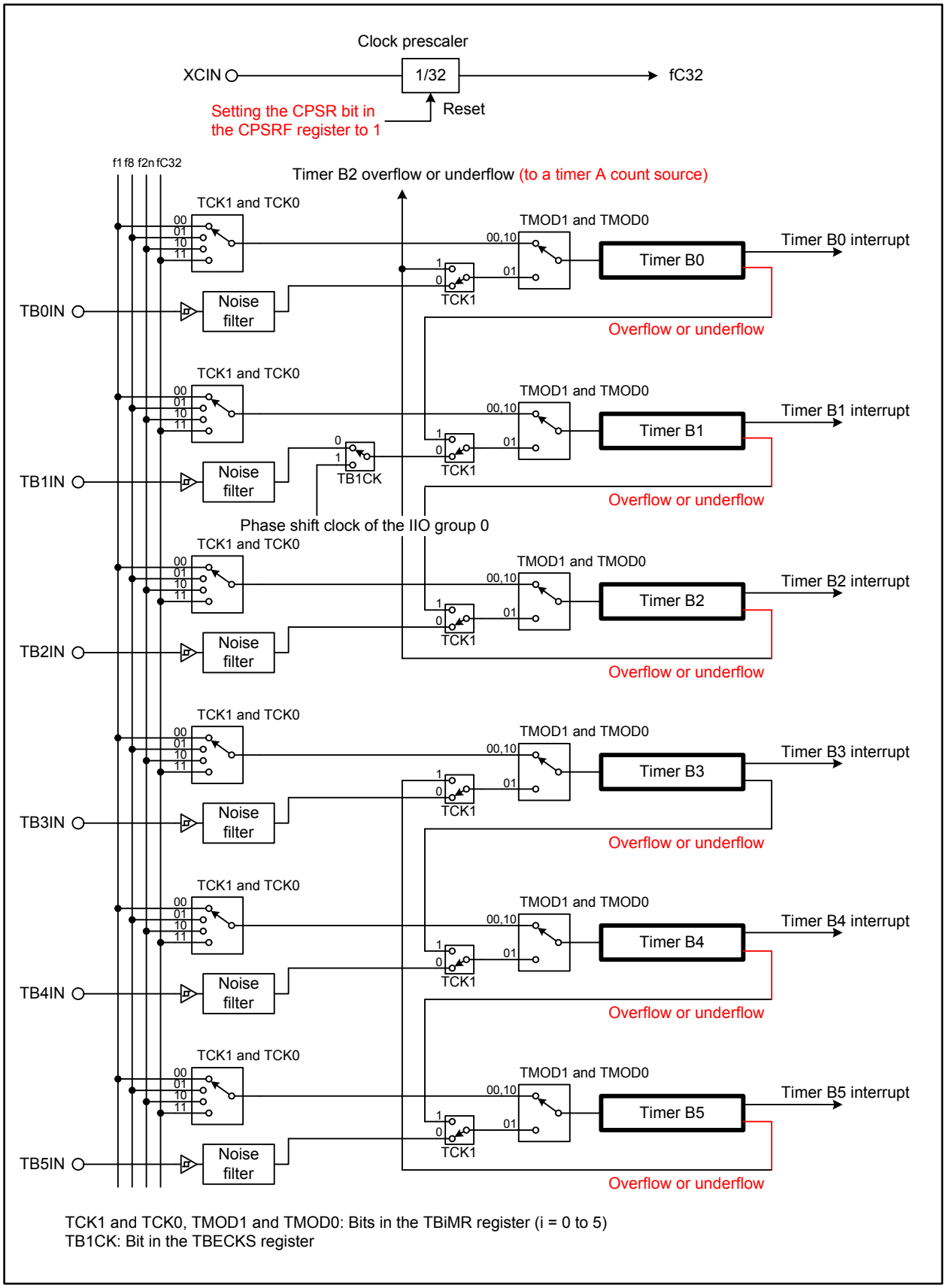


Figure 15.2 Timer B Configuration

•Page 177 of 586, expression “Counting” is deleted from bit names of bits TA0UD to TA4UD and the register name in Figure 15.7

•Page 185 of 586, bit name of the MR2 bit in Figure 15.12 is modified as follows:
“Increment/Decrement Switching Source Select Bit”

•Page 185 of 586, bit symbols “TAiTGH and TAiTGL” in Note 5 of Figure 15.12 are corrected as follows:
“TAjTGH and TAjTGL”

•Page 187 of 586, register symbol “TA4NR” in line 3 of 15.1.3 is corrected as follows:
“TA4MR”

•Page 205 of 586, description in the first bullet point of 15.3.3.2 is corrected as follows:
“While the TBjS bit in the TABSR or TBSR register is 1 (start counter), after the MR3 bit becomes 1 (overflow) and at least one count source cycle has elapsed, a write operation to the TBjMR register sets the MR3 bit to 0 (no overflow).”

•Page 205 of 586, expression “TBj interrupt handler” in the eighth bullet point of 15.3.3.2 is changed as follows:
“timer Bj interrupt handler”

•Page 209 of 586, descriptions of functions of the INV13 bit in Figure 16.3 are corrected as follows:
“0: Timer A1 reload control signal is 0
1: Timer A1 reload control signal is 1”

•Page 209 of 586, description of Note 1 in Figure 16.3 is corrected as follows:
“Set this register after setting the PRC1 bit in the PRCR register to 1 (write enabled). Also, rewrite this register while timers A1, A2, A4, and B2 are stopped.”

•Page 213 of 586, descriptions of functions of bits MR2 and MR3 in Figure 16.8 are corrected as follows:
MR2: “No register bit; should be written with 0 and read as undefined value”
MR3: “Disabled when using the three-phase motor control timers. Should be written with 0 and read as undefined value”

•Page 214 of 586, description of function of the PWCON bit in Figure 16.9 is corrected as follows:
“1: The underflow of timer B2 when the reload control signal for timer A1 is 0”

•Page 215 of 586, description “The sum of setting values for registers TAi and TAi1 should be identical to the setting value of the TB2 register in this mode.” is deleted from lines 8 to 9 of 16.3

•Page 215 of 586, description in line 11 of 16.3 is corrected as follows:
“Figure 16.11 shows registers TA1M, TA2M, TA4M, TA11M, TAM21M, and TA41M in this function.”

•Page 220 of 586, bit symbol “INV06” in Note 3 of Figure 16.16 is corrected as follows:
“INV16”

•Page 221 of 586, register symbol “INV1” in Note 2 of Figure 16.18 is corrected as follows:
“INVC1”

•Page 223 of 586, description of 16.6.1 is corrected as follows:
“When a low signal is applied to the $\overline{\text{NMI}}$ pin with the following bit settings, pins TA1OUT, TA2OUT, and TA4OUT become high-impedance: the PM24 bit in the PM2 register is 1 (NMI enabled), the SDE bit in the IOBC register is 1 (shutdown enabled), the INV02 bit in the INVC0 register is 1 (three-phase motor control timers used), and the INV03 bit is 1 (three-phase motor control timer output enabled).”

•Page 223 of 586, description of 16.6.2 is corrected as follows:
"Do not write to the TAi1 register before and after timer B2 underflows (i = 1, 2, 4). Before writing to the TAi1 register, read the TB2 register to verify that sufficient time remains until timer B2 underflows. Then, immediately write to the TAi1 register so no interrupt handling is performed during this write procedure. If the TB2 register indicates little time remains until the underflow, write to the TAi1 register after timer B2 underflows."

•Pages 229 and 230 of 586, descriptions for the CRD bit in Figures 17.5 and 17.6 are modified as follows:

Bit Symbol	Bit Name	Function	RW
CRD	CTS Function Disable Bit	0: CTS function enabled 1: CTS function disabled	RW

•Page 229 of 586, Note 1 "Bits CNT3 to CNT0 in the TCSPR register select a divide ratio from two options: no division (n = 0) or divide-by-2n (n = 1 to 15)." is deleted from Figure 17.5.

•Page 231 of 586, description of function of the UiIRS bit in Figure 17.7 is modified as follows:
"0: Transmit buffer is empty (TI = 1)
1: Transmission is completed (TXEPT = 1)"

•Page 233 of 586, description of function of the SWC bit in Figure 17.11 is modified as follows:
"0: No wait-state/wait-state cleared
1: Hold the SCLi pin low after the eighth bit is received"

•Page 234 of 586, description "UiBRG count source" in the function of bits DL0 to DL2 in Figure 17.12 is corrected as follows:
"baud rate generator count source"

•Page 235 of 586, description of function of the SWC9 bit in Figure 17.13 is modified as follows:
"0: No wait-state/wait-state cleared
1: Hold the SCLi pin low after the ninth bit is received"

•Pages 235 and 261 of 586, bit symbol "STARREQ" in Note 3 of Figure 17.13 and line 1 of 17.3.2 is corrected as follows:
"STAREQ"

•Page 241 of 586, description "TXEPT flag" in Figure 17.18 is corrected as follows:
"TXEPT bit"

•Page 241 of 586, bit symbol "UiRS" in the fourth dash of Figure 17.18 is corrected as follows:
"UiIRS"

•Pages 249 and 250 of 586, descriptions of functions of the UiIRS bit in Figures 17.23 and 17.24 are corrected as follows:
0: "(an interrupt request is generated when the transmit buffer is empty)"
1: "(an interrupt request is generated when transmission is completed)"

•Pages 253 and 254 of 586, description "Transmit/receive clock" in Figures 17.27 and 17.28 is corrected as follows:
"CLKi"

•Page 271 of 586, description of the fourth dash in 17.5.3.1 is moved as follows:
"- The TE bit in the UiC1 register is 1 (transmission enabled).
- The RE bit in the UiC1 register is 1 (reception enabled). This bit setting is not required when only transmitting.
- The TI bit in the UiC1 register is 0 (data held in the UiTB register)."

•Page 284 of 586, description in 18.1.5 is modified as follows:
"In repeat sweep mode 1, the analog voltage applied to eight selected pins including one to four prioritized pins is repeatedly converted into a digital code. Table 18.6 lists specifications of repeat sweep mode 1."

•Page 284 of 586, description for the function in Table 18.6 is modified as follows:
"The analog voltage applied to eight selected pins including one to four prioritized pins is repeatedly converted into a digital code. The prioritized pins are selected by setting bits SCAN1 and SCAN0 in the AD0CON1 register and bits APS1 and APS0 in the AD0CON2 register"

•Page 291 of 586, description "AD0i register" in the ninth bullet point of 18.3.2 is modified as follows:
"AD00 register"

•Page 292 of 586, description "CRC_CCITT" in line 2 of 19. CRC Calculator is corrected as follows:
"CRC-CCITT"

•Page 292 of 586, Figure 19.1 is corrected as follows:

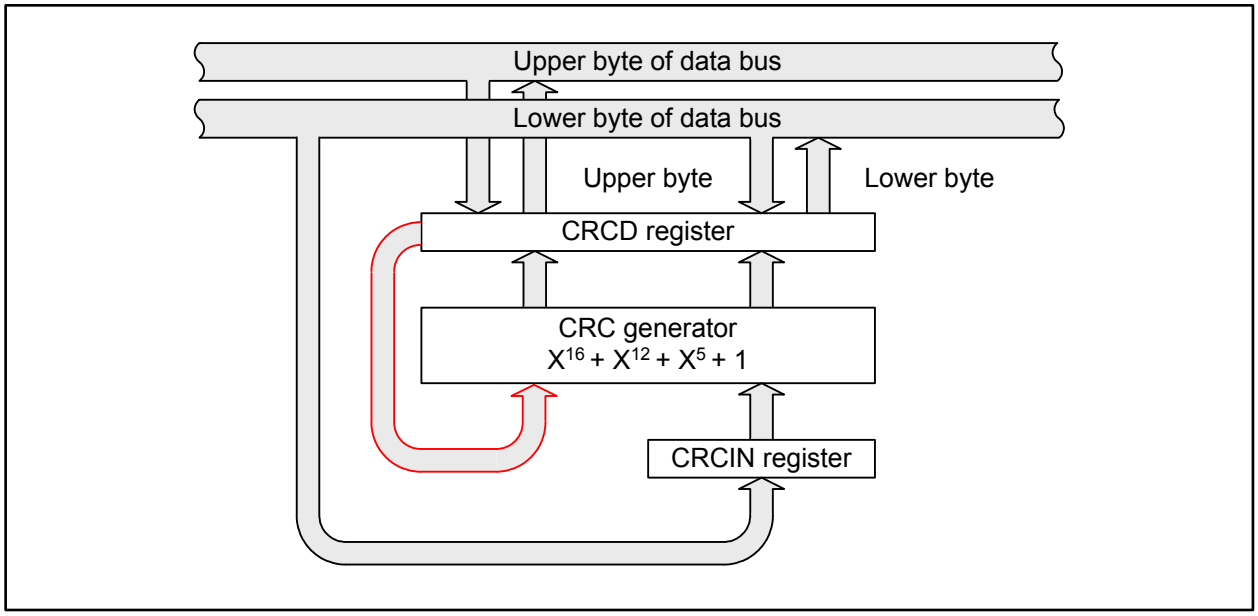


Figure 19.1 CRC Calculator Block Diagram

•Page 300 of 586, description "Request from the $\overline{INT0}$ pin" in Figure 21.1 is corrected as follows:
"Request from the $\overline{INT0}$ pin or the $\overline{INT1}$ pin"

•Page 303 of 586, descriptions for bits RST2, UD0, and UD1 in Figure 21.4 are modified as follows:

Bit Symbol	Bit Name	Function	RW
RST2	Base Timer Reset Source Select Bit 2	0: No reset 1: Low signal input into the INT0/INT1 pin (2)	RW

UD0	Increment/Decrement Control Bit	b6 b5 0 0 : Increment mode 0 1 : Increment/decrement mode 1 0 : Two-phase pulse signal processing mode (3) 1 1 : Do not use this combination	RW
UD1			RW

•Page 303 of 586, the following description is added to Figure 21.4 as Note 2:
"The base timer is reset by an input of low signal to the external interrupt input pin selected for the UD0Z signal by the IFS2 register."

•Page 304 of 586, Note 3 "The GOC bit becomes 0 after gating is cleared." is deleted from Figure 21.5.

•Page 311 of 586, description in the second bullet point for the reset conditions in Table 21.2 is corrected as follows:
"An input of low signal into the external interrupt pin (INT0 or INT1) as follows:
for group 0: selected using the IFS22 bit in the IFS2 register"

•Page 311 of 586, description in the first bullet point for the selectable functions in Table 21.2 is corrected as follows:
"The base timer starts counting when the BTS bit is set to 1. When the base timer reaches FFFFh, it starts decrementing. When the RST1 bit in the G0BCR1 register is 1 (the base timer is reset by matching with the G0PO0 register), the timer counter starts decrementing two counts after the base timer value matches the G0PO0 register setting. When the timer counter reaches 0000h, it starts incrementing again (refer to Figure 21.16)."

•Page 312 of 586, description "Low signal input to the INT0 pin" in Figure 21.14 is corrected as follows:
"Low signal input to the INT0/INT1 pin"

•Page 315 of 586, description "INT0" in Figure 21.17 is corrected as follows:
"INT0/INT1"

•Pages 322, 324, and 327 of 586, description "Input to the IIO0_j pin" in Figures 21.21 to 21.23 is corrected as follows:
"IIO0_j pin"

•Page 333 of 586, bit symbol "SBUMS" in 22. Serial Bus Interface is corrected as follows:
"SSUMS"

•Pages 334 and 336 of 586, pin name "SS0CK" and register symbol "SS0RDR" in Tables 22.1 and 22.2 are corrected as follows:
"SSCK0" and "SS0TDR"

•Page 336 of 586, descriptions "SSI0 (I): Data input pin" and "SSO0 (O): Data output pin" for the I/O pins in Table 22.2 are corrected as follows:
"SSI0 (I/O): Data I/O pin" and "SSO0 (I/O): Data I/O pin"

•Page 338 of 586, description “b6 b5 b4” in Figure 22.3 is corrected as follows:
“b2 b1 b0”

•Page 360 of 586, bit symbol “MSL” in line 15 of 22.1.7 is corrected as follows:
“MLS”

•Page 368 of 586, descriptions “Break dominant” and “Break delimiter” in Table 23.1 are modified as follows:
“Transmit break length” and “Transmit break delimiter length”

•Page 369 of 586, pin names “LINOUT” and “LININ” in Figure 23.1 are corrected as follows:
“LIN0OUT” and “LIN0IN”

•Page 372 of 586, the following description is added to Figure 23.3 as Note 1:
“No interrupt is generated by the input signal low detection when this bit is 1.”

•Page 374 of 586, description in Note 4 of Figure 23.7 is modified as follows:
“The LD bit in the LST register becomes 1 and an interrupt request is generated in the following cases:
- When the falling edge of the input signal is detected when this bit is 1.
- When this bit is set to 1 while the input signal is low.”

•Page 377 of 586, bit names “Break Transmission Setting Bit” and “Break Delimiter Transmission Setting Bit” in Figure 23.10 are modified as follows:
Bits BLT0 to BLT3: “Transmit Break (Low) Length Setting Bit”
Bits BDT0 and BDT1: “Transmit Break Delimiter (High) Length Setting Bit”

•Page 379 of 586, reset value “XXXX XX00b” in Figure 23.14 is corrected as follows:
“0000 0000b”

•Page 379 of 586, description of b7 to b2 in Figure 23.14 is modified as follows:
“No register bits; should be written with 0 and read as 0”

•Pages 380 and 381 of 586, description in Note 1 of Figures 23.16 and 23.17 is modified as follows:
“These bits do not become 0 automatically. Set them to 0 by a program. Writing 1 to these bits has no effect.”

•Page 380 of 586, the following description is added to Figure 23.16 as Note 3:
“When this bit is 1, no interrupt request is generated even if the conditions of the LD bit becoming 1 are satisfied again.”

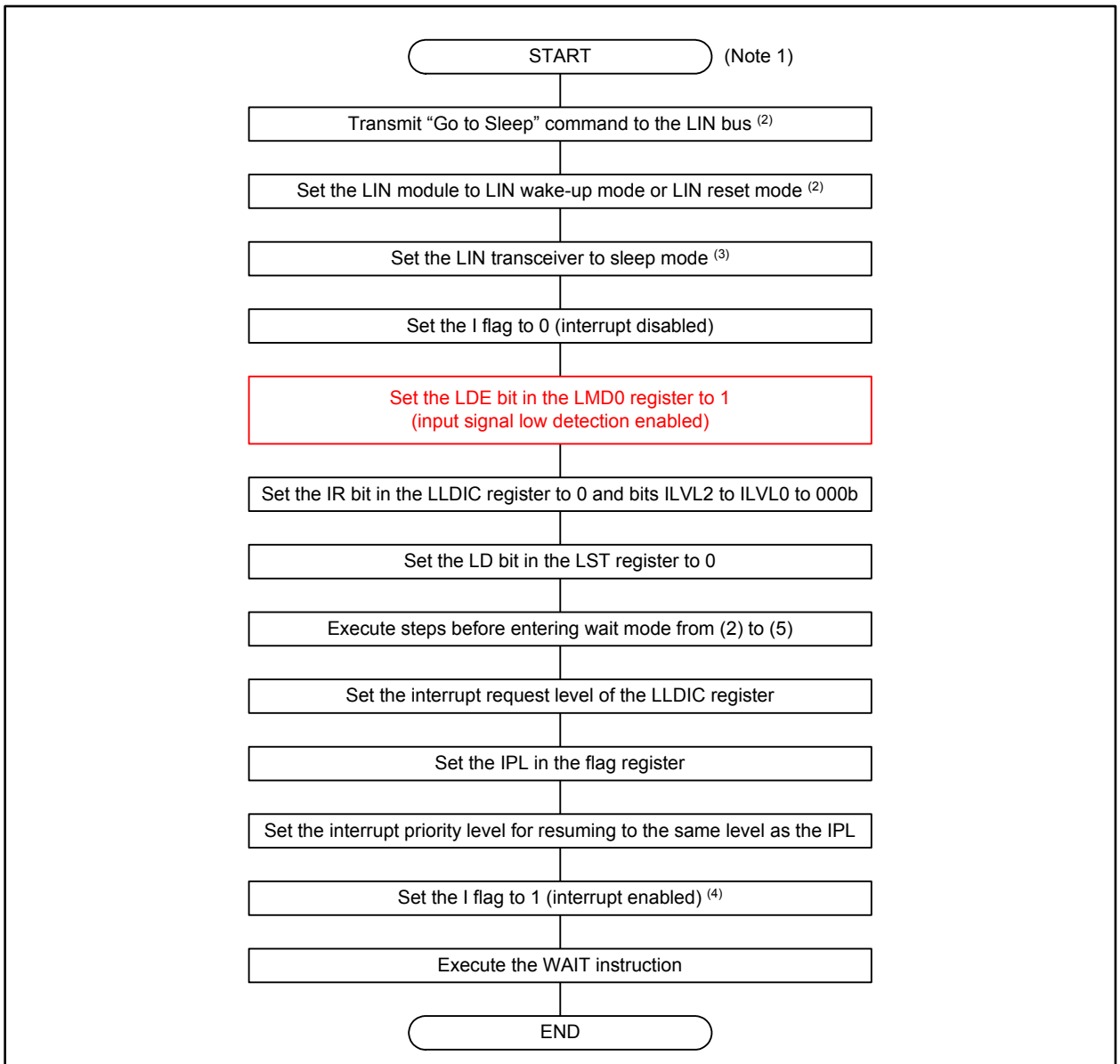
•Page 385 of 586, bit symbols “BFTL3 to BFTL0” and “BFTD1 and BFTD0” in Table 23.3 are corrected as follows:
“BLT3 to BLT0” and “BDT1 to BDT0”

•Page 386 of 586, description in (4) for “LIN Module Processing” in Table 23.4 is changed as follows:
“Transmit Data 2, then the next interbyte space
Transmit data 3, then the next interbyte space
(Repeat this process for the data length specified in bits RFDL3 to RFDL0 in the LRFC register. Go to (6) if an error occurs.)”

•Page 387 of 586, description in (4) for “LIN Module Processing” in Table 23.5 is changed as follows:
“Receive Data 2 due to start bit detection
Receive Data 3 due to start bit detection
(Repeat this process for the data length specified in bits RFDL3 to RFDL0 in the LRFC register. Abort the reception and go to (5) if an error occurs. Checksum judgement is not performed in this case.)”

•Page 389 of 586, description “BPR0” in Note 1 of Table 23.6 is corrected as follows:
“BRP0”

•Page 396 of 586, Figure 23.30 is corrected as follows:



Notes:
1. This flowchart shows an example of the setting procedure to exit wait mode using a wake-up signal from the LIN bus after entering wait mode.
2. Set the LIN module in PLL mode (high speed mode or medium speed mode).
3. The setting depends on the LIN transceiver specification.
4. Enter low speed mode or low power mode before setting the I flag to 1.

Figure 23.30 Example of Setting Before Transition to Wait Mode

•Page 397 of 586, description for the Input signal Low detection row in Table 23.8 is modified as follows:
“When the falling edge of input signal at the LIN0IN pin is detected with the setting of the LDE bit in the LMD0 register to 1 (input signal low detection enabled), or when setting the LDE bit to 1 while the LIN0IN pin is low”

•Page 400 of 586, the following description is added to line 8 of 23.11:
"No new interrupt request is generated by the other sources if any of them is 1 since multiple interrupt sources are aggregated."

•Page 400 of 586, Figure 23.32 is corrected as follows:

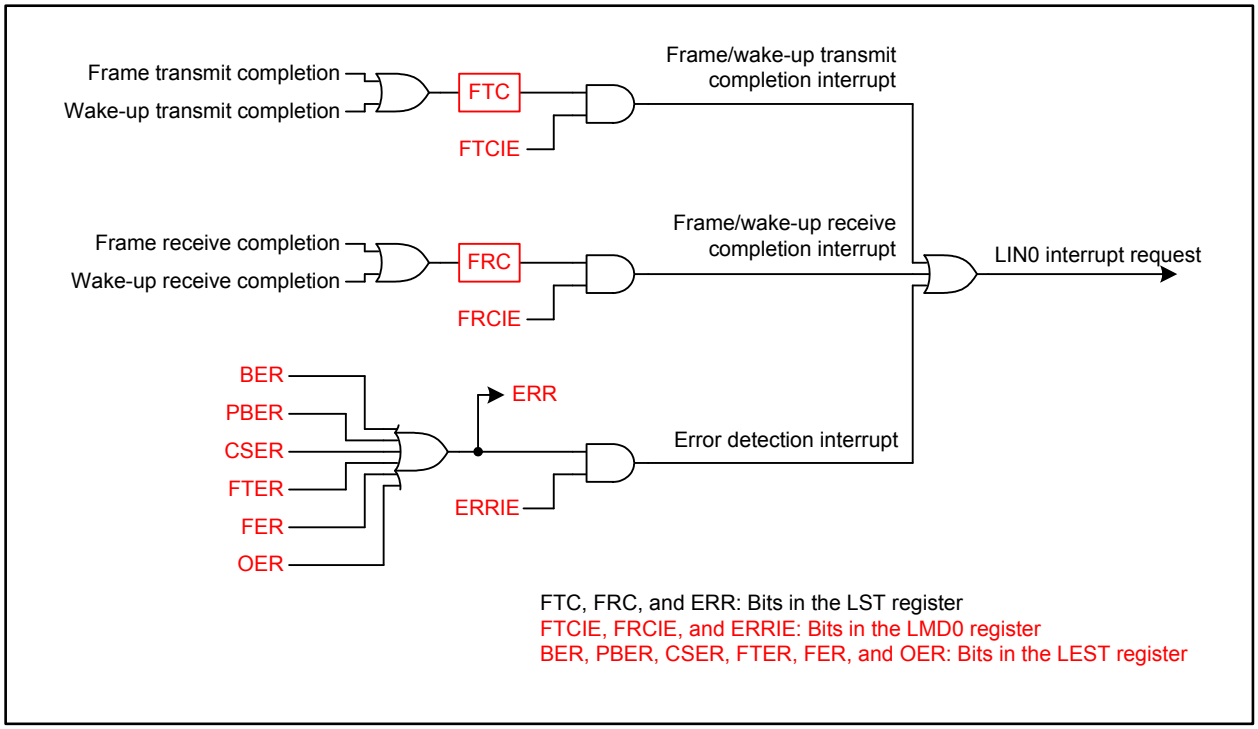


Figure 23.32 LIN0 Interrupt Block Diagram

•Page 400 of 586, Figure 23.33 is corrected as follows:

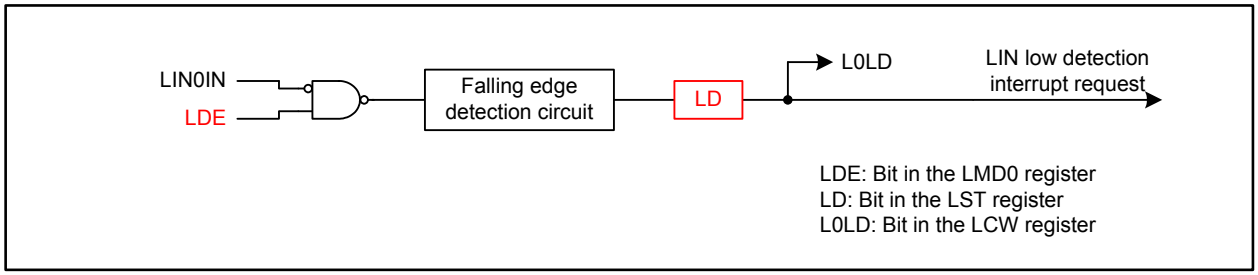


Figure 23.33 LIN Low Detection Interrupt Block Diagram

•Page 401 of 586, table number "Table 24.1" in line 5 of 24. CAN Module is modified as follows:
"Tables 24.1 and 24.2"

•Page 405 of 586, descriptions for the RBOC bit in Figure 24.2 are modified as follows:

Bit Symbol	Bit Name	Function	RW
RBOC	Forced Recovery From Bus-off Bit (4)	0: Nothing occurred 1: Forced recovery from bus-off (5)	RW

•Page 422 of 586, description “fCAN (CAN system clock)” in line 4 of 24.1.9.5 is modified as follows:
“the peripheral bus clock”

•Page 424 of 586, description of Note 2 in Figure 24.11 is modified as follows:
“When setting the RFE bit to 0, set the RFMLF bit to 0 as well.”

•Page 425 of 586, description “fCAN” in line 5 of 24.1.10.3 is modified as follows:
“the peripheral bus clock”

•Page 431 of 586, description of function of b7 in Figure 24.17 is corrected as follows:
b7: “No register bit; this bit is read as 0” (“should be written with 0 and” is deleted)

•Page 455 of 586, description of the first paragraph in 24.2.3 is modified as follows:
“CAN sleep mode is used for reducing current consumption by stopping the clock supply to the CAN module. After a MCU reset, the CAN module starts from CAN sleep mode.”

•Page 456 of 586, register symbol “CiSTR” in 24.2.4 is corrected as follows:
“CiTCR”

•Page 458 of 586, q value “q = 1, 2, 3, 4” in Figure 24.36 is corrected as follows:
“q = 2, 3, 4”

•Page 470 of 586, description in the first paragraph of 25. I/O Pins is corrected as follows (refer to TN-16C-A198A/E):
“Each pin of the MCU functions as a programmable I/O port or an I/O pin for internal peripherals. These functions can be switched by the function select registers. The pull-up resistors are enabled for every group of four pins. However, a pull-up resistor is separated from other peripheral functions even if it is enabled, when a pin functions as an output pin.” (“or an analog I/O pin” is deleted)

•Page 470 of 586, Figure 25.1 is corrected as follows (refer to TN-16C-A198A/E):

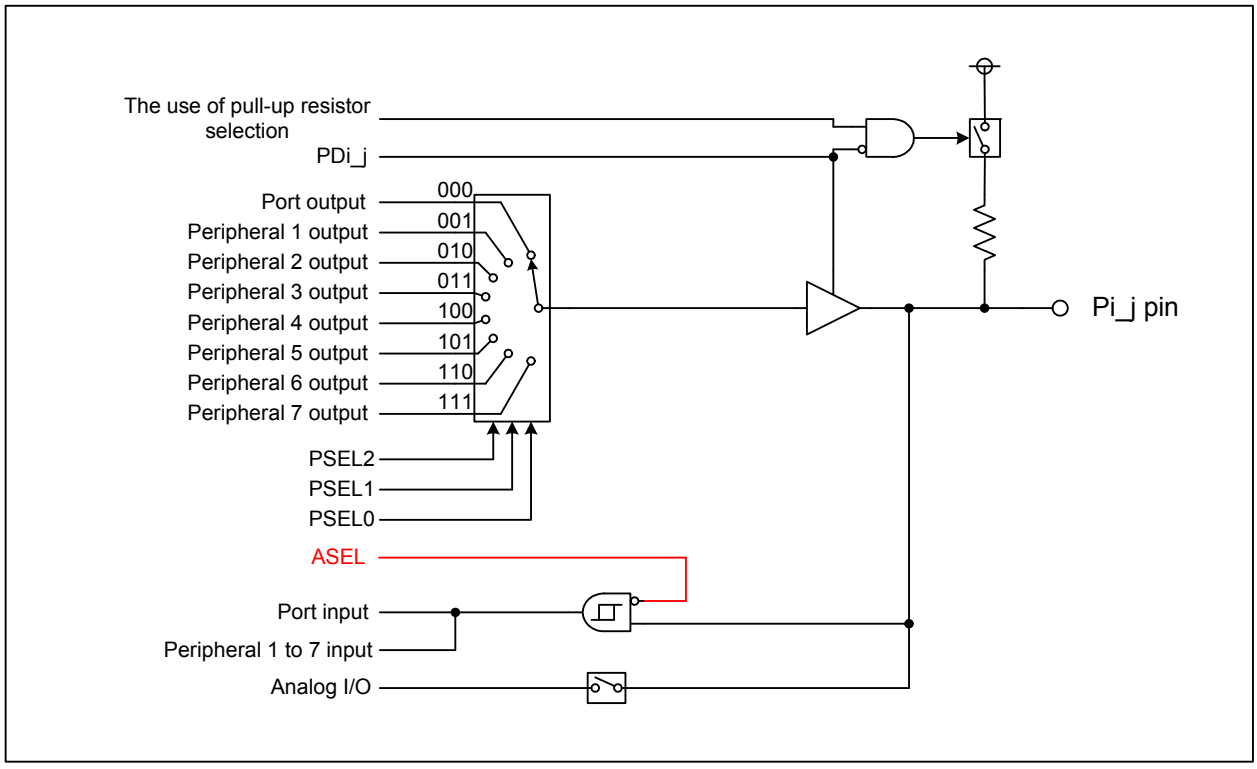


Figure 25.1 Typical I/O Pin Block Diagram (i = 0 to 9; j = 0 to 7)

•Page 470 of 586, description in the last paragraph of 25. I/O Pins is corrected as follows:
"The input-only port P8_5 shares a pin with $\overline{\text{NMI}}$ and has no function select register or bit 5 in the PD8 register. Port P9_1 also functions as an input-only port. The function select register and bit 1 in the PD9 register are reserved. Port P9 is protected from unexpected write accesses by the PRC2 bit in the PRCR register. Ports P3, P7, and P8 are protected from unexpected write accesses by the PRC30 bit in the PRCR3 register (refer to 9. "Protection")."

•Page 474 of 586, reset value "XXXX X000b" for registers P1_0S to P1_4S in Figure 25.4 is corrected as follows:
"0XXX X000b"

•Pages 474 and 478 of 586, description "IIO0 output" in Figures 25.4 and 25.8 is changed as follows:
"IIO0_i output"

•Page 476 of 586, description "PD3_i register" in line 4 below Figure 25.6 is corrected as follows:
"PD3_i bit"

•Page 480 of 586, addresses of registers P7_4S to P7_6S in Figure 25.10 are corrected as follows:
P7_4S: "400D9h"
P7_5S: "400DBh"
P7_6S: "400DDh"

•Page 493 of 586, descriptions in Table 26.3 are corrected as follows:

Protection Type	Lock Bit Protection	ROM Code Protection	ID Code Protection
Protected operations	Erase, write	Read, write	Read, erase, write

("erase" is deleted from the ROM Code Protection column)

Protection disabled by	Setting the LBD bit in the FMR register to 1 (lock bit protection disabled), or by erasing the blocks whose lock bits are set to 0 to permanently disable the protection	Erasing all blocks whose protect bits are set to 0	Sending a proper ID code from the serial programmer

("by using the serial programmer" is deleted from the ROM Code Protection column)

•Page 493 of 586, description "use the serial programmer to" is deleted from line 3 of 26.2.2.

•Page 494 of 586, Figure 26.2 is corrected as follows:

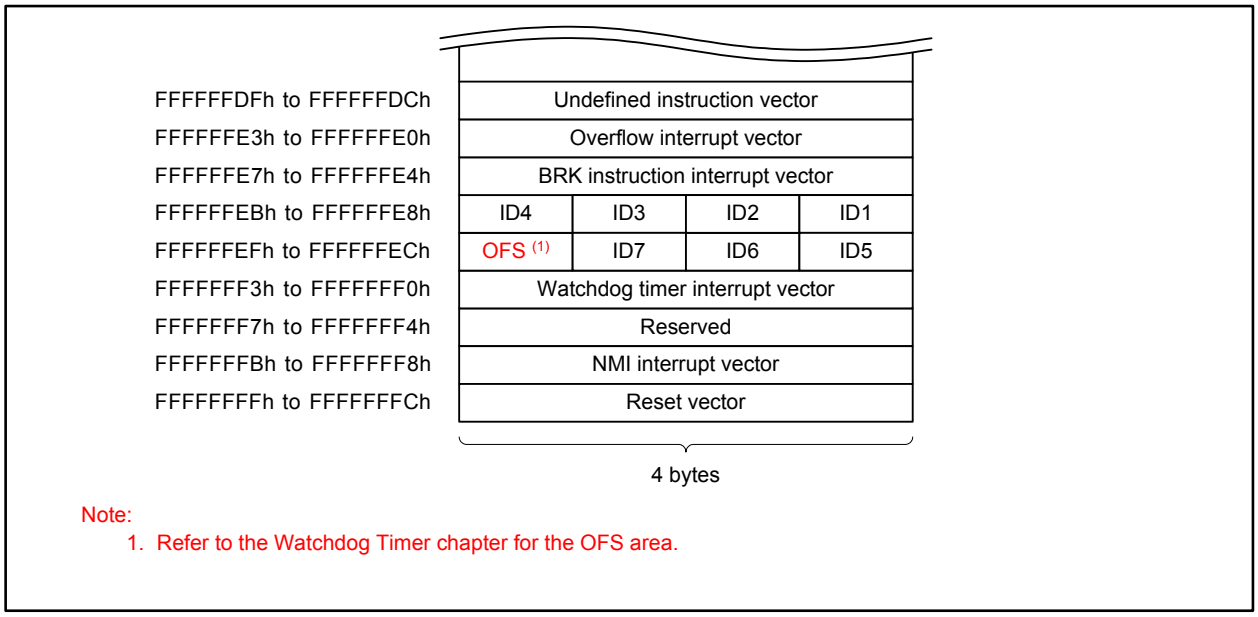


Figure 26.2 Addresses for ID Code Stored

•Page 496 of 586, descriptions in Table 26.5 are modified as follows:

Restrictions on software commands	None	• Do not execute either the program command or the block erase command for blocks where the rewrite control programs are written to • Do not execute the enter read status register mode command • Execute the enter read lock bit status mode command in RAM • Execute the enter read protect bit status mode command in RAM

Flash memory state detection by	• Reading the FMSR0 register by a program • Executing the enter read status register mode command to read data	• Reading the FMSR0 register by a program

•Pages 502 and 504 of 586, descriptions in Figures 26.12 and 26.13 are corrected as follows:

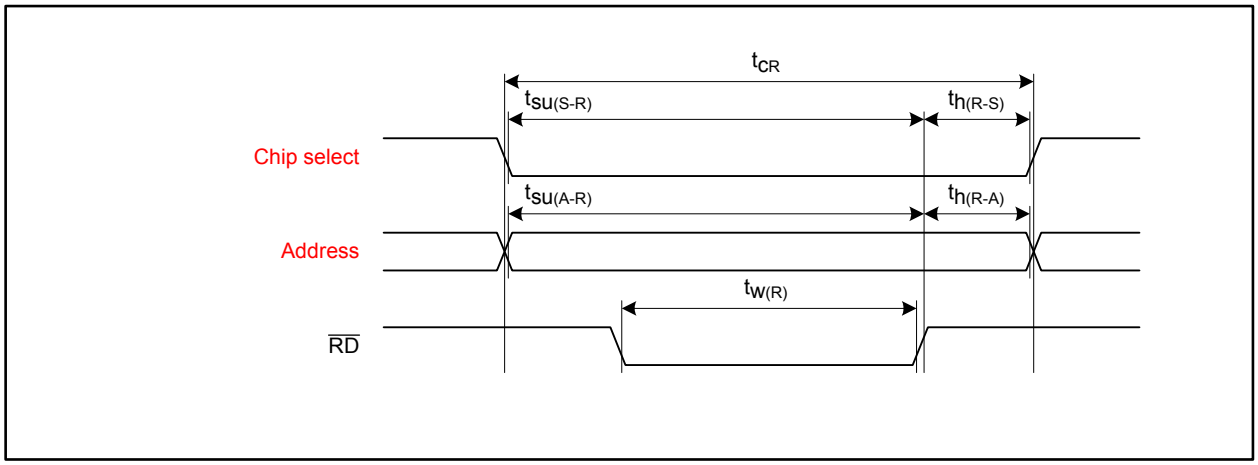


Figure 26.12 Read Timing

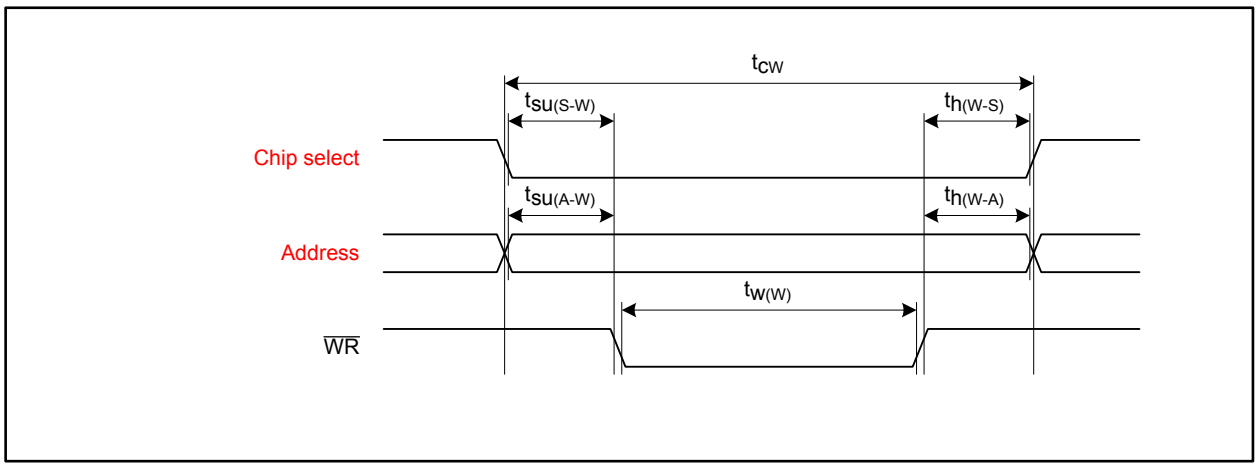


Figure 26.13 Write Timing

•Page 522 of 586, the following description is added to Note 3 of Figure 27.2:
"However, the registers are not initialized."

•Page 522 of 586, description "This mode setting prevents data from being overwritten if a program goes out of control." is deleted from Note 5 in Figure 27.2.

•Page 528 of 586, description "EERR bit in the E2FS0 register is 1?" in Figure 27.12 is corrected as follows:
"EERR bit in the E2FS0 register is 0?"

•Pages 537 and 538 of 586, description "Programming and erasure endurance of flash memory" in Tables 28.8 and 28.9 is changed as follows:
"Program/erase cycles"

•Pages 537 and 538 of 586, unit "times" for "Programming and erasure endurance of flash memory" in Tables 28.8 and 28.9 is corrected as follows:
"Cycles"

•Page 541 of 586, descriptions in Figure 28.5 are corrected as follows:

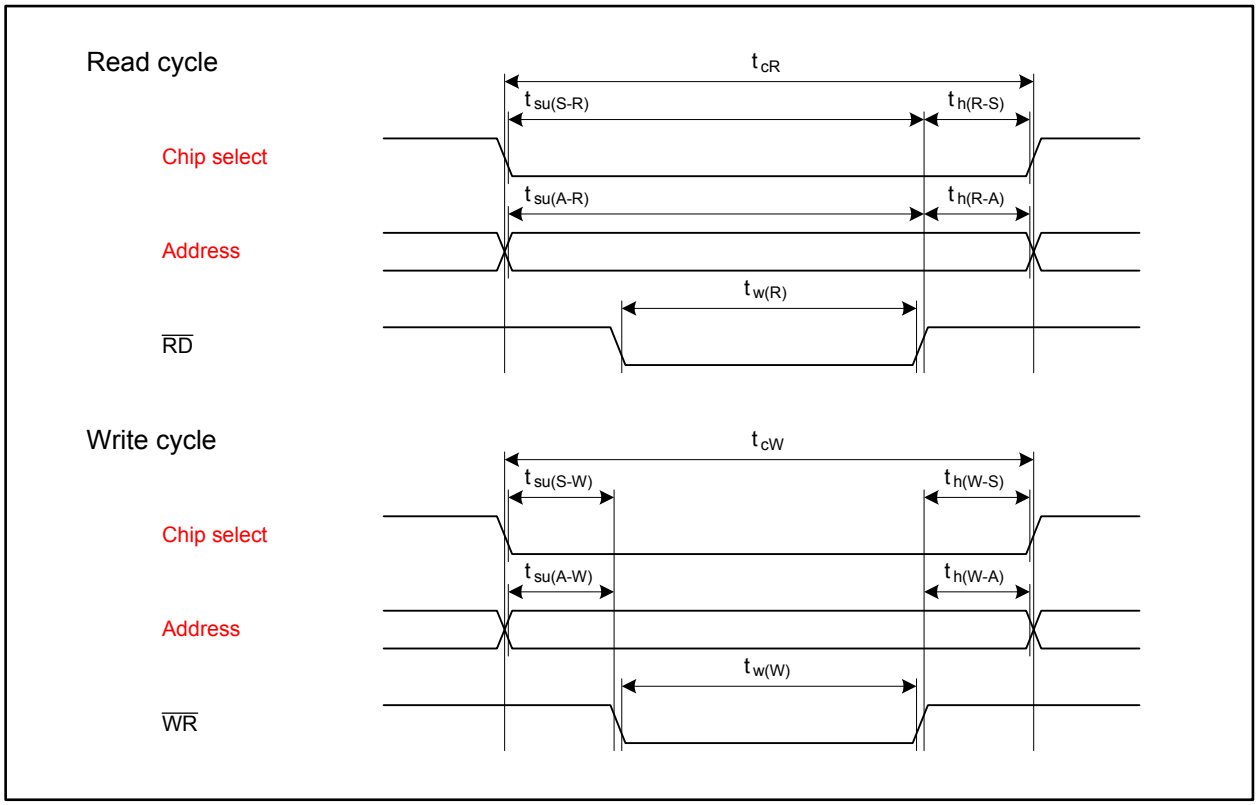


Figure 28.5 Flash Memory CPU Rewrite Mode Timing

•Pages 543 and 553 of 586, pin name “LININ” in Tables 28.17 and 28.36 is corrected as follows:
“LIN0IN”

•Pages 549 and 559 of 586, pin name “INTi” in the title of Tables 28.31 and 28.50 is corrected as follows:
“$\overline{\text{INT}}$i”

•Page 573 of 586, description in the first bullet point of 29.6.3.2 is corrected as follows:
“While the TBjS bit in the TABSR or TBSR register is 1 (start counter), after the MR3 bit becomes 1 (overflow) and at least one count source cycle has elapsed, a write operation to the TBjMR register sets the MR3 bit to 0 (no overflow).”

•Page 573 of 586, expression “TBj interrupt handler” in the eighth bullet point of 29.6.3.2 is changed as follows:
“timer Bj interrupt handler”

•Page 574 of 586, description of 29.7.1 is corrected as follows:
“When a low signal is applied to the $\overline{\text{NMI}}$ pin with the following bit settings, pins TA1OUT, TA2OUT, and TA4OUT become high-impedance: the PM24 bit in the PM2 register is 1 (NMI enabled), the SDE bit in the IOBC register is 1 (shutdown enabled), the INV02 bit in the INVC0 register is 1 (three-phase motor control timers used), and the INV03 bit is 1 (three-phase motor control timer output enabled).”

•Page 574 of 586, description of 29.7.2 is corrected as follows:
“Do not write to the TAi1 register before and after timer B2 underflows (i = 1, 2, 4). Before writing to the TAi1 register, read the TB2 register to verify that sufficient time remains until timer B2 underflows. Then, immediately write to the TAi1 register so no interrupt handling is performed during this write procedure. If the TB2 register indicates little time remains until the underflow, write to the TAi1 register after timer B2 underflows.”

•Page 575 of 586, description of the fourth dash in 29.8.3.1 is moved as follows:

"- The TE bit in the UiC1 register is 1 (transmission enabled).

- The RE bit in the UiC1 register is 1 (reception enabled). This bit setting is not required when only transmitting.

- The TI bit in the UiC1 register is 0 (data held in the UiTB register)."

•Page 577 of 586, description "AD0i register" in the ninth bullet point of 29.9.2 is modified as follows:

"AD00 register"